Ordering Information			
Part Numbers	**Description**	**AMB Vendor**	**Device Vendor**
SG5127FBD225652HCD	512Mx72 (4GB), DDR2, 240-pin Fully Buffered DIMM, ECC, 256Mx4 Based, PC2-5300, DDR2-667-555, 30.35mm, Green Module (RoHS Compliant). Label: 4GB 2Rx4 PC2-5300F-555-11-E_*	IDT, Rev. C1 AMB0482C1RJ	Hynix, Rev. C HY5PS1G431CFP-Y5

* This character defines PCB revision.

(All specifications of this module are subject to change without notice.)

Revision History

- **December 20, 2007**
  Datasheet released.

4GByte (512Mx72) DDR2 SDRAM Module - 256Mx4 Based 240-pin Fully Buffered DIMM, ECC

Features:

Device Speed	CL (Device)	Cycle Time	Link Speed
DDR2-667	3.0/4.0/5.0	3.0ns	4.0Gb/s

- High-Speed differential PTP link between Controller & AMB
- SMBus Interface access to AMB Configuration Registers
- AMB allows up to 8 Double-Rank DIMMs/Channel (288 devices) Transparent Mode for DRAM Test
- MEMBIST and IBIST Test Functions
- $V_{DD} = V_{DDQ}$ = 1.8V +/- 0.1V (for DDR2 SDRAM)
- V_{CC} = 1.5V +/- 0.045V (for AMB)
- V_{TT} = 0.9V +/- 0.036V (DRAM Interface Termination)
- V_{DDSPD} = 3.3V +/- 0.3V
- Dual Rank Module (JEDEC Raw Card “E”)
- Lead Finish : Gold

FBD/AMB Specifications:

Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer (AMB) on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density. Currently, FBD/AMB specification is broken-out into the following specifications:

1. FBD Design Specification: This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FBDs).

2. FBD Architecture and Protocol Specification: This specification covers Overview, Channel Initialization, Channel Protocol, and Reliability, Availability, and Serviceability (RAS) features of FBDIMM architecture.

3. FBD AMB Specification: The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. This specification covers information about various AMB interfaces (Channel/DRAM), Test & Initialization functions, SMBus Interface, Clocking, Registers, etc.

4. FBD High-Speed Differential PTP Link Specification: This specification defines the high-speed differential point-to-point signaling link for FB-DIMM, operating at the buffer supply voltage of 1.5V that is provided at the FBDIMM connector. This specification also applies to FBD host chips which may operate with a different supply voltage. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream.The link utilizes a derived clock approach and transmitter de-emphasis to compensate for channel loss characteristics.

5. FBD SPD Specification: This specification describes the Serial Presence Detect (SPD) values for FBD.

6. FBD DFx Specification: The FB-DIMM DFx spec covers Design for Test (DFT), Design for Manufacturing (DFM) and Design for Validation (DFV) requirements and implementation guidelines for Fully Buffered DIMM technology.

DDR2 240-Pin FB-DIMM Pin List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD}	31	PN3	61	PN9#	91	PS9#	121	V_{DD}	151	SN3	181	SN9#	211	SS9#
2	V_{DD}	32	PN3#	62	V_{SS}	92	V_{SS}	122	V_{DD}	152	SN3#	182	V_{SS}	212	V_{SS}
3	V_{DD}	33	V_{SS}	63	PN10	93	PS5	123	V_{DD}	153	V_{SS}	183	SN10	213	SS5
4	V_{SS}	34	PN4	64	PN10#	94	PS5#	124	V_{SS}	154	SN4	184	SN10#	214	SS5#
5	V_{DD}	35	PN4#	65	V_{SS}	95	V_{SS}	125	V_{DD}	155	SN4#	185	V_{SS}	215	V_{SS}
6	V_{DD}	36	V_{SS}	66	PN11	96	PS6	126	V_{DD}	156	V_{SS}	186	SN11	216	SS6
7	V_{DD}	37	PN5	67	PN11#	97	PS6#	127	V_{DD}	157	SN5	187	SN11#	217	SS6#
8	V_{SS}	38	PN5#	68	V_{SS}	98	V_{SS}	128	V_{SS}	158	SN5#	188	V_{SS}	218	V_{SS}
9	V_{CC}	39	V_{SS}	69	V_{SS}	99	PS7	129	V_{CC}	159	V_{SS}	189	V_{SS}	219	SS7
10	V_{CC}	40	PN13	70	PS0	100	PS7#	130	V_{CC}	160	SN13	190	SS0	220	SS7#
11	V_{SS}	41	PN13#	71	PS0#	101	V_{SS}	131	V_{SS}	161	SN13#	191	SS0#	221	V_{SS}
12	V_{CC}	42	V_{SS}	72	V_{SS}	102	PS8	132	V_{CC}	162	V_{SS}	192	V_{SS}	222	SS8
13	V_{CC}	43	V_{SS}	73	PS1	103	PS8#	133	V_{CC}	163	V_{SS}	193	SS1	223	SS8#
14	V_{SS}	44	RFU	74	PS1#	104	V_{SS}	134	V_{SS}	164	RFU	194	SS1#	224	V_{SS}
15	V_{TT}	45	RFU	75	V_{SS}	105	RFU	135	V_{TT}	165	RFU	195	V_{SS}	225	RFU
16	VID1	46	V_{SS}	76	PS2	106	RFU	136	VID0	166	V_{SS}	196	SS2	226	RFU
17	RESET#	47	V_{SS}	77	PS2#	107	V_{SS}	137	DNU/M_Test	167	V_{SS}	197	SS2#	227	V_{SS}
18	V_{SS}	48	PN12	78	V_{SS}	108	V_{DD}	138	V_{SS}	168	SN12	198	V_{SS}	228	SCK
19	RFU	49	PN12#	79	PS3	109	V_{DD}	139	RFU	169	SN12#	199	SS3	229	SCK#
20	RFU	50	V_{SS}	80	PS3#	110	V_{SS}	140	RFU	170	V_{SS}	200	SS3#	230	V_{SS}
21	V_{SS}	51	PN6	81	V_{SS}	111	V_{DD}	141	V_{SS}	171	SN6	201	V_{SS}	231	V_{DD}
22	PN0	52	PN6#	82	PS4	112	V_{DD}	142	SN0	172	SN6#	202	SS4	232	V_{DD}
23	PN0#	53	V_{SS}	83	PS4#	113	V_{DD}	143	SN0#	173	V_{SS}	203	SS4#	233	V_{DD}
24	V_{SS}	54	PN7	84	V_{SS}	114	V_{SS}	144	V_{SS}	174	SN7	204	V_{SS}	234	V_{SS}
25	PN1	55	PN7#	85	V_{SS}	115	V_{DD}	145	SN1	175	SN7#	205	V_{SS}	235	V_{DD}
26	PN1#	56	V_{SS}	86	RFU	116	V_{DD}	146	SN1#	176	V_{SS}	206	RFU	236	V_{DD}
27	V_{SS}	57	PN8	87	RFU	117	V_{TT}	147	V_{SS}	177	SN8	207	RFU	237	V_{TT}
28	PN2	58	PN8#	88	V_{SS}	118	SA2	148	SN2	178	SN8#	208	V_{SS}	238	V_{DDSPD}
29	PN2#	59	V_{SS}	89	V_{SS}	119	SDA	149	SN2#	179	V_{SS}	209	V_{SS}	239	SA0
30	V_{SS}	60	PN9	90	PS9	120	SCL	150	V_{SS}	180	SN9	210	SS9	240	SA1

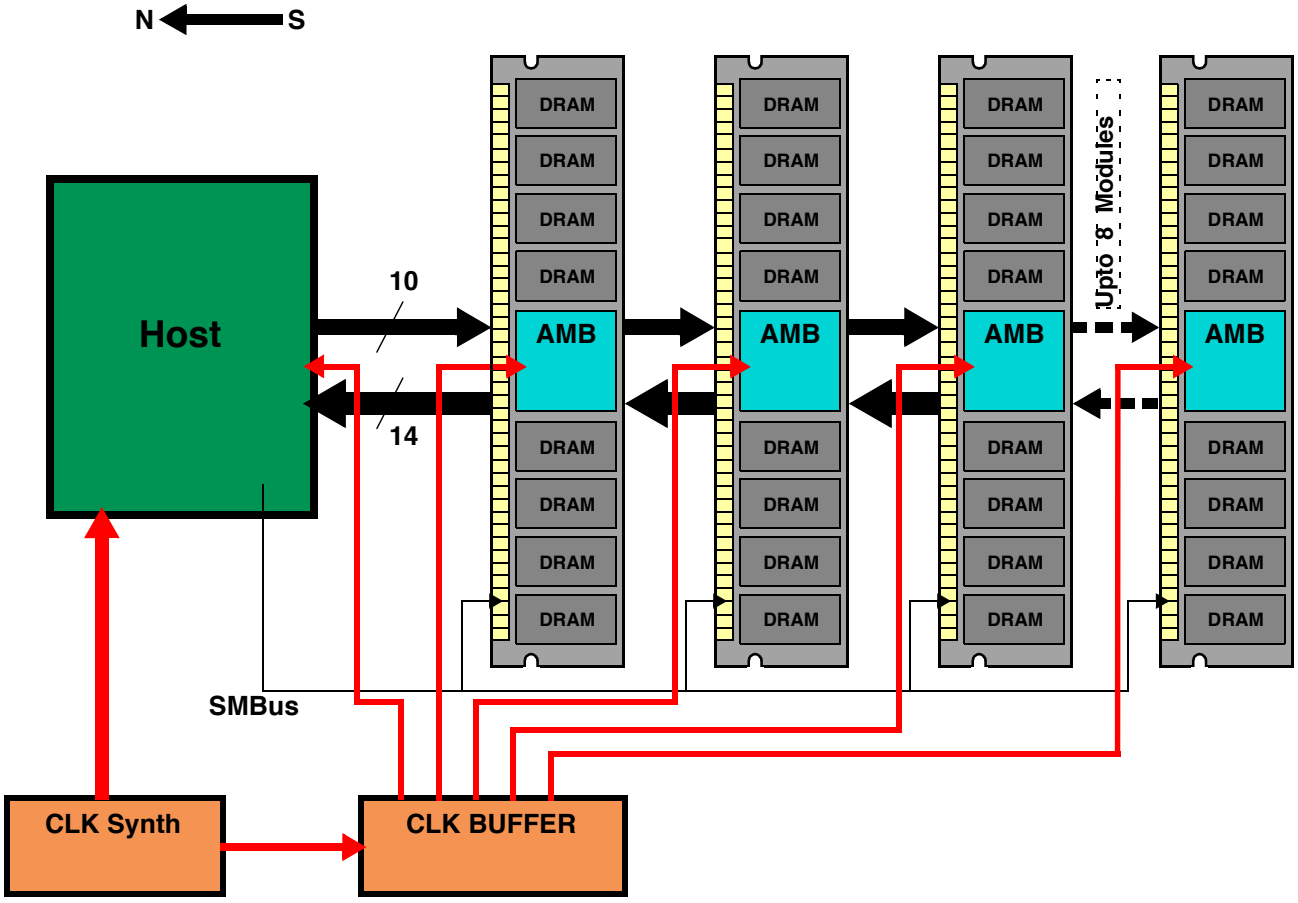
Pin Description:

DIMM Connector Pin Description

Symbol	Type	Polarity	Function
SCK	Input	Positive Edge	Positive line of the differential pair of system clock inputs.
SCK#	Input	Negative Edge	Negative line of the differential pair of system clock inputs.
PN0 ~ PN13	Output	Positive Edge	Primary Northbound Data, positive lines.
PN0# ~ PN13#	Output	Negative Edge	Primary Northbound Data, negative lines.
PS0 ~ PS9	Input	Positive Edge	Primary Southbound Data, positive lines.
PS0# ~ PS9#	Input	Negative Edge	Primary Southbound Data, negative lines.
SN0 ~ SN13	Input	Positive Edge	Secondary Northbound Data, positive lines.
SN0# ~ SN13#	Input	Negative Edge	Secondary Northbound Data, negative lines.
SS0 ~ SS9	Output	Positive Edge	Secondary Southbound Data, positive lines.
SS0# ~ SS9#	Output	Negative Edge	Secondary Southbound Data, negative lines.
SCL	Input/Output	-	Serial Presence Detect (SPD) for Clock Input.
SDA	Input/Output	-	SPD Data Input/Output.
SA0 ~ SA2	Input	-	SPD Address Inputs, also used to select the DIMM number in the AMB.
VID0 ~ VID1	Supply	-	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs. VID0 is V_{DD} value: OPEN = 1.8V, GND = 1.5V; VID1 is V_{CC} value: OPEN = 1.5V, GND = 1.2V;
V_{CC}	Supply	-	AMB Core Power and AMB Channel Interface Power(1.5 Volt).
V_{DD}	Supply	-	DRAM Power and AMB DRAM I/O Power(1.8 Volt).
V_{SS}	Supply	-	Ground.
V_{TT}	Supply	-	DRAM Address/Command/Clock termination Power (V_{DD}/2).
V_{DDSPD}	Supply	-	SPD Power (3.3 Volt).
RESET#	Input	Active Low	Advanced Memory Buffer (AMB) reset signal.
RFU	-	-	Reserved for Future Use.
DNU/M_Test	-	-	The DNU/M_Test pin provides an external connection for testing the margin of V_{REF} which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system.

Note: System Clock Signals (SCK & SCK#) switch at one-half the DRAM CK/CK# frequency.

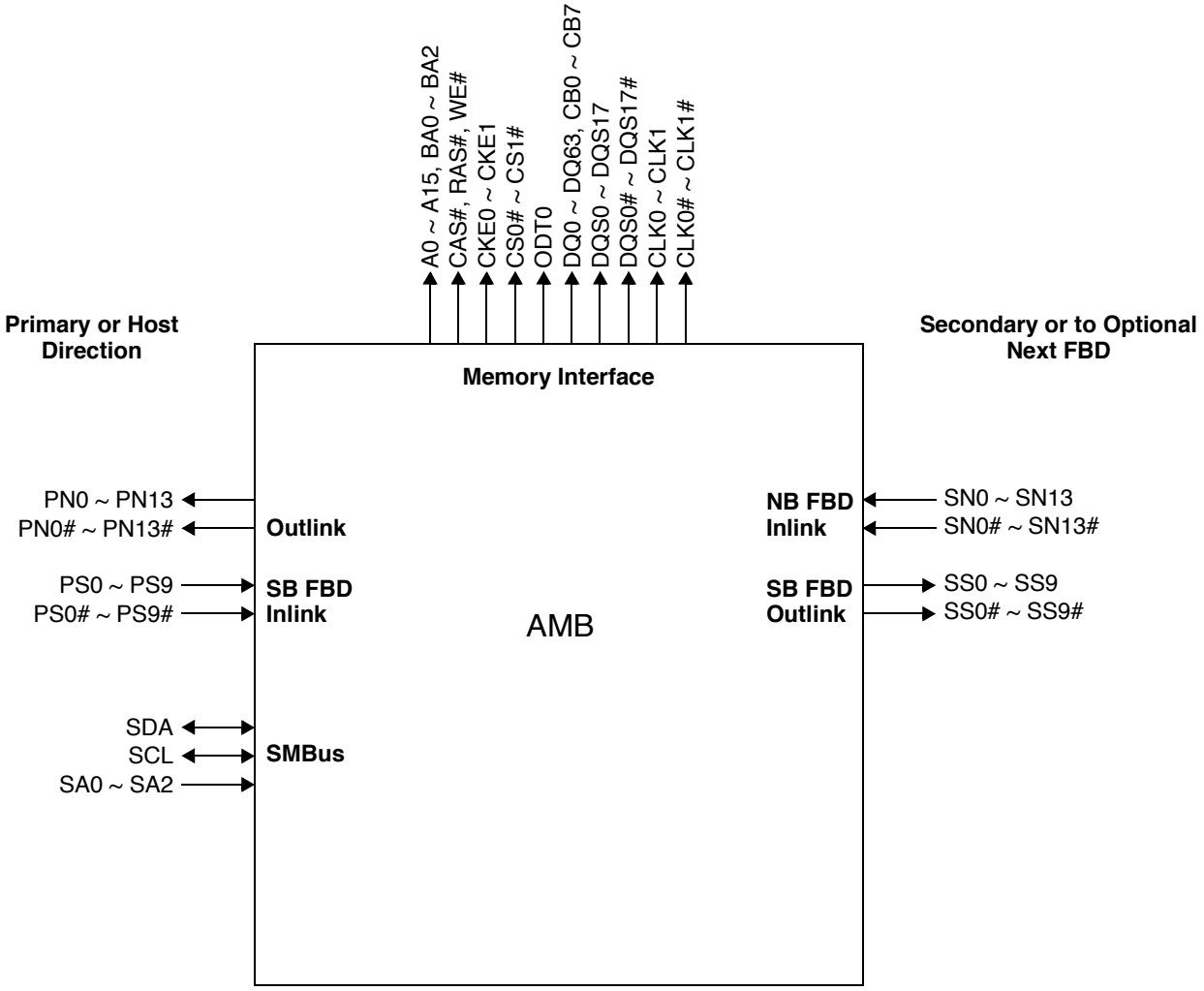
FBD System Block Diagram



The above system block diagram shows a generic example of a clock distribution for a simple single-channel FBD Platform. Also shown are the Northbound/Southbound channels as well as SMBus Interface. “Northbound” refers to the transfer of data towards host Controller. “Southbound” refers to the transfer of data away from the host controller.

An FBD channel can support upto 8 double-rank modules (36 devices each) for a total of 288 devices.

Advanced Memory Buffer - Interface Block Diagram



AMB Pin Description

FBD Channel Signals (Signal Count: 99)

Pin Name	Pin Description	Count
SCK	Positive line of the differential pair of system clock inputs.	1
SCK#	Negative line of the differential pair of system clock inputs.	1
PN0 ~ PN13	Primary Northbound Data, positive lines.	14
PN0# ~ PN13#	Primary Northbound Data, negative lines.	14
PS0 ~ PS9	Primary Southbound Data, positive lines.	10
PS0# ~ PS9#	Primary Southbound Data, negative lines.	10
SN0 ~ SN13	Secondary Northbound Data, positive lines.	14
SN0# ~ SN13#	Secondary Northbound Data, negative lines.	14
SS0 ~ SS9	Secondary Southbound Data, positive lines.	10
SS0# ~ SS9#	Secondary Southbound Data, negative lines.	10
FBDRES	To an external precision calibration resistor connected to V_{CC}.	1

DDR2 Interface Signals (Signal Count: 175)

Pin Name	Pin Description	Count
DQS0 ~ DQS8	Data Strobes, positive lines.	9
DQS0# ~ DQS8#	Data Strobes, negative lines.	9
DQS9 ~ DQS17/ DM0 ~ DM8	Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
DQS9# ~ DQS17#	Data Strobes (x4 DRAM only), negative lines.	9
DQ0 ~ DQ63	Data.	64
CB0 ~ CB7	Checkbits.	8
A0A ~ A15A, A0B ~ A15B	Address.	32
BA0A ~ BA2A, BA0B ~ BA2B	Bank Select Addresses.	6
RASA#, RASB#, CASA#, CASB#, WEA#, WEB#	Command Signals.	6
ODTA, ODTB	On-Die Termination Enable.	2
CKE0A, CKE1A, CKE0B, CKE1B	Clock Enable (One per Rank).	4
CS0A#, CS1A#, CS0B#, CS1B#	Chip Select (One per Rank).	4
CLK0 ~ CLK3	CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
CLK0# ~ CLK3#	Clock, Negative lines.	4

AMB Pin Description (Contd...)

DDR2 Interface Signals (Contd...)

Pin Name	Pin Description	Count
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14.	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14.	1
DDRC_B12	DDR Compensation: Resistor connected to V_{SS}.	1
DDRC_C12	DDR Compensation: Resistor connected to V_{DD}.	1

SPD Bus Interface Signals (Signal Count: 5)

Pin Name	Pin Description	Count
SCL	Serial Presence Detect (SPD) Clock Input.	1
SDA	SPD Data Input/Output.	1
SA0 ~ SA2	SPD Address Inputs, also used to select the DIMM number in the AMB.	3

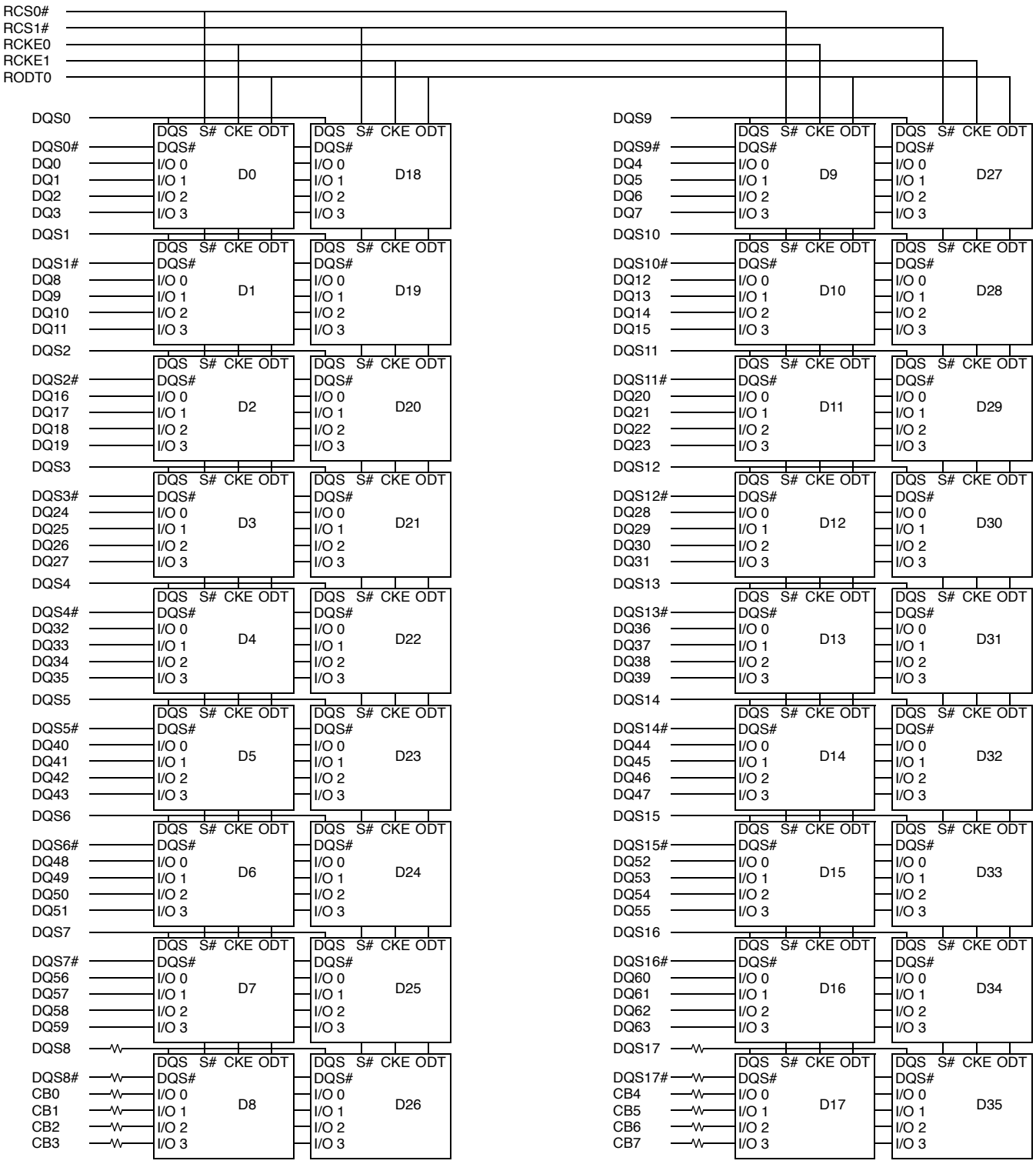
Miscellaneous (Signal Count: 163)

Pin Name	Pin Description	Count
PLLTSTO	PLL Clock Observability Output.	1
V_{CCAPLL}	Analog V_{CC} for the PLL. Tied with low pass filter to V_{CC}.	1
V_{SSAPLL}	Analog V_{SS} for the PLL. Tied to ground on the AMB die. Do not tie to ground on the DIMM.	1
TEST_pin#	Leave floating on the DIMM.	6
TESTLO_pin#	Tie to ground on the DIMM.	5
BFUNC	Tie to ground to set functionality as “buffer on DIMM.”	1
RESET#	AMB Reset Signal.	1
NC	No connect. Many NC are connected to V_{DD} on the DIMM, to lower the impedance of the V_{DD} power islands.	129
RFU	Reserved for Future Use.	18

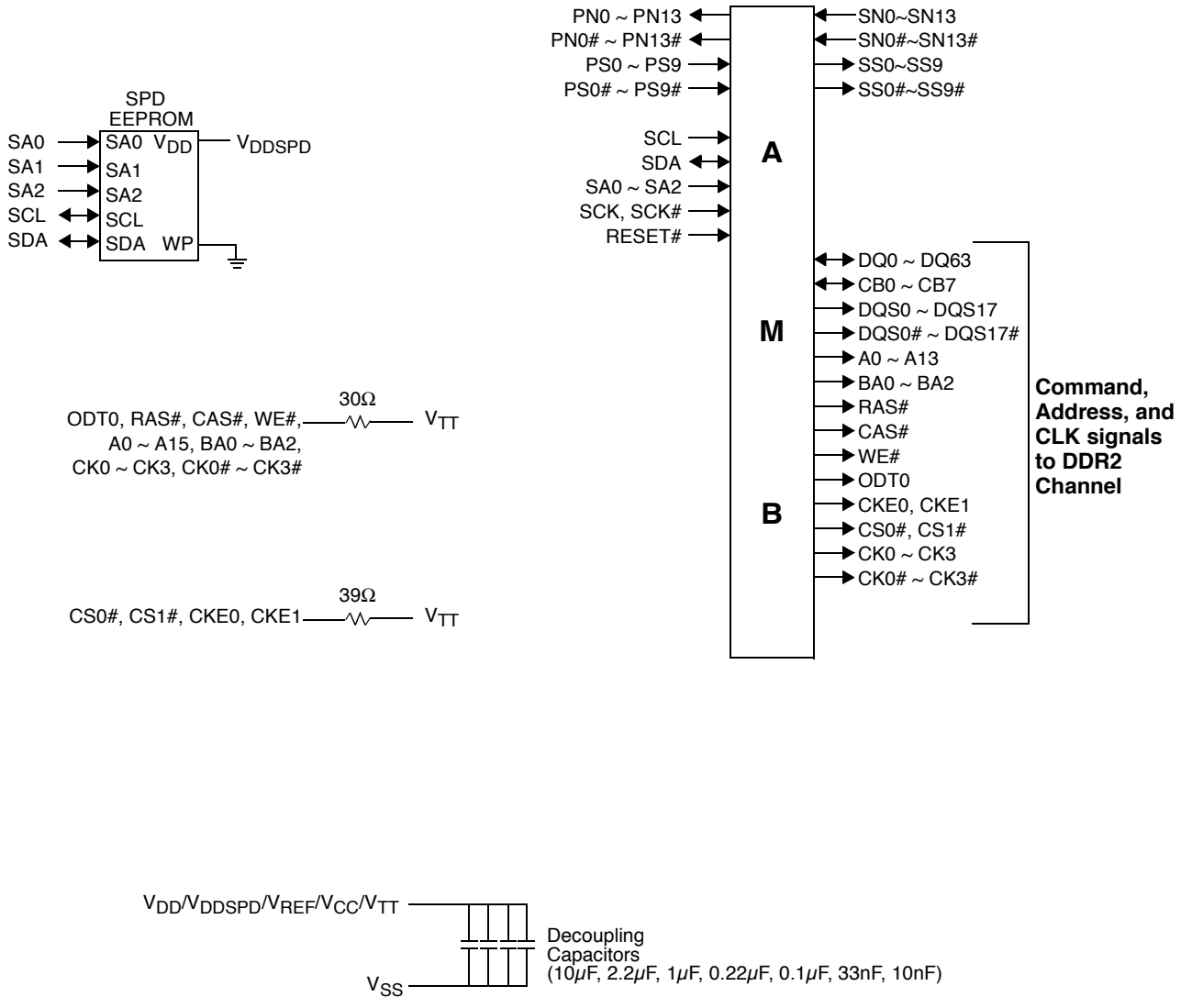
Power/Ground Signals (Signal Count: 213)

Pin Name	Pin Description	Count
V_{CC}	AMB Core Power (1.5 Volt).	24
V_{CCFBD}	AMB Channel I/O Power (1.5 Volt).	8
V_{DD}	AMB DRAM I/O Power (1.8 Volt).	24
V_{DDSPD}	SPD Power (3.3 Volt).	1
V_{SS}	Ground.	156

Block Diagram



Note: Unless otherwise noted, data resistor values are 22Ω ± 5%.

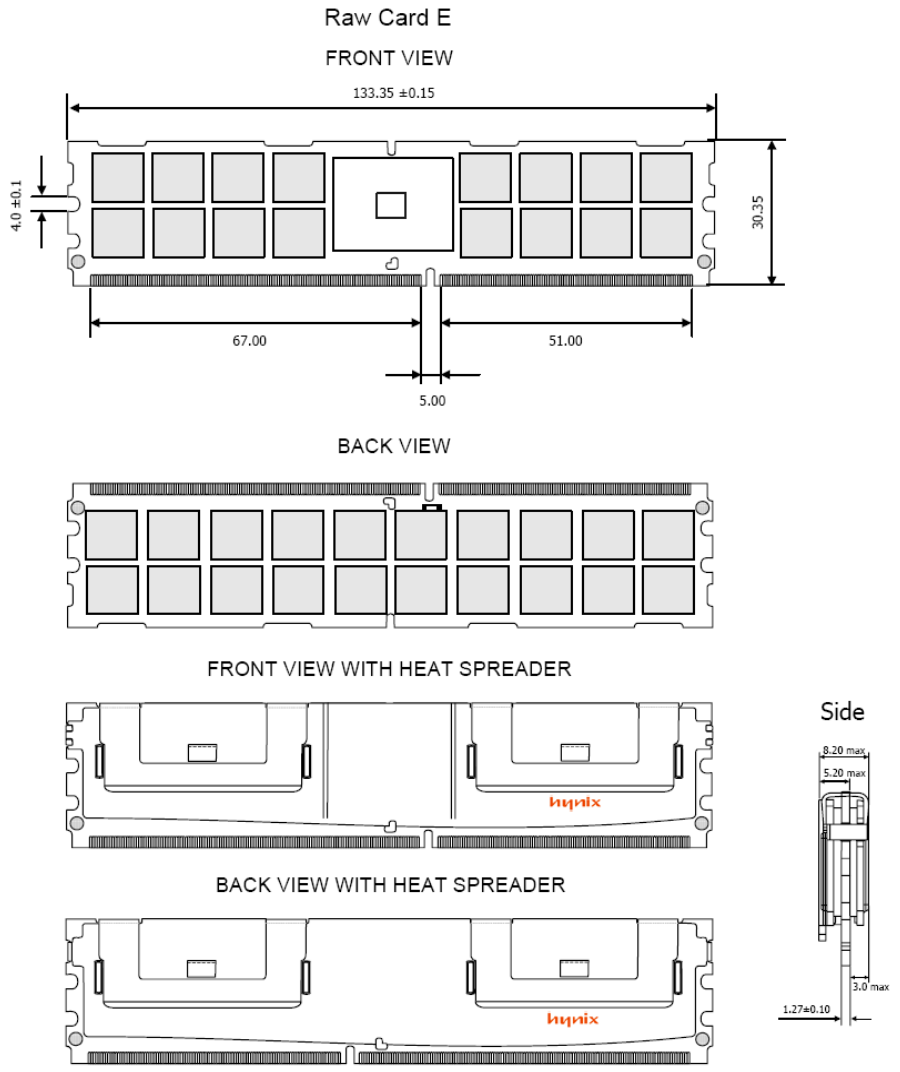


Notes:

1. There are two physical copies of each address/command/control/clock.

Physical Dimensions

240-pin Fully Buffered DIMM



Note 1: All dimensions are typical millimeter scale unless otherwise stated.

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Absolute Maximum Ratings

Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5	2.3	V
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}	-0.3	1.75	V
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.5	2.3	V
V_{TT}	Voltage on V_{TT} relative to V_{SS}	-0.5	2.3	V
T_{STG}	Storage Temperature	-55	100	°C
T_{CASE}	DDR2 SDRAM device operating temperature (Ambient)	0	85	°C
	AMB device operating temperature (Ambient)	0	110	°C

Input DC Voltage and Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Notes
AMB supply voltage	V_{CC}	1.455	1.5	1.575	V	
DDR2 SDRAM supply voltage	V_{DD}	1.7	1.8	1.9	V	
Termination voltage	V_{TT}	$0.49xV_{DD}$-0.04	$0.50xV_{DD}$	$0.51xV_{DD}$+0.04	V	
EEPROM supply Voltage	V_{DDSPD}	3.0	3.3	3.6	V	
SPD Input High (logic 1) voltage	$V_{IH(DC)}$	2.1	-	V_{DDSPD}	V	1
SPD Input Low (logic 0) voltage	$V_{IL(DC)}$	-	-	0.8	V	1
RESET Input High (logic 1) voltage	$V_{IH(DC)}$	1.0	-	-	V	2
RESET Input Low (logic 0) voltage	$V_{IL(DC)}$	-	-	0.5	V	1
Leakage Current (RESET)	I_L	-90	-	90	µA	2
Leakage Current (link)	I_L	-	-	10	µA	3

Notes:

1. Applies for SMB and SPD bus signals.
2. Applies for AMB CMOS signal RESET#.
3. For all other AMB related DC parameters, please refer to the high-speed differential link interface specification.

Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Notes
EI assertion pass-through timing	$t_{EI\ Propogate}$	-	-	4	CK	
EI deassertion pass-through timing	t_{EID}	-	-	Bitlock	CK	2
EI assertion duration	t_{EI}	100	-	-	CK	1,2
FBD command to DDR2 clock out that latches command		7.1	8.1	9.1	ns	3
FBD command to DDR2 WRITE		-	TBD	-	ns	
DDR2 READ to FBD (last FBDIMM)		4.0	5.0	6.0	ns	4
Resample pass-through time		-	1.25	-	ns	
Resynch pass-through time		-	2.25	-	ns	
Bitlock interval	$t_{Bitlock}$	-	-	119	frames	1
Framelock interval	$t_{Framelock}$	-	-	154	frames	1

Notes:
1. Defined in FBDIMM architecture and protocol specification.
2. Clocks defined as core clocks - 2x SCK input.
3. For DDR2-667 (PC2-5300), this is measured from the beginning of the frame at the southbound input to the DDR2 clock output that latches the first command of a frame to the DDR2 SDRAM devices.
4. For DDR2-667 (PC2-5300), this is measured from the latest DQS input to the AMB to the start of the matching data frame at the northbound FBDIMM outputs.

Assumptions for all Parameters:

Primary channel drive strength at 100 percent with de-emphasis at -6.5dB, secondary channel drive strength at 60 percent with de-emphasis at -3dB when enabled.

Address and data fields are psuedo-random, which provides a 50 percent toggle rate on DDR2 SDRAM data lines and link lanes when data is being transferred.

Assuming 1 ACTIVATE command and 1 READ/WRITE command per BL transfer, BL = 4.

10 southbound lanes and 14 northbound lanes are enabled and active.

SPD-specific assumptions:
- Number of devices on the specific FBDIMM assumed.
- Termination of command, address, and control is actual value used on the FBDIMM.
- ECC as per the specific FBDIMM.
- SPD specifies Delta T.

AMB power spec specific assumptions:
- Specific ECC FBDIMM assumed (72 bit data, 14 lanes northbound with DDR2 SDRAMs as defined in the configuration options of this datasheet.
- Modeled with 27Ω termination for command, address, and clocks, and 47Ω termination for control.
- AMB specification describes current for each rail.

DDR2 I_{DD} Specifications and Conditions

Symbol	Parameter/Condition	Power Supply	DDR2-667	Units
$I_{CC\_IDLE\_0}$	**Idle current, single or last FBDIMM:** L0 state, idle (0 BW); primary channel enabled, secondary channel disabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	1.5V	TBD	A
$I_{DD\_IDLE\_0}$		1.8V	TBD	A
	Total Power		TBD	W
$I_{CC\_IDLE\_1}$	**Idle current, first FBDIMM:** L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	1.5V	TBD	A
$I_{DD\_IDLE\_1}$		1.8V	TBD	A
	Total Power		TBD	W
$I_{CC\_IDLE\_2}$	**Idle current, DDR2 SDRAM power down:** L0 state, idle (0 BW); primary and secondary channels enabled, CKE low; command and address lines floated, DDR2 SDRAM clock active; ODT and CKE driven LOW.	1.5V	TBD	A
$I_{DD\_IDLE\_2}$		1.8V	TBD	A
	Total Power		TBD	W
$I_{CC\_ACTIVE\_1}$	**Active Power:** L0 state; 50% DDR2 SDRAM BW, 67% READ, 33% WRITE; primary and secondary channels enabled, CKE high; DDR2 SDRAM clock active.	1.5V	TBD	A
$I_{DD\_ACTIVE\_1}$		1.8V	TBD	A
	Total Power		TBD	W
$I_{CC\_ACTIVE\_2}$	**Active Power, data pass through:** L0 state; 50% DDR2 SDRAM BW to downstream FBDIMM, 67% READ, 33% WRITE; primary and secondary channels enabled; command and address lines stable, CKE high; DDR2 SDRAM clock active.	1.5V	TBD	A
$I_{DD\_ACTIVE\_2}$		1.8V	TBD	A
	Total Power		TBD	W
I_{CC_L0s}	**Channel standby:** Average power over 42 frames where the channel enters and exits L0s; DDR2 SDRAM devices idle (0 BW); CKE low; command and address lines floated; DDR2 SDRAM clock active, ODT and CKE driven LOW.	1.5V	TBD	A
I_{DD_L0s}		1.8V	TBD	A
	Total Power		TBD	W
$I_{CC\_TRAINING}$	**Training:** Primary and secondary channels enabled; 100% toggle on all channel lanes; DDR2 SDRAM devices idle (0 BW); CKE high, command and address lines stable; DDR2 SDRAM clock active.	1.5V	TBD	A
$I_{DD\_TRAINING}$		1.8V	TBD	A
	Total Power		TBD	W

Notes:

1. $V_{CC(max)}$ = 1.575V; $V_{DD(max)}$ = 1.9V.
2. Total Power = I_{CC} x $V_{CC(max)}$ + I_{DD} x $V_{DD(max)}$.
3. FBDIMM Power was calculated on the basis of DRAM and AMB Values in the datasheet.

V_{TT} Currents

Description	Symbol	Typ	Max	Units
Idle current, DDR2 SDRAM device power down	I_{TT1}	500	700	mA
Active power, 50% DDR2 SDRAM BW	I_{TT2}	500	700	mA

Reference Clock Input Specifications

Parameter	Symbol	Min	Max	Units	Notes
Reference clock frequency	f_{SCK}	133.33	200	MHz	1, 2
Rise time, fall time	$T_{SCK-RISE}$, $T_{SCK-FALL}$	175	700	ps	3
Voltage high	$V_{SCK-HIGH}$	660	850	mV	
Voltage low	$V_{SCK-LOW}$	-150	-	mV	
Absolute crossing point	$V_{CROSS-ABS}$	250	550	mV	4
Relative crossing point	$V_{CROSS-REL}$	calculated	calculated		5
Percentage mismatch between rise and fall times	$T_{SCK-RISE-FALL-MATCH}$	-	10	%	
Duty cycle of reference clock	$T_{SCK-DUTYCYCLE}$	40	60	%	
Clock leakage current	I_{I-CK}	-10	10	μA	6, 7
Clock leakage capacitance	C_{I-CK}	0.5	2	pF	7
Clock leakage capacitance delta	$C_{I-CK(D)}$	-0.25	0.25	pF	8
Transport delay	T1	-	5	ns	9, 10
Phase jitter sample size	NSAMPLE	10^{16}		Periods	11
Reference clock jitter, filtered	$T_{REF-JITTER}$	-	40	ps	12, 13
Reference clock deterministic jitter	T_{REF-DJ}	-	TBD	ps	

Notes:

1. 133MHz for PC2-4200 and 166MHz for PC2-5300.
2. Measured with SSC Disabled.
3. Measured differentially through the range of 0.175V to 0.525V.
4. The crossing point must meet the absolute and relative crossing point specification simultaneously.
5. $V_{CROSS\_REL\_(MIN)}$ and $V_{CROSS\_REL\_(MAX)}$ are derived using the following calculation: Min = $0.5(V_{havg} - 0.710) + 0.250$; and Max = $0.5(V_{havg} - 0.710) + 0.550$, where V_{havg} is the average of $V_{SCK-HIGHM}$.
6. Measured with a single-ended input voltage of 1V.
7. Applies to reference clocks SCK and SCK#.
8. Difference between SCK and SCK# input.
9. T1 = ITdata path - TclockpathI (excluding PLL loop delays). This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter $T_{REF-JITTER}$.
10. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to the data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time of flight of interpolators or other clock adjustments mechanisms. They do not include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
11. Direct measurement of phase jitter records over 10^{16} periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at 10^{16} samples extrapolated from an estimate of the sigma of the random jitter components.
12. Measured wuth SSC enabled on reference clock generator.
13. As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRXTotal-MIN parameters.

Differential Transmitter Output Specifications

Parameter	Symbol	Values		Units	Comments
		Min	Max		
Differential peak-to-peak output voltage for large voltage swing	$V_{TX-DIFFp-p\_L}$	900	1300	mV	EQ 1, Note1
Differential peak-to-peak output voltage for regular voltage swing	$V_{TX-DIFFp-p\_R}$	800	-	mV	EQ 1, Note1
Differential peak-to-peak output voltage for small voltage swing	$V_{TX-DIFFp-p\_S}$	520	-	mV	EQ 1, Note1
DC common code output voltage for large voltage swing	V_{TX-CM_L}	-	375	mV	EQ 2, Note1
DC common code output voltage for small voltage swing	V_{TX-CM_S}	135	280	mV	EQ 2, Note 1, 2
De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	$V_{TX-DE-3.5-Ratio}$	-3.0	-4.0	dB	1, 3, 4
De-emphasized differential output voltage ratio for -6.0 dB de-emphasis	$V_{TX-DE-6.0-Ratio}$	-5.0	-7.0	dB	1, 2, 3
AC peak-to-peak common mode output voltage for large swing	$V_{TX-CM-ACp-p\_L}$	-	90	mV	EQ 7, Note 1, 5
AC peak-to-peak common mode output voltage for regular swing	$V_{TX-CM-ACp-p\_R}$	-	80	mV	EQ 7, Note 1, 5
AC peak-to-peak common mode output voltage for small swing	$V_{TX-CM-ACp-p\_S}$	-	70	mV	EQ 7, Note 1, 5
Maximum single ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE}$	-	50	mV	6
Maximum single ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE-DC}$	-	20	mV	6
Maximum peak-to-peak differential voltage in EI condition	$V_{TX-IDLE-DIFFp-p}$	-	40	mV	
Single-ended voltage (w.r.t V_{SS}) on D+/D-	V_{TX-SE}	-75	750	mV	1, 7
Minimum TX eye width, 3.2 and 4.0 Gb/s	$T_{TX-EYE-MIN}$	0.7	-	UI	1, 8
Minimum TX eye width, 4.8 Gb/s	$T_{TX-EYE-MIN4.8}$	TBD	-	UI	1, 8
Maximum TX deterministic jitter, 3.2 and 4.0 Gb/s	$T_{TX-DJ-DD}$	-	0.2	UI	1, 8, 9
Maximum TX deterministic jitter, 4.8 Gb/s	$T_{TX-DJ-DD4.8}$	-	TBD	UI	1, 8, 9
Instantaneous pulse width	$T_{TX-PULSE}$	0.85	-	UI	10

Differential Transmitter Output Specifications (Contd.)

Parameter	Symbol	Values		Units	Comments
		Min	Max		
Differential TX output rise/fall time	$T_{TX-RISE}$ $T_{TX-FALL}$	30	90	ps	20-80% voltage, Note 1
Mismatch between rise and fall times	$T_{TX-RF-MISMATCH}$	-	20	ps	
Differential return loss	$RL_{TX-DIFF}$	8	-	dB	1GHz-2.4GHz, Note 11
Common mode return loss	RL_{TX-CM}	6	-	dB	1GHz-2.4GHz, Note 11
Transmitter termination impender	RL_{TX}	41	55		12
D+/D- TX Impedance difference	$RL_{TX-MATCH-DC}$	-	4	%	EQ 4, Boundaries are applied seperately to high and low output voltage states
Lane-to lane skew at TX	$L_{TX-SKEW1}$	-	100+3UI	ps	13, 15
Lane-to lane skew at TX	$L_{TX-SKEW2}$	-	100+2UI	ps	14, 15
Maximum TX Drift (resync mode)	$T_{TX-DRIFT-RESYNC}$	-	240	ps	16
Maximum TX Drift (resample mode only)	$T_{TX-DRIFT-RESAMPLE}$	-	120	ps	16
Bit Error Ratio	BER	10^{-12}	-		17

Notes:

1. Specified at the packaged pins into a timing and voltage compliance test load. Common mode measurements to be performed using a 101010 pattern.
2. The transmitter design should not artificially elevate the common mode in order to meet this specification.
3. This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit aftre a transition.
4. De-emphasis shall be disabled in the calibration state.
5. Includes all sources of AC common mode noise.
6. Single ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.
7. The maximum value is specified to be at least $(V_{TX\text{-}DIFFp\text{-}p\_L}/4) + V_{TX\text{-}CM\_L} + (V_{TX\text{-}CM\text{-}ACp\text{-}p}/2)$.
8. This number does not include the effects of SSC or reference clock jitter.
9. Defined as expected maximum jitter for the given probability as measured in the system (TJ), less the unbounded jitter.
10. Pulse width measure at 0V differential.
11. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
12. The termination of small signal resistance; tolerance across voltages from 100mV to 400mV shall not exceed +/-5W with regard to the average of the values measured at 100mV and 400mV for that pin.
13. Lane to Lane skew at the Transmitter pins for an end component.
14. Lane to Lane skew at the Transmitter pins for an intermediate component (assuming zero Lane to Lane skew at the Receiver pins of the incoming PORT).
15. This is static skew. An FBDIMM component is not allowed to change its lane to lane phase relationship after initialization.
16. Measured form the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperture ranges for a single component. Drift rate change is significantly below the tracking capability of the receiver.
17. BER per differential lane.

$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \left| V_{TX\text{-}D+} - V_{TX\text{-}D-} \right|$ (EQ1)

$V_{TX\text{-}CM} = DC_{(avg)}$ of $(\left| V_{TX\text{-}D+} + V_{TX\text{-}D-} \right| /2)$ (EQ2)

$V_{TX\text{-}CM\text{-}AC} = ((\text{Max} \left| V_{TX\text{-}D+} + V_{TX\text{-}D-} \right|)/2) - ((\text{Min} \left| V_{TX\text{-}D+} + V_{TX\text{-}D-} \right|)/2)$ (EQ3)

$R_{TX\text{-}MATCH\text{-}DC} = 2 \times ((\left| R_{TX\text{-}D+} - R_{TX\text{-}D-} \right|) / (\left| R_{TX\text{-}D+} + R_{TX\text{-}D-} \right|))$ (EQ4)

Differential Receiver Input Specifications

Parameter	Symbol	Values		Units	Comments
		Min	Max		
Differential peak-to-peak input voltage for large voltage swing	$V_{RX-DIFFp-p}$	170	TBD	mV	EQ 7, Note 1, 5
Maximum single ended voltage in EI condition	$V_{RX-IDLE-SE}$	-	75	mV	EQ 7, Note 1, 5
Maximum single ended voltage in EI condition (DC only)	$V_{RX-IDLE-SE-DC}$	-	50	mV	EQ 7, Note 1, 5
Maximum peak-to-peak diffenrential voltage in EI condition	$V_{RX-IDLE-DIFFp-p}$	-	65	mV	6
Single ended voltage (w.r.t V_{SS}) on D+/D-	V_{RX-SE}	-300	900	mV	6
Single-pulse peak differential input voltage	$V_{RX-DIFF-PULSE}$	85	-	mV	
Amplitude ratio between adjacent symbols	$V_{RX-DIFF-ADJ-RATIO}$	-	TBD		1, 7
Maximum RX inherent timing error, 3.2 and 4.0 Gb/s	$T_{RX-TJ-MAX}$	-	0.4	UI	1, 8
Maximum RX inherent deterministic timing error, 3.2 and 4.8 Gb/s	$T_{RX-TJ-MAX4.8}$	-	TBD	UI	1, 8
Single pulse width at zero-voltage crossing	$V_{RX-DJ-DD}$	-	0.3	UI	1, 8, 9
Single pulse width at minimum-level crossing	$V_{RX-DJ-DD4.8}$	-	TBD	UI	1, 8, 9
Differential RX input rise/fall time	$T_{RX-PW-ZC}$	0.55	-	UI	20-80% voltage, Note 1
Common mode of the input voltage	$T_{RX-PW-ML}$	0.2	-	UI	
Differential RX output rise/fall time	$T_{RX-RISE}$ $T_{RX-FALL}$	50	-	ps	1GHz-2.4GHz, Note 11
Common mode of the input voltage	V_{RX-CM}	120	400	mV	1GHz-2.4GHz, Note 11
AC peak-to-peak common mode of the input voltage	$V_{RX-CM-ACp-p}$	-	270	mV	12
Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$	$V_{RX-CM-EH-RATOP}$	-	45	%	EQ 4, Boundaries are applied seperately to high and low output voltage states

Differential Receiever Input Specifications

Parameter	Symbol	Values		Units	Comments
		Min	Max		
Differential return loss	$RL_{RX-DIFF}$	9	-	dB	13, 15
Common mode return loss	RL_{RX-CM}	6	-	dB	14, 15
RX termination impedance	R_{RX}	41	55	%	EQ 4, Boundaries are applied seperately to high and low output voltage states
D+/D- RX Impedance difference	$R_{RX-MATCH-DC}$	-	4	%	13, 15
Lane-to lane PCB skew at RX	$L_{RX-PCB-SKEW}$	-	6	UI	14, 15
Minimum RX drift tolerance	$T_{RX-DRIFT}$	400	-	ps	EQ 1, Note1
Minimum data tracking 3dB bandwidth	F_{TRK}	0.2	-	MHz	EQ 1, Note1
Electrical idle entry detect time	$T_{EI-ENTRY-DETECT}$	-	60	ns	EQ 1, Note1
Electrical idle exit detect time	$T_{EI-EXIT-DETECT}$	-	30	ns	EQ 2, Note1
Bit Error Ratio	BER	-	10^{-12}		EQ 2, Note1

Notes:

1. Specified at the package pins into a timing and voltage compliant test setup. Note that the signal levels at the pad will be lower than that at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst case margins are determined for the case with transmitter using small voltage swing.
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
4. Specified at the package pins into a timing and voltage compliant test setup.
5. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask.
6. The relative amplitude ratio limit between adjacent symbols prevents excessive intersymbol interference in the RX. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
7. This number does not include the effects of the SSC or reference clock jitter.
8. This number includes setup and hold of the RX sampling flop.
9. Defined as the dual-dirac deterministic timing error.
10. Allows for 15mV DC offset between transmit and receive devices.
11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if $V_{RX\_DIFFp\text{-}p}$ is 200mV, the maximum AC peak-to-peak common mode is lesser of (200mV *0.45 = 90mV) and $V_{RX\text{-}CM\text{-}AC\text{-}p\text{-}p}$.
12. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
13. The termination small signal resistance tolerance across voltages from 100mV to 400mV shall not exceed +/- 5W with regard to the average of the values measured at 100mV and 400mV for that pin.
14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMD specification.
15. Mesured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of the change is signicantly below the tracking capability of the receiver.
16. This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI.
17. The specified time includes the time required to forward the EI entry condition.
18. BER per differential lane.

$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \left| V_{RX\text{-}D+} - V_{RX\text{-}D-} \right|$ (EQ5)

$V_{RX\text{-}CM} = DC_{(avg)}$ of $(\left| V_{RX\text{-}D+} + V_{RX\text{-}D-} \right| /2)$ (EQ6)

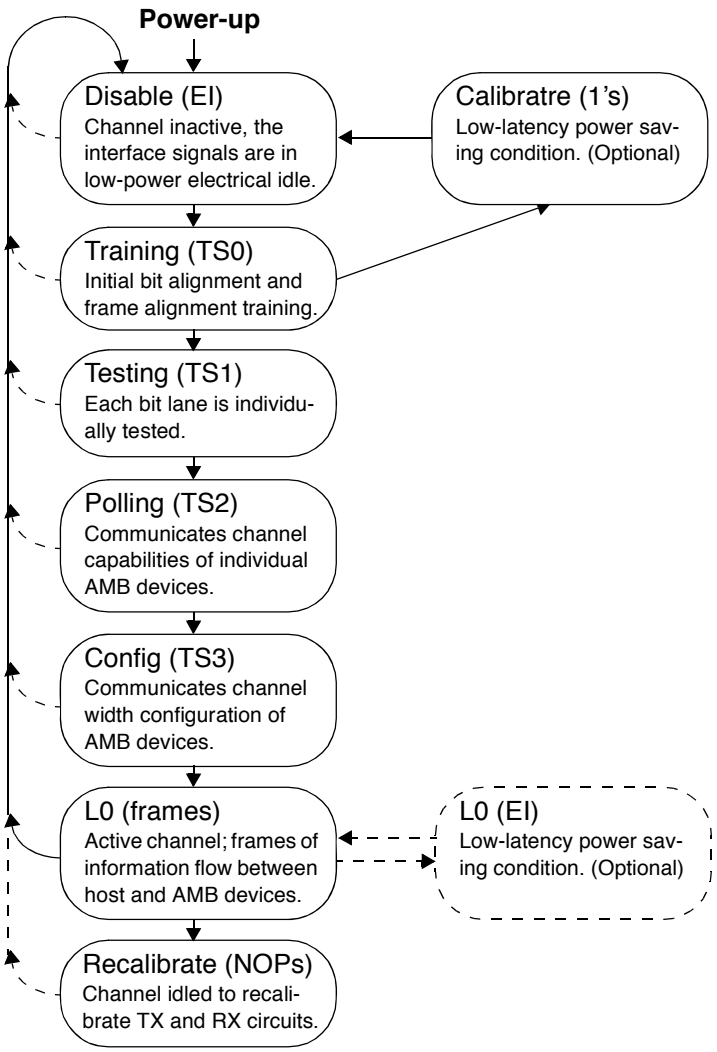
$V_{RX\text{-}CM\text{-}AC} = ((\text{Max} \left| V_{RX\text{-}D+} + V_{RX\text{-}D-} \right|)/2) - ((\text{Min} \left| V_{RX\text{-}D+} + V_{RX\text{-}D-} \right|)/2)$ (EQ7)

$R_{RX\text{-}MATCH\text{-}DC} = 2 \times ((\left| R_{RX\text{-}D+} - R_{RX\text{-}D-} \right|) / (\left| R_{RX\text{-}D+} + R_{RX\text{-}D-} \right|))$ (EQ8)

AMB Initialization

The FBD initialization process generally follows the top-to-bottom sequence of the state transitions shown in the the high level AMB Initialization Flow diagram. The host must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state. The value in paranthesis in each state bubble indicates the condition/activity of the links during these states.

AMB Initialization Flow Diagram



Each bit lane is initialized (mostly) independently to support fault tolerance. The transitions in the AMB Initialization Flow Diagram represent the transitions of the AMB core logic state machine and are taken when the transition event is detected on the minimum required number of southbound bit lanes. The chain of FBDIMM links connecting the host to the AMBs must each be initialized to establish the timing for broadcasting data frames in the southbound direction and for merging data frames in the northbound direction. The AMBs on the channel are generally initiaized as a group but because each AMB is individually addressable many alternate initialization sequences may be employed.

Part Number Decode

S	G	512	7	FBD2	256	5	2	H	C	D
1	2	3	4	5	6	7	8	9	10	11

1 **SMART Modular Technologies**

2 **Module Process Technology**
G: Green Module (RoHS Compliant)

3 **Module Address Depth**
512: 512M

4 **Module Data Bus Width**
7: x72

5 **Module Configuration**
FBD2: DDR2 240-pin Fully Buffered DIMM

6 **Device Depth**
256: 256Mx4

7 **CAS Latency**
5: CL 5.0

8 **Module Speed**
2: DDR2-667

9 **Device Vendor**
H: Hynix

10 **Device Revision**
C: Revision C

10 **AMB Vendor & Revision**
D: IDT AMB Revision C1

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