

ULTRA MOBILE PC/MOBILE INTERNET DEVICE

ICS9UMS9633B

Recommended Application:

Poulsbo Based Ultra-Mobile PC (UMPC)

Output Features:

- 3 CPU low power differential push-pull pairss
- 3 SRC low power differential push-pull pairs
- 1 LCD100 SSCD low power differential push-pull pair
- 1 DOT96 low power differential push-pull pair
- 1 REF, 14.31818MHz, 3.3V SE output

Features/Benefits:

- Supports Dothan ULV CPUs with 67 to 167 MHz CPU outputs
- Dedicated TEST/SEL and TEST/MODE pins saves isolation resistors on pins
- CPU STOP# input for power manangment
- Fully integrated Vreg
- Integrated series resistors on differential outputs
- 1.5V VDD IO operation, 3.3V VDD core and REF supply pin for REF
- Industrial Temperature (-40 to +85C) version available

SSOP Pin Configuration

48 SSOP Package

^{*} indicates inputs with internal pull up of ~10Kohm to 3.3V

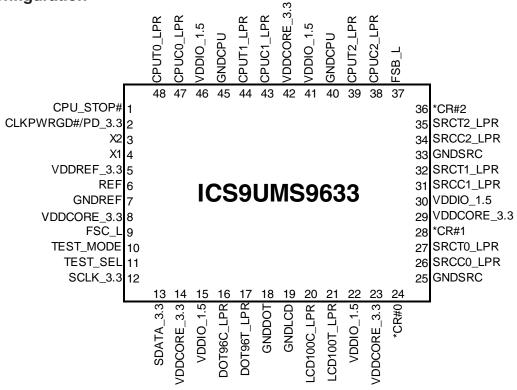
SSOP Pin Description

PIN#	PIN NAME	TYPE	DESCRIPTION
1	REF	OUT	14.318 MHz reference clock.
2	GNDREF	PWR	Ground pin for the REF outputs.
3	VDDCORE_3.3	PWR	3.3V power for the PLL core
4	FSC_L	IN	Low threshold input for CPU frequency selection. Refer to input electrical
4	1 30_L	IIN	characteristics for Vil_FS and Vih_FS values.
5	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode
	TEST_INIODE	111	while in test mode. Refer to Test Clarification Table.
			TEST_SEL: latched input to select TEST MODE
6	TEST_SEL	IN	1 = All outputs are tri-stated for test
			0 = All outputs behave normally.
7	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
8	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
	VDDCORE_3.3	PWR	3.3V power for the PLL core
10	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
11	11 DOT96C_LPR		Complement clock of low power differential pair for 96.00MHz DOT clock. No 50ohm
			resistor to GND needed. No Rs needed.
12	12 DOT96T_LPR		True clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor
12			to GND needed. No Rs needed.
13	GNDDOT	PWR	Ground pin for DOT clock output
14	GNDLCD	PWR	Ground pin for LCD clock output
15	LCD100C_LPR	OUT	Complement clock of low power differential pair for LCD100 SS clock. No 50ohm
	LOD TOOO_LI TI		resistor to GND needed. No Rs needed.
16	LCD100T_LPR	OUT	True clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to
			GND needed. No Rs needed.
	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
	VDDCORE_3.3	PWR	3.3V power for the PLL core
19	*CR#0	IN	Clock request for SRC0, 0 = enable, 1 = disable
20	GNDSRC	PWR	Ground pin for the SRC outputs
21	SRCC0_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm
21	611000_Ei 11	001	series resistor. No 50ohm resistor to GND needed.
22	SRCT0_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series
		501	resistor. No 50ohm resistor to GND needed.
23	*CR#1	IN	Clock request for SRC1, 0 = enable, 1 = disable
24	VDDCORE_3.3	PWR	3.3V power for the PLL core

SSOP Pin Description (continued)

PIN#	PIN NAME	TYPE	DESCRIPTION
25	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
26	SRCC1_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm
20	SHOOT_LF H	001	series resistor. No 50ohm resistor to GND needed.
27	SRCT1_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series
21	SHOTT_ELT	001	resistor. No 50ohm resistor to GND needed.
28	GNDSRC	PWR	Ground pin for the SRC outputs
29	SRCC2_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm
23	SHOOZ_EFT	001	series resistor. No 50ohm resistor to GND needed.
30	SRCT2_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series
- 50	OHOTZ_LITT	001	resistor. No 50ohm resistor to GND needed.
31	*CR#2	IN	Clock request for SRC2, 0 = enable, 1 = disable
32	FSB_L	IN	Low threshold input for CPU frequency selection. Refer to input electrical
- 52	1 0B_E	111	characteristics for Vil_FS and Vih_FS values.
33	CPUC2_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated
- 55	OI OOZ_LI II	001	33ohm series resistor. No 50 ohm resistor to GND needed.
34	CPUT2_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm
34	OI OIZ_EI II	001	series resistor. No 50 ohm resistor to GND needed.
35	GNDCPU	PWR	Ground pin for the CPU outputs
36	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
37	VDDCORE_3.3	PWR	3.3V power for the PLL core
38	CPUC1_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated
36	CFUCI_LFN	0	33ohm series resistor. No 50 ohm resistor to GND needed.
39	CPUT1_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm
39	CPUTI_LPN	0	series resistor. No 50 ohm resistor to GND needed.
40	GNDCPU	PWR	Ground pin for the CPU outputs
41	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
42	CPUC0_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated
42	CPUCU_LPR	001	33ohm series resistor. No 50 ohm resistor to GND needed.
40	CDUTA LDD	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm
43	CPUT0_LPR	001	series resistor. No 50 ohm resistor to GND needed.
44	CPU_STOP#	IN	Stops all CPU clocks, except those set to be free running clocks
15	CLKBWBCD#/BD 3 3	INI	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs
45	CLKPWRGD#/PD_3.3	IN	are valid and are ready to be sampled. This is an active low input. / Asynchronous
			active high input pin used to place the device into a power down state.
46	X2	OUT	Crystal output, Nominally 14.318MHz
47	X1	IN	Crystal input, Nominally 14.318MHz.
48	VDDREF_3.3	PWR	Power pin for the XTAL and REF clocks, nominal 3.3V

MLF Pin Configuration



48-pin MLF, 6x6 mm, 0.4mm pitch

^{*} indicates inputs with internal pull up of ~10Kohm to 3.3V

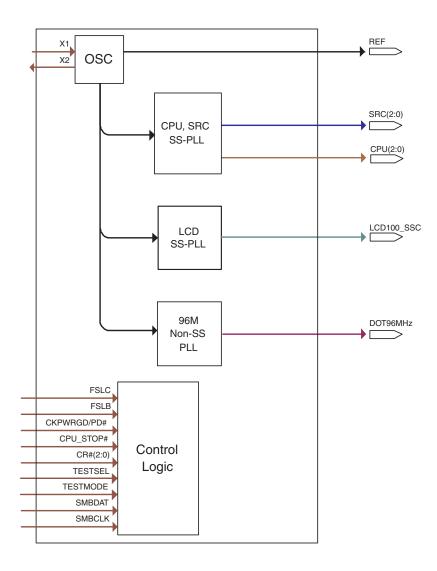
MLF Pin Description

PIN#	PIN NAME	TYPE	DESCRIPTION
1	CPU_STOP#	IN	Stops all CPU clocks, except those set to be free running clocks
2	CLKPWRGD#/PD_3.3	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input. / Asynchronous active high input pin used to place the device into a power down state.
3	X2	OUT	Crystal output, Nominally 14.318MHz
4	X1	IN	Crystal input, Nominally 14.318MHz.
5	VDDREF_3.3	PWR	Power pin for the XTAL and REF clocks, nominal 3.3V
6	REF	OUT	14.318 MHz reference clock.
7	GNDREF	PWR	Ground pin for the REF outputs.
8	VDDCORE_3.3	PWR	3.3V power for the PLL core
9	FSC_L	IN	Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
10	TEST_MODE	IN	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
11	TEST_SEL	IN	TEST_SEL: latched input to select TEST MODE 1 = All outputs are tri-stated for test 0 = All outputs behave normally.
12	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
13	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
14	VDDCORE_3.3	PWR	3.3V power for the PLL core
15	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
16	DOT96C_LPR	OUT	Complement clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed.
17	DOT96T_LPR	OUT	True clock of low power differential pair for 96.00MHz DOT clock. No 50ohm resistor to GND needed. No Rs needed.
18	GNDDOT	PWR	Ground pin for DOT clock output
19	GNDLCD	PWR	Ground pin for LCD clock output
20	LCD100C_LPR	OUT	Complement clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed.
21	LCD100T_LPR	OUT	True clock of low power differential pair for LCD100 SS clock. No 50ohm resistor to GND needed. No Rs needed.
22	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
23	VDDCORE_3.3	PWR	3.3V power for the PLL core
24	*CR#0	IN	Clock request for SRC0, 0 = enable, 1 = disable
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MLF Pin Description (continued)

SRCT0_LPR OUT Series resistor. No 500hm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RCR#1 IN Clock request for SRC1, 0 = enable, 1 = disable 29 VDDCORE_3.3 PWR 3.3V power for the PLL core OUT Complementary clock of differential outputs, nominal 1.5V. Complementary clock of differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC1_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC outputs SRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC outputs SRCC2_LPR OUT Ground pin for the SRC outputs SRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the CPU output selection. Refer to input electrical characteristics for Vil_FS and Vil_FS output with integrated 330hm series resistor. No 50 ohm resistor to GND needed. CPUT2_LPR OUT Ground pin for the CPU outputs OUT Ground pin for the CPU outputs OUT Ground pin for the CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR OUT Ground pin for the CPU outputs OUT Grou	PIN#	PIN NAME	TYPE	DESCRIPTION
SRCT0_LPR OUT Series resistor. No 500hm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RCR#1 IN Clock request for SRC1, 0 = enable, 1 = disable 29 VDDCORE_3.3 PWR 3.3V power for the PLL core OUT Complementary clock of differential outputs, nominal 1.5V. Complementary clock of differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC1_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC outputs SRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC outputs SRCC2_LPR OUT Ground pin for the SRC outputs SRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Ground pin for the CPU output selection. Refer to input electrical characteristics for Vil_FS and Vil_FS output with integrated 330hm series resistor. No 50 ohm resistor to GND needed. CPUT2_LPR OUT Ground pin for the CPU outputs OUT Ground pin for the CPU outputs OUT Ground pin for the CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR OUT Ground pin for the CPU outputs OUT Grou	25	GNDSRC	PWR	Ground pin for the SRC outputs
Senes resistor. No 500hm resistor to GND needed. 28 *CR#1 IN Clock request for SRC1, 0 = enable, 1 = disable 29 *VDDCORE_3.3 PWR 3.3 PWR Power supply for low power differential outputs, nominal 1.5V. 30 *VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 31 *SRCC1_LPR OUT Complementary clock of differential outputs, nominal 1.5V. 32 *SRCT1_LPR OUT True clock of differential 0.8V push-pull SRC output with integrated 330 series resistor. No 500hm resistor to GND needed. 33 *GNDSRC PWR Ground pin for the SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. 34 *SRCC2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. 35 *SRCT2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. 36 **CR#2 IN Clock request for SRC2, 0 = enable, 1 = disable 17 *Lock to differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. 38 *CPUC2_LPR OUT Clock request for SRC2, 0 = enable, 1 = disable 19 *Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil FS and Vih FS values. 39 *CPUT2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 40 *GNDCPU PWR Ground pin for the CPU outputs 41 *VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 42 *VDDCORE_3.3 PWR 3.3V power for the PLL core 44 *CPUT1_LPR OUT Saohm series resistor. No 50 ohm resistor to GND needed. 45 *GNDCPU PWR Ground pin for the CPU outputs 46 *GNDCPU PWR Ground pin for the CPU outputs 47 *CPUC0_LPR OUT Saohm series resistor. No 50 ohm resistor to GND needed. 48 *CPUT0_LPR OUT Saohm series resistor. No 50 ohm resistor to GND needed. 49 *CPUT0_LPR OUT Saohm series resistor. No 50 ohm resistor to GND needed. 40	06	SBCC0 LBB	OLIT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm
28 *CR#1 IN Clock request for SRC1, 0 = enable, 1 = disable 29 VDDCORE 3.3 PWR 3.3V power for the PLL core 30 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 31 SRCC1_LPR OUT 32 SRCT1_LPR OUT 33 GNDSRC PWR Ground pin for the PLL core resistor. No 500hm resistor to GND needed. 34 SRCC2_LPR OUT 35 SRCT2_LPR OUT 36 SRCT2_LPR OUT 37 FSB_L IN Clock request for SRC2, 0 = enable, 1 = disable 38 CPUC2_LPR OUT 39 CPUT2_LPR OUT 39 CPUT2_LPR OUT 40 GNDCPU PWR Ground pin for the PLL core 40 GNDCPU PWR Ground pin for the PLL core 41 VDDIO_1.5 PWR Power supply for low power differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 500hm resistor to GND needed. 39 CPUC1_LPR OUT 40 GNDCPU PWR Ground pin for the PLL core 41 VDDIO_1.5 PWR Power supply for low power differential pair 0.8V push-pull SRC output with integrated 33ohm series resistor. No 500hm resistor to GND needed. 40 GNDCPU PWR Ground pin for the PLL core 41 VDDIO_1.5 PWR Power supply for low power differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 500hm resistor to GND needed. 41 VDDIO_1.5 PWR Power supply for low power differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 500 hm resistor to GND needed. 42 CPUT1_LPR OUT 43 GNDCPU PWR Ground pin for the CPU outputs 44 CPUT1_LPR OUT 53 GNDCPU PWR Ground pin for the CPU outputs 54 GNDCPU PWR GROUND power for the PLL core 55 CPUC0_LPR OUT 56 GNDCPU PWR GROUND power differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 57 True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 58 CPUC1_LPR OUT 58 OND POWER STAND PO	20	SRCCU_LPR	0	series resistor. No 50ohm resistor to GND needed.
resistor. No 500hm resistor to GND needed. 1 N Clock request for SRC1, 0 = enable, 1 = disable 29 VDDCORE_3.3 30 VDDIO_1.5 PWR 3.3V power for the PLL core 30 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. Complementary clock of differential 0.8V push-pull SRC output with integrated 33ol series resistor. No 500hm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ol series resistor. No 500hm resistor to GND needed. RRCC2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33olm series resistor. No 500hm resistor to GND needed. SRCC2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33olm series resistor. No 500hm resistor to GND needed. SRCC2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33olm series resistor. No 500hm resistor to GND needed. SRCC2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 500hm resistor to GND needed. IN Clock request for SRC2, 0 = enable, 1 = disable CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differentia	27	SPCTO LDD		True clock of differential 0.8V push-pull SRC output with integrated 33ohm series
PWR 3.3V power for the PLL core	21	ShC10_LFN	5	resistor. No 50ohm resistor to GND needed.
SRCC1_LPR	28		IN	Clock request for SRC1, 0 = enable, 1 = disable
SRCC1_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33ol series resistor. No 50ohm resistor to GND needed. OUT True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. SRCC1_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. SRCC2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. IN Clock request for SRC2, 0 = enable, 1 = disable Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential outputs, nominal 1.5V. PWR Ground pin for the CPU outputs OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Strue clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential pair 0.8V push-pull CPU	29	VDDCORE_3.3	PWR	3.3V power for the PLL core
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resistor. No 50ohm resistor to GND needed. Ground pin for the SRC outputs OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. IN Clock request for SRC2, 0 = enable, 1 = disable IN Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Ground pin for the CPU outputs Ground pin for the CPU outputs CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential outputs, nominal 1.5V. CPUC1_LPR OUT COMPLEMENTARY COVER OUT Salah Pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR OUT COMPLEMENTARY COVER OUT Salah Pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR OUT COMPLEMENTARY COVER OUT Salah Pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with inte	31	ShCCI_LFh	0	series resistor. No 50ohm resistor to GND needed.
resistor. No 50ohm resistor to GND needed. 34 SRCC2_LPR OUT OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33oh series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. IN Clock request for SRC2, 0 = enable, 1 = disable Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. PWR Ground pin for the CPU outputs PWR CPUC1_LPR OUT Complementary clock of differential outputs, nominal 1.5V. CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR OUT Complementary clock of differential outputs, nominal 1.5V. Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	20	SPCT1 LDD	CIT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series
SRCC2_LPR OUT Complementary clock of differential 0.8V push-pull SRC output with integrated 33ols series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. IN Clock request for SRC2_0 = enable, 1 = disable Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. PWR Ground pin for the CPU outputs CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR OUT Ground pin for the CPU outputs CPUC1_LPR OUT Ground pin for the CPU outputs True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	32	ShCTI_LFN	0	resistor. No 50ohm resistor to GND needed.
series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. IN Clock request for SRC2, 0 = enable, 1 = disable Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. PWR Ground pin for the CPU outputs VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. PWR Ground pin for the CPU outputs GROUNDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	33	GNDSRC	PWR	Ground pin for the SRC outputs
series resistor. No 500hm resistor to GND needed. True clock of differential 0.8V push-pull SRC output with integrated 330hm series resistor. No 500hm resistor to GND needed. IN Clock request for SRC2, 0 = enable, 1 = disable Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. PWR Ground pin for the CPU outputs VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR OUT Complementary clock of differential outputs, nominal 1.5V. CPUC0_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed.	24	SBCC2 LBB	CIT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm
SRC12_LPR	34	ShCC2_LFh	5	series resistor. No 50ohm resistor to GND needed.
resistor. No 500hm resistor to GND needed. 1	25	SPCT2 LBB	CIT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series
IN Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. PWR Ground pin for the CPU outputs PWR Power supply for low power differential outputs, nominal 1.5V. PWR J. 3.3V power for the PLL core of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC1_LPR CPUT1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR Ground pin for the CPU outputs FWR Ground pin for the CPU outputs OUT Complementary clock of differential outputs, nominal 1.5V. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	33	35 SRC12_LPR		resistor. No 50ohm resistor to GND needed.
characteristics for Vil_FS and Vih_FS values. CPUC2_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. PWR Ground pin for the CPU outputs PWR Power supply for low power differential outputs, nominal 1.5V. PWR 3.3V power for the PLL core CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUC0_LPR OUT Complementary clock of differential outputs, nominal 1.5V. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	36	*CR#2	IN	Clock request for SRC2, 0 = enable, 1 = disable
Characteristics for VII_FS and VII_FS values. OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. PWR Power supply for low power differential outputs, nominal 1.5V. PWR J.33V power for the PLL core CPUC1_LPR OUT CPUC1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. FURDIO_1.5 PWR Ground pin for the CPU outputs Ground pin for the CPU outputs Ground pin for the CPU outputs CPUC0_LPR OUT Complementary clock of differential outputs, nominal 1.5V. COMPLEMENTARY CONDITION OF True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	27	ESB I	INI	Low threshold input for CPU frequency selection. Refer to input electrical
330hm series resistor. No 50 ohm resistor to GND needed. OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 40 GNDCPU PWR Ground pin for the CPU outputs 41 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 42 VDDCORE_3.3 PWR 3.3V power for the PLL core Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 43 CPUT1_LPR OUT CPUT1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU PWR Ground pin for the CPU outputs 46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed.	37	GD_L	IIN	
330hm series resistor. No 50 ohm resistor to GND needed. OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 40 GNDCPU PWR Ground pin for the CPU outputs 41 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 42 VDDCORE_3.3 PWR 3.3V power for the PLL core Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 43 CPUT1_LPR OUT CPUT1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU PWR Ground pin for the CPU outputs 46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed.	20	CDLICS LDD	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated
series resistor. No 50 ohm resistor to GND needed. 40 GNDCPU 41 VDDIO_1.5 42 VDDCORE_3.3 CPUC1_LPR 43 CPUT1_LPR 44 CPUT1_LPR 45 GNDCPU 46 VDDIO_1.5 CPUC0_LPR 47 CPUC0_LPR CPUC0_LPR COUT Series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR CPUC0_LPR CPUC0_LPR COUT Series resistor. No 50 ohm resistor to GND needed. Series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR CPUC0_LPR CPUC0_LPR CPUC0_LPR COUT Series resistor. No 50 ohm resistor to GND needed. CPUT1_LPR CPUC0_LPR CPUC0_LPR CPUC0_LPR CPUT1_LPR CPUC0_LPR	30	CI OCZ_LI II	0	33ohm series resistor. No 50 ohm resistor to GND needed.
Series resistor. No 50 ohm resistor to GND needed.	30	CDLIT2 LDD	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm
41 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 42 VDDCORE_3.3 PWR 3.3V power for the PLL core 43 CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 44 CPUT1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU PWR Ground pin for the CPU outputs 46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 47 CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 48 CPUT0_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm	39	CF012_LFN	0	series resistor. No 50 ohm resistor to GND needed.
42 VDDCORE_3.3 PWR 3.3V power for the PLL core 43 CPUC1_LPR OUT OUT COmplementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 44 CPUT1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU PWR Ground pin for the CPU outputs 46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUT0_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	40	GNDCPU	PWR	Ground pin for the CPU outputs
CPUC1_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. FWR Ground pin for the CPU outputs FWR Power supply for low power differential outputs, nominal 1.5V. CPUC0_LPR OUT COMPlementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. CPUT0_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	41	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
33ohm series resistor. No 50 ohm resistor to GND needed. 44 CPUT1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU 46 VDDIO_1.5 PWR Ground pin for the CPU outputs 46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUC0_LPR OUT CPUC0_LPR OUT COmplementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.	42	VDDCORE_3.3	PWR	3.3V power for the PLL core
330hm series resistor. No 50 ohm resistor to GND needed. 44 CPUT1_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU 46 VDDIO_1.5 PWR Ground pin for the CPU outputs Power supply for low power differential outputs, nominal 1.5V. CPUC0_LPR OUT CPUC0_LPR OUT OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 330hm series resistor. No 50 ohm resistor to GND needed.	12	CDLIC1 LDD	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated
series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU 46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 47 CPUCO_LPR OUT CPUCO_LPR OUT CPUCO_LPR OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm	43	CFOCT_LFR	0	33ohm series resistor. No 50 ohm resistor to GND needed.
series resistor. No 50 ohm resistor to GND needed. 45 GNDCPU 46 VDDIO_1.5 PWR Ground pin for the CPU outputs 46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. CPUCO_LPR OUT CPUCO_LPR OUT COMPlementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm	11	CDLIT1 LDD		True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm
46 VDDIO_1.5 PWR Power supply for low power differential outputs, nominal 1.5V. 47 CPUCO_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. 48 CPLITO LPB OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm	44	CFOTI_LFR	0	series resistor. No 50 ohm resistor to GND needed.
47 CPUC0_LPR OUT Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm	45	GNDCPU	PWR	Ground pin for the CPU outputs
33ohm series resistor. No 50 ohm resistor to GND needed. 48 CPUTO LPB OUT True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm	46	VDDIO_1.5	PWR	Power supply for low power differential outputs, nominal 1.5V.
33ohm series resistor. No 50 ohm resistor to GND needed. True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm	47	CDUCA LDD	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated
1 48 IUPHIII IPH	47		501	33ohm series resistor. No 50 ohm resistor to GND needed.
40 OLOTO_LITE OUT OUT Series resistant No FO show resistant OND residue!	10	CPLITO LPB	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm
series resistor. No 50 onm resistor to GND needed.	40		001	series resistor. No 50 ohm resistor to GND needed.

Funtional Block Diagram



Power Groups

Pin N	umber	n	occription.
VDD	GND	U	escription
41, 46	40, 45	CBLICLK	Low power outputs
42	40, 45	CFOCLK	VDDCORE_3.3V
30	25, 33	SBCCI K	Low power outputs
29	25, 33	SHOOLK	VDDCORE_3.3V
22	19	LCDCLK	Low power outputs
23	19	LODGER	VDDCORE_3.3V
15	10	DOT OSMba	Low power outputs
14	18	SRCCLK VDDCORE_3.3' Low power outpu VDDCORE_3.3' Low power outpu VDDCORE_3.3' Low power outpu VDDCORE_3.3' Low power outpu	VDDCORE_3.3V
5	7		Xtal, REF

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
3.3V Supply Voltage	VDDxxx_3.3	Supply Voltage		3.9	V	1,2
1.5V Supply Voltage	VDDxxx_1.5	Supply Voltage		2.1	V	1,2
3.3_Input High Voltage	V _{IH3.3}	3.3V Inputs		VDD_3.3+ 0.3V	V	1,2,3
Minimum Input Voltage	V _{IL}	Any Input	GND - 0.5		٧	1
Storage Temperature	Ts	-	-65	150	°C	1,2
Input ESD protection	ESD prot	Human Body Model	2000		V	1,2
input LOD protection	LOD PIOU	Man Machine Model	200		V 13+ V 1	1,2

¹Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	No Airflow	0	70	°C	1
3.3V Supply Voltage	VDDxxx_3.3	3.3V +/- 5%	3.135	3.465	V	1
1.5V Supply Voltage	VDDxxx_1.5	1.5V +/- 5%	1.425	1.575	V	1
3.3V Input High Voltage	V _{JHSE3.3}	Single-ended inputs	2	$V_{DD} + 0.3$	V	1
3.3V Input Low Voltage	V _{ILSE3.3}	Single-ended inputs	V _{SS} - 0.3	0.8	V	1
Input Leakage Current	\\link	$V_{IN} = V_{DD}, V_{IN} = GND$	-5	5	uA	1
Input Leakage Current	INRES	Inputs with pull or pull down resistors (CR# pins) $V_{IN} = V_{DD}, V_{IN} = GND$	-200	200	uA	1
Output High Voltage	V _{OHSE}	Single-ended outputs, I _{OH} = -1 mA	2.4		V	1
Output Low Voltage	V _{OLSE}	Single-ended outputs, I _{OL} = 1 mA		0.4	V	1
Low Threshold Input- High Voltage	V _{IH_FS}	3.3 V +/-5%	0.7	1.5	٧	1
Low Threshold Input- Low Voltage	V_{IL_FS}	3.3 V +/-5%	V _{SS} - 0.3	0.35	٧	1
	I _{DD_DEFAULT}	3.3V supply, LCDPLL off		55	mA	1
Operating Supply Current	I _{DD_LCDEN}	3.3V supply, LCDPLL enabled		60	mA	1
	I _{DD_IO}	1.5V supply, Differential IO current, all outputs enabled		50	mA	1
	I _{DD_PD3.3}	3.3V supply, Power Down Mode		1	mA	1
Power Down Current	I _{DD_PDIO}	1.5V IO supply, Power Down Mode		0.1	mA	1
Input Frequency	F _i	$V_{DD} = 3.3 \text{ V}$		15	MHz	2
Pin Inductance	L_{pin}			7	nΗ	1
	C _{IN}	Logic Inputs	1.5	5	pF	1
Input Capacitance	C _{OUT}	Output pin capacitance		6	pF	1
	C _{INX}	X1 & X2 pins		5	рF	1
Spread Spectrum Modulation Frequency	f _{ssmod}	Triangular Modulation	30	33	kHz	1

² Operation under these conditions is neither implied, nor guaranteed.

³ Maximum input voltage is not to exceed maximum VDD

AC Electrical Characteristics - Input/Common Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	T _{STAB}	From VDD Power-Up or de- assertion of PD# to 1st clock		1.8	ms	1
Tdrive_SRC	T _{DRSRC}	SRC output enable after PCI_STOP# de-assertion		15	ns	1
Tdrive_PD#	T _{DRPD}	Differential output enable after PD# de-assertion		300	us	1
Tdrive_CPU	T _{DRSRC}	CPU output enable after CPU_STOP# de-assertion		10	ns	<u></u>
Tfall_PD#	T _{FALL}	Fall/rise time of PD# and		5	ns	\ \(\1\)
Trise_PD#	T _{RISE}	CPU_STOP# inputs		5	ns	1

AC Electrical Characteristics - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t _{SLR}	Differential Measurement	0.5	4	V/ns	1,2
Falling Edge Slew Rate	t _{FLR}	Differential Measurement	0.5	\\\ <u>4</u> \\	V/ns	1,2
Rise/Fall Time Variation	t _{SLVAR}	Single-ended Measurement		125	ps	1
Maximum Output Voltage	V _{HIGH}	Includes overshoot		1150	mV	1
Minimum Output Voltage	V _{LOW}	Includes undershoot	-300		mV	1
Differential Voltage Swing	V _{SWING}	Differential Measurement	300		mV	1
Crossing Point Voltage	V _{XABS}	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	V _{XABSVAR}	Single-ended Measurement		140	mV 🤇	1,3,5
Duty Cycle	D _{CYC}	Differential Measurement	45	_△ 55	%	^{>} 1
CPU Jitter - Cycle to Cycle	CPUJ _{C2C}	Differential Measurement		85	ps	1
SRC Jitter - Cycle to Cycle	SRCJ _{C2C}	Differential Measurement		125	ps	1
DOT Jitter - Cycle to Cycle	DOTJ _{C2C}	Differential Measurement		250	ps	1
CPU[2:0] Skew	CPU _{SKEW10}	Differential Measurement		100	ps	1
SRC[2:0] Skew	SRC _{SKEW}	Differential Measurement		250	ps	1

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-300	300	ppm	1,2
Clock period	T _{period}	14.318MHz output nominal	69.8203	69.8622	ns	2
Absolute min/max period	T _{abs}	14.318MHz output nominal	69.8203	70.86224	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4		V	1
Output Low Voltage)) V _{OL}	I _{OL} = 1 mA		0.4	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V, V _{OH} @ MAX = 3.135 V	-33	-33	mA	1
Output Low Current	I _{OL}	V_{OL} @ MIN = 1.95 V, V_{OL} @ MAX = 0.4 V	30	38	mA	1
Rising Edge Slew Rate	t _{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	t _{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45	55	%	1
Jitter	t _{jcyc-cyc}	V _T = 1.5 V		1000	ps	1

Electrical Characteristics - SMBus Interface

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	V_{DD}		2.7	3.3	V	1
Low-level Output Voltage	V_{OLSMB}	@ I _{PULLUP}		0.4	V	1
Current sinking at	-	SMB Data Pin	4		т Л	,
$V_{OLSMB} = 0.4 V$	I _{PULLUP}	SIVIB Data PIN	4		mA	'
SCLK/SDATA	T _{RI2C}	(Max VIL - 0.15) to		1000	ns	1
Clock/Data Rise Time	' RI2C	(Min VIH + 0.15)		1000	113	
SCLK/SDATA	_	(Min VIH + 0.15) to		200		-
Clock/Data Fall Time	T _{FI2C}	(Max VIL - 0.15)		300	ns	1//
Maximum SMBus Operating	_	Block Mode		100	kHz	1
Frequency	F _{SMBUS}	Block Wode		100	KI IZ	

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

Clock Periods Differential Outputs with Spread Spectrum Enabled

Measureme	ent Window	1 Clock	1us (0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error 0ppm +	+ ppm error +SSC	Lg+)				
		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
Defir	Definition		Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
	SRC 100	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2
Signal Name	CPU 100	9.91400	9.99900	9.99900	10.00000	10.00100	10.05130	10.13630	ns	1,2
Sig	CPU 133	7.41425	7.49925	7.49925	7.50000	7.50075	7.53845	7.62345	ns	1,2
	CPU 166	5.91440	5.99940	5.99940	6.00000	6.00060	6.03076	6.11576	ns	1,2

Clock Periods Differential Outputs with Spread Spectrum Disabled

Clock i Cilodo Billolollada Outputo Will Opicad Opocada										
Measureme	ent Window	1 Clock) 1us	0.1s	0.1s	0.1s	1us	1 Clock		
Syr	nbol	Lg-	-ssc	C -ppm error	or Oppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute	Minimum Absolute	Minimum Absolute	Nominal	Maximum	Maximum	Maximum		
		Period	Period	Period					Units	Notes
Ð	SRC 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2
Name	CPU 100	9.91400		9.99900	10.00000	10.00100		10.13630	ns	1,2
<u>=</u>	CPU 133	7.41425		7.49925	7.50000	7.50075		7.62345	ns	1,2
Signal	CPU 166	5.91440		5.99940	6.00000	6.00060		6.11576	ns	1,2
S	DOT 96	10.16560		10.41560	10.41670	10.41770		10.66770	ns	1,2

¹Guaranteed by design and characterization, not 100% tested in production.

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² Slew rate measured through Vswing centered around differential zero

³ Vxabs is defined as the voltage where CLK = CLK#

⁴ Only applies to the differential rising edge (CLK rising and CLK# falling)

⁵ Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#. The average cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁶ All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz

⁷ Operation under these conditions is neither implied, nor guaranteed.

⁸ Maximum input voltage is not to exceed maximum VDD

⁹ See PCI Clock-to-Clock Delay Figure

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Table 1: CPU Frequency Select Table

FS _L C ¹	FS _L B ¹	CPU MHz	SRC MHz	DOT MHz	LCD MHz	REF MHz
0	0	133.33				
0	1	166.67	100.00	96.00	100.00	14.318
1	0	100.00				
1	1	Reserved				

FS_LC is a low-threshold input.Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Also refer to the Test Clarification Table.

Table 2: LCD Spread Select Table (Pin 20/21)

B1b5	B1b4	B1b3	Spread %	Comment
0	0	0	-0.5%	LCD100
0	0	1	-1%	LCD100
0	1	0	-2%	LCD100
0	1	1	-2.5%	LCD100
1	0	0	+/- 0.25%	LCD100
1	0	1	+/-0.5%	LCD100
1	1	0	+/-1%	LCD100
1	1	1	+/-1.25%	LCD100

Table 3: CPU N-step Programming

			<u> </u>
CPU (MHz)	Р	Default N (hex)	Fcpu
133.33	3	64	= 4MHz x N/P
166.67	3	7D	= 4MHz x N/P
100.00	4	64	= 4MHz x N/P
200.00	2	64	= 4MHz x N/P

CPU Power Management Table

PD	CPU_STOP#	SMBus Register OE	CPU	CPU#
0	1	Enable	Running	Running
1	Χ	Enable	Low/20K	Low
0	0	Enable	High	Low
0	Х	Disable	Low/20K	Low

SRC, LCD, DOT Power Management Table

PD	CR_x#	SMBus Register OE	SRC	SRC#	DOT/LCD	DOT#/LCD#
0	0	Enable	Running	Running	Running	Running
1	Χ	X	Low/20K	Low	Low/20K	Low
0	1	Enable	Low/20K	Low	Running	Running
0	Χ	Disable	Low/20K	Low	Low/20K	Low

REF Power Management Table

PD	SMBus Register OE	REF
0	Enable	Running
1	Χ	Low
0	Disable	Low

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General I²C serial interface information for the ICS9UMS9633B

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will acknowledge
- Controller (host) sends the begining byte location = N
- ICS clock will acknowledge
- Controller (host) sends the data byte count = X
- ICS clock will acknowledge
- Controller (host) starts sending Byte N through Byte N + X -1
- ICS clock will acknowledge each byte one at a time
- · Controller (host) sends a Stop bit

In	dex Block M	Vrit	e Operation		
Col	ntroller (Host)		ICS (Slave/Receiver)		
T	starT bit				
Slav	e Address D2 _(H)				
WR	WRite				
			ACK		
Beg	inning Byte = N				
	•		ACK		
Data	Byte Count = X				
			ACK		
Begir	nning Byte N				
			ACK		
	0	ţ			
	0	X Byte	0		
	0	$ \times $	0		
			0		
Byte N + X - 1					
			ACK		
Р	stoP bit				

Inday Diade Write Operation

How to Read:

- · Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will acknowledge
- Controller (host) sends the begining byte location = N
- ICS clock will acknowledge
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will acknowledge
- ICS clock will send the data byte count = X
- ICS clock sends Byte N + X -1
- ICS clock sends Byte 0 through byte X (if X_(H) was written to byte 8).
- Controller (host) will need to acknowledge each byte
- · Controllor (host) will send a not acknowledge bit
- · Controller (host) will send a stop bit

In	dex Block Rea	ad (Operation	
Cor	ntroller (Host)	IC	S (Slave/Receiver)	
Т	starT bit			
Slav	e Address D2 _(H)			
WR	WRite			
		ACK		
Begi	nning Byte = N			
			ACK	
RT	Repeat starT			
Slav	e Address D3 _(H)			
RD	ReaD			
		ACK		
		Data Byte Count = X		
	ACK			
			Beginning Byte N	
	ACK			
		X Byte	0	
	0	<u>6</u>	0	
	0	×	0	
0				
	1	Ш	Byte N + X - 1	
N	Not acknowledge			
Р	stoP bit			

Byte 0 PLL & Divider Enable Register

Буш		PLL & DIVIGEI Ellar	ne riegiotei				
Bit(s)	Pin #	Name	Description	Type	0	1	Default
7	-	PLL1 Enable	This bit controls whether the PLL driving the CPU and SRC clocks is enabled or not.	RW	0 = Disabled	1 = Enabled	1
6	-	PLL2 Enable	This bit controls whether the PLL driving the DOT and clock is enabled or not.	RW	0 = Disabled	1 = Enabled	1
5	-	PLL3 Enable	This bit controls whether the PLL driving the LCD clock is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4	-		Reserved				0
3	-	CPU Divider Enable	This bit controls whether the CPU output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 7 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
2	-	SRC Output Divider Enable	This bit controls whether the SRC output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 7 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
1	-	LCD Output Divider Enable	This bit controls whether the LCD output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 5 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
0	-	DOT Output Divider Enable	This bit controls whether the DOT output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 6 is set to '0'.	RW	0 = Disabled	1 = Enabled	1

Byte 1 PLL SS Enable/Control Register

Ditt		Name Bearington Time 0						
Bit(s)	Pin #	Name	Description	Type	0	1	Default	
7		PLL1 SS Enable	This bit controls whether PLL1 has spread enabled or not. Spread spectrum for PLL1 is set at -0.5% down-spread. Note that PLL1 drives the CPU and SRC clocks.	RW	0 = Disabled	1 = Enabled	1	
6		PLL3 SS Enable	This bit controls whether PLL3 has spread enabled or not. Note that PLL3 drives the SSC clock, and that the spread spectrum amount is set in bits 3-5.	RW	0 = Disabled	1 = Enabled	1	
5			These 3 bits select the frequency of PLL3 and the		0 T-1-1- 0	1 OD O	0	
4		PLL3 FS Select	SSC clock when Byte 1 Bit 6 (PLL3 Spread	RW		LCD Spread	0	
3			Spectrum Enable) is set.		Selec	t Table	0	
2			Reserved					
1			Reserved					
0			Reserved				0	

Byte 2 Output Enable Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7		CPU0 Enable	This bit controls whether the CPU[0] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
6		CPU1 Enable	This bit controls whether the CPU[1] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
5		CPU2 Enable	This bit controls whether the CPU[2] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4		SRC0 Enable	This bit controls whether the SRC[0] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
3		SRC1 Enable	This bit controls whether the SRC[1] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
2		SRC2 Enable	This bit controls whether the SRC[2] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
1		DOT Enable	This bit controls whether the DOT output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
0		LCD100 Enable	This bit controls whether the LCD output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1

Byte 3 Output Control Register

Byte	3	Output Control Reg	ister				
Bit(s)	Pin#	Name	Description	Type	0	1	Default
7			Reserved				0
6			Reserved				0
5		REF Enable	This bit controls whether the REF output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4		REF Slew	These bits control the edge rate of the REF clock.	RW		Edge Rate n Edge Rate	10
3		TILI SIEW	These bits control the edge rate of the FILE Clock.	1100		Edge Rate eserved	10
2		CPU0 Stop Enable	This bit controls whether the CPU[0] output buffer is free-running or stoppable. If it is set to stoppable the CPU[0] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0
1		CPU1 Stop Enable	This bit controls whether the CPU[1] output buffer is free-running or stoppable. If it is set to stoppable the CPU[1] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0
0		CPU2 Stop Enable	This bit controls whether the CPU[2] output buffer is free-running or stoppable. If it is set to stoppable the CPU[2] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0

Byte 4 CPU PLL N Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default		
Bit 7			Reserved				1		
Bit 6			Reserved				1		
Bit 5			Reserved						
Bit 4			Reserved						
Bit 3			Reserved				1		
Bit 2			Reserved				1		
Bit 1			Reserved						
Bit 0		CPU N Div8	N Divider Prog bit 8	RW		-	0		

Byte 5 CPU PLL/N Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		CPU N Div7		RW		Χ	
Bit 6		CPU N Div6	RW RW RW	RW	Default deper	Χ	
Bit 5		CPU N Div5		'	Χ		
Bit 4		CPU N Div4		RW	input fre Default for CPU	Χ	
Bit 3		CPU N Div3	See Table 3: CPU N-step Programming	RW		Χ	
Bit 2		CPU N Div2		RW	Default for all other frequencies is 64h.	Χ	
Bit 1		CPU N Div1		RW	is t	Χ	
Bit 0		CPU N Div0		RW		Χ	

Byte 6 Reserved

Bit(s)	Pin #	Name	Control Function	Туре	0	1	Default		
Bit 7			Reserved				1		
Bit 6			Reserved				1		
Bit 5			Reserved						
Bit 4			Reserved						
Bit 3			Reserved				0		
Bit 2			Reserved				0		
Bit 1			Reserved				1		
Bit 0			Reserved				1		

Byte 7 Reserved

Bit(s)	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

Byte 8 Reser	ved	
--------------	-----	--

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				0
Bit 5			Reserved				0
Bit 4			Reserved				0
Bit 3			Reserved				0
Bit 2			Reserved				0
Bit 1			Reserved				0
Bit 0			Reserved				0

Byte 9 LCD100 PLL N Register

Bit(s)	Pin #	Name	Control Function	Туре	0	1	Default
Bit 7		LCD100 N Div7		R			Х
Bit 6		LCD100 N Div6		R			Х
Bit 5		LCD100 N Div5		R			Χ
Bit 4		LCD100 N Div4	N Divider Programming Byte9 bit(7:0) and Byte8	R	See N-step programming		Χ
Bit 3		LCD100 N Div3	bit7	R	forr	nula	Χ
Bit 2		LCD100 N Div2		R			Χ
Bit 1		LCD100 N Div1		R			Χ
Bit 0		LCD100 N Div0		R			Χ

Byte 10 Status Readback Register

			g. e. e.					
Bit(s)	Pin #	Name	Description	Туре	0	1	Default	
7	37	FSB	Frequency Select B	R	See Table 1: 0	Latch		
6	9	FSC	Frequency Select C	R	Selec	Latch		
5	24	CR0# Readbk	Real time CR0# State Indicator	R	CR0# is Low	CR0# is High	Χ	
4	28	CR1# Readbk	Real time CR1# State Indicator	R	CR1# is Low	CR1# is High	Χ	
3	36	CR2# Readbk	Real time CR2# State Indicator	R	CR2# is Low	CR2# is High	Х	
2			Reserved				0	
1			Reserved					
0			Reserved				0	

Byte 11 Revision ID/Vendor ID Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7		Rev Code Bit 3		R			Х
6		Rev Code Bit 2	Revision ID	R		Χ	
5		Rev Code Bit 1	(0 for A rev)	Χ			
4		Rev Code Bit 0		R	Vendor	Χ	
3		Vendor ID bit 3		R	Vendoi	Specific	0
2		Vendor ID bit 2	Vendor ID	R		0	
1		Vendor ID bit 1	Vendorib	R		0	
0		Vendor ID bit 0		R		1	

Byte 12 Device ID Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default	
7		DEV_ID3	Device ID MSB	R			0	
6		DEV_ID2	Device ID 2	R			0	
5		DEV_ID1	Device ID 1	R			1	
4		DEV_ID0	Device ID LSB	R			1	
3			Reserved				0	
2			Reserved				0	
1			Reserved					
0			Reserved				0	

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Byte 13 Reserved Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				0
Bit 6			Reserved				
Bit 5			Reserved				0
Bit 4		Reserved				0	
Bit 3		Reserved				0	
Bit 2		Reserved				0	
Bit 1		Reserved				0	
Bit 0			Reserved				0

Byte 14 Reserved Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default	
Bit 7			Reserved				0	
Bit 6			Reserved					
Bit 5			Reserved					
Bit 4		Reserved				0		
Bit 3		Reserved				0		
Bit 2		Reserved				0		
Bit 1		Reserved					0	
Bit 0			Reserved				0	

Byte 15 Byte Count Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default	
Bit 7		Reserved						
Bit 6			Reserved					
Bit 5		BC5	Byte Count 5	RW			0	
Bit 4		BC4	Byte Count 4	RW	Specifies Num	ber of bytes to	0	
Bit 3		BC3	Byte Count 3	RW	be read back d	uring an SMBus	1	
Bit 2		BC2	Byte Count 2	RW	rea	ad.	1	
Bit 1		BC1	Byte Count 1	RW	Default	is 0xF.	1	
Bit 0		BC0	Byte Count LSB	RW			1	

Bytes 16:40 are reserved

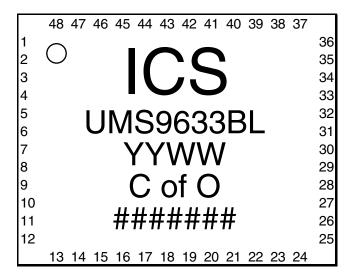
Byte 41 N Program Enable Register

Bit(s)	Pin #	Name	Control Function	Type	0	1	Default	
Bit 7			Reserved					
Bit 6			Reserved					
Bit 5			Reserved					
Bit 4			Reserved					
Bit 3			Reserved					
Bit 2		Reserved					0	
Bit 1		CPU N Enable	Enables CPU N programming	RW	Disabled	Enabled	0	
Bit 0		LCD N Enable	Enables LCD N programming	RW	Disabled	Enabled	0	

Test Clarification Table

Comments	Н	W	
	TEST_SEL HW PIN	TEST_MODE HW PIN	OUTPUT
	<0.35V	Х	NORMAL
Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode	>0.7V	<0.35V	HI-Z
TEST_MODE>low Vth input TEST_MODE is a real time input	>0.7V	>0.7V	REF/N

MLF Top Mark Information (9UMS9633BKLF)



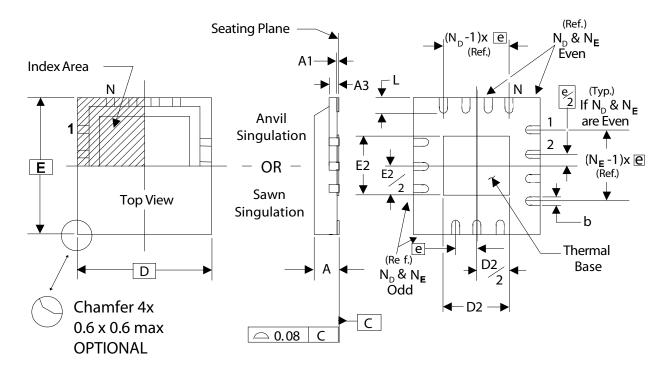
Line 1. Company name

Line 2. Part Number

Line 3. YYWW = Date Code

Line 3. Country of Origin

Line 4. ###### = Lot Number



THERMALLY ENHANCED, VERY THIN, FINE PITCH QUAD FLAT / NO LEAD PLASTIC PACKAGE

DIMENSIONS						
SYMBOL	MIN.	MAX.				
Α	8.0	1.0				
A1	0	0.05				
А3	0.20 Re	eference				
b	0.18	0.3				
e 0.40 BASIC						

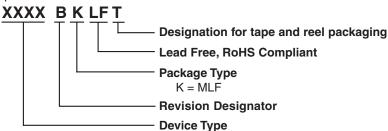
DIMENSIONS

	48L		
SYMBOL	TOLERANCE		
N	48		
N_D	12		
N _E	12		
D x E BASIC	6.00 x 6.00		
D2 MIN. / MAX.	3.95 / 4.25		
E2 MIN. / MAX.	3.95 / 4.25		
L MIN. / MAX.	0.30 / 0.50		

Ordering Information

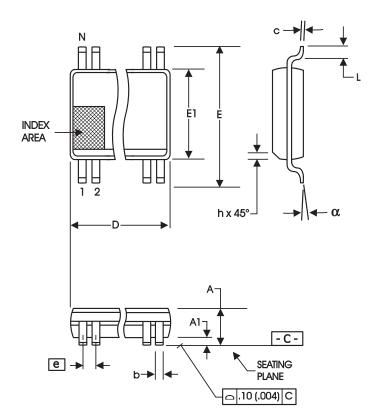
9UMS9633BKLFT





IDT™/ICS™ Ultra Mobile PC/Mobile Internet Device

1423—01/20/09



In Millimeters In Inches SYMBOL COMMON DIMENSIONS COMMON DIMENSIONS MIN MAX MIN MAX 2.41 2.80 .095 .110 0.20 0.40 .008 .016 .008 0.20 0.34 .0135 0.13 0.25 .005 .010 SEE VARIATIONS SEE VARIATIONS 10.03 10.68 .395 .420

Α1 b С D Ε .291 E1 7.40 7.60 .299 0.635 BASIC 0.025 BASIC е 0.38 0.64 .015 h .025 0.50 1.02 .020 .040 SEE VARIATIONS SEE VARIATIONS Ν 0° 0° 8° а

300 mil SSOP

VARIATIONS

N	D mm.		D (inch)		
N	MIN	MAX	MIN	MAX	
48	15.75	16.00	.620	.630	

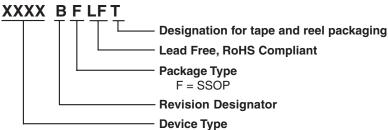
Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

9UMS9633BFLFT

Example:



IDT™/ICS™ Ultra Mobile PC/Mobile Internet Device

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Revision History

nevision mistory							
Rev.	Issue Date	Description	Page #				
0.1	12/06/07	Initial Release	-				
		1. Byte 4 default value changed to FF hex					
0.2	02/27/08	2. Byte 6 default value changed to F3 hex.					
		1. Corrected Reference in Byte 5 to CPU NDIV8. Should refer to					
		Byte 4, bit 0.					
		2. Corrected Reference in LCD100 NDIV to only refer to Byte 9					
		3. Corrected headings in clock period table.					
		4. Added N-step programming info.					
0.3	05/21/08	5. Corrected Byte 4 default value					
0.4	11/12/08	Removed reference to 1.5V inputs	Various				
0.5	01/20/09	Updated SMBus byte 4/5; added CPU N-Step Programming table	11,15				

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For Sales

800-345-7015 408-284-8200 Fax: 408-284-2775

For Tech Support

408-284-6578 pcclockhelp@idt.com

Corporate Headquarters

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138 United States 800 345 7015 +408 284 8200 (outside U.S.)

Asia Pacific and Japan

Integrated Device Technology Singapore (1997) Pte. Ltd. Reg. No. 199707558G 435 Orchard Road #20-03 Wisma Atria Singapore 238877 +65 6 887 5505

Europe

IDT Europe, Limited Prime House Barnett Wood Lane Leatherhead, Surrey United Kingdom KT22 7DE +44 1372 363 339



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