

# Four Output Differential Fanout Buffer for PCI Express Gen 1 & 2

ICS9DBL411

### **Recommended Application:**

PCI-Express fanout buffer

### **Output Features:**

- 4 low power differential output pairs
- Individual OE# control of each output pair

# **Key Specifications:**

- Output cycle-cycle jitter < 25ps additive
- Output to output skew: < 50ps

### Features/Benefits:

- Low power differential fanout buffer for PCI-Express and CPU clocks
- 20-pin MLF or TSSOP packaging

# **General Description:**

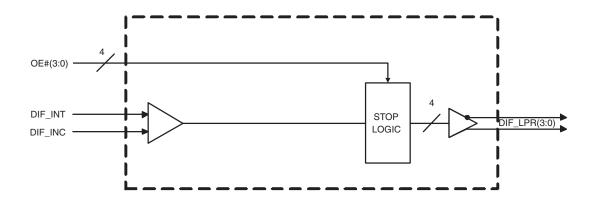
The **ICS9DBL411** is a 4 output lower power differential buffer. Each output has its own OE# pin. It has a maximum input frequency of 400 MHz.

### **Power Groups**

Pin Numl	per (TSSOP)	Description
VDD	GND	Description
9,18	10,17	DIF(3:0)
4	5	Analog VDD & GND

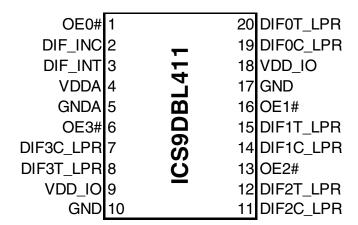
Pin Nun	nber (MLF)	Description		
VDD	GND	Description		
6,15	7,14	DIF(3:0)		
1	2	Analog VDD & GND		

### **Funtional Block Diagram**

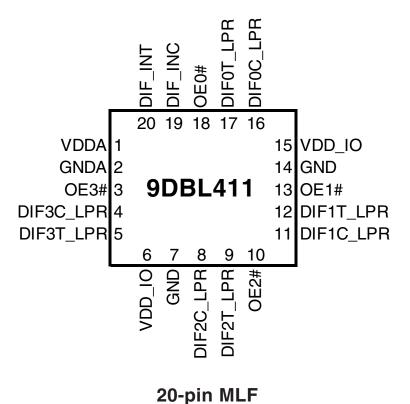


IDT™/ICS™ Four Output Differential Buffer for PCI Express

# **Pin Configuration**



20-pin TSSOP



IDT™/ICS™ Four Output Differential Buffer for PCI Express

# **TSSOP Pin Description**

PIN # (TSSOP)	PIN NAME	PIN TYPE	DESCRIPTION
4	OE0#	IN	Output Enable for DIF0 output. Control is as follows:
I	OE0#	IIN	0 = enabled, 1 = Low-Low
2	DIF_INC	IN	Complement side of differential input clock
3	DIF_INT	IN	True side of differential input clock
4	VDDA	PWR	3.3V Power for the Analog Core
5	GNDA	GND	Ground for the Analog Core
6	OE3#	IN	Output Enable for DIF3 output. Control is as follows:
6	OE3#	IIN	0 = enabled, 1 = Low-Low
7	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
8	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
10	GND	GND	Ground pin
11	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE2#	IN	Output Enable for DIF2 output. Control is as follows:
13	OE2#	IIN	0 = enabled, 1 = Low-Low
14	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
15	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
16	OE1#	IN	Output Enable for DIF1 output. Control is as follows:
10	OE1#	IIN	0 = enabled, 1 = Low-Low
17	GND	GND	Ground pin
18	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
19	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
20	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)

# **MLF Pin Description**

PIN # (MLF)	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDA	PWR	3.3V Power for the Analog Core
2	GNDA	GND	Ground for the Analog Core
3	OE3#	IN	Output Enable for DIF3 output. Control is as follows:  0 = enabled, 1 = Low-Low
4	DIF3C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
5	DIF3T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
6	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
7	GND	GND	Ground pin
8	DIF2C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
9	DIF2T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
10	OE2#	IN	Output Enable for DIF2 output. Control is as follows: 0 = enabled, 1 = Low-Low
11	DIF1C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
12	DIF1T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
13	OE1#	IN	Output Enable for DIF1 output. Control is as follows:  0 = enabled, 1 = Low-Low
14	GND	GND	Ground pin
15	VDD_IO	PWR	Power supply for low power differential outputs, nominal 1.05V to 3.3V
16	DIF0C_LPR	OUT	Complement clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
17	DIF0T_LPR	OUT	True clock of low power differential clock pair. (no 50ohm shunt resistor to GND needed)
18	OE0#	IN	Output Enable for DIF0 output. Control is as follows:  0 = enabled, 1 = Low-Low
19	DIF_INC	IN	Complement side of differential input clock
20	DIF_INT	IN	True side of differential input clock

### **Absolute Maximum Ratings**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDA	Core Supply Voltage		4.6	٧	1,7
Maximum Supply Voltage	VDD_IO	Low-Voltage Differential I/O Supply	0.99	3.8	V	1,7
Maximum Input Voltage	V <sub>IH</sub>	3.3V LVCMOS Inputs		4.6	V	1,7,8
Minimum Input Voltage	V <sub>IL</sub>	Any Input	Vss - 0.5		V	1,7
Storage Temperature	Ts	-	-65	150	°C	1,7
Input ESD protection	ESD prot	Human Body Model	2000		V	1,7

# **Electrical Characteristics - Input/Supply/Common Output Parameters**

	•					
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	°C	1
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.465	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.99	3.465	V	1
Input High Voltage	V <sub>IHSE</sub>	Single-ended inputs	2	$V_{DD} + 0.3$	V	1
Input Low Voltage	V <sub>ILSE</sub>	Single-ended inputs	V <sub>SS</sub> - 0.3	0.8	V	1
Differential Input High Voltage	V <sub>IHDIF</sub>	Differential inputs (single-ended measurement)	600	1.15	V	1
Differential Input Low Voltage	$V_{ILDIF}$	Differential inputs (single-ended measurement)	V <sub>SS</sub> - 0.3	300	V	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4	8	V/ns	2
Input Leakage Current	I <sub>IN</sub>	$V_{IN} = V_{DD}, V_{IN} = GND$	-5	5	uA	1
	I <sub>DD_3.3V</sub>	3.3V supply		25	mA	1
Operating Supply Current	I <sub>DD_IO+100M</sub>	VDD_IO supply @ fOP = 100MHz		15	mA	1
	I <sub>DD_IO_400M</sub>	VDD_IO supply @ fOP = 400MHz		54	mA	1
Standby Current	I <sub>DD SB33</sub>	3.3V supply, Input stopped		25	mA	1
Standby Current	I <sub>DD SBIO</sub>	VDD_IO supply, Input stopped		0.1	mA	1
Input Frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V	33	400	MHz	2
Pin Inductance	$L_{pin}$			7	nΗ	1
Input Capacitance	C <sub>IN</sub>	Logic Inputs	1.5	5	pF	1
mput Capacitance	C <sub>OUT</sub>	Output pin capacitance		6	pF	1
OE# latency	T <sub>OE#LAT</sub>	Number of clocks to enable or disable output from assertion/deassertion of OE#	1	3	periods	1
Tdrive_OE#	T <sub>DROE#</sub>	Output enable after OE# de-assertion		10	ns	1
Tfall_OE#	T <sub>FALL</sub>	Fall/rise time of OE# inputs		5	ns	1
Trise_OE#	T <sub>RISE</sub>	Tais in on OEm inputs		5	ns	1

### **AC Electrical Characteristics - DIF Low Power Differential Outputs**

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t <sub>SLR</sub>	Differential Measurement	1	2.5	V/ns	1,2
Falling Edge Slew Rate	t <sub>FLR</sub>	Differential Measurement	1	2.5	V/ns	1,2
Slew Rate Variation	t <sub>SLVAR</sub>	Single-ended Measurement		20	%	1
Maximum Output Voltage	V <sub>HIGH</sub>	Includes overshoot		1150	mV	1
Minimum Output Voltage	$V_{LOW}$	Includes undershoot	-300		mV	1
Differential Voltage Swing	V <sub>SWING</sub>	Differential Measurement	1200		mV	1
Crossing Point Voltage	V <sub>XABS</sub>	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	V <sub>XABSVAR</sub>	Single-ended Measurement		140	mV	1,3,5
	D <sub>CYCDIS0</sub>	Differential Measurement, fIN<=100MHz		0.5	%	1,6
Duty Cycle Distortion	D <sub>CYCDIS1</sub>	Differential Measurement 100MHz < flN<=267MHz		+5	%	1,6
	D <sub>CYCDIS2</sub>	Differential Measurement, fIN>267MHz		+7	%	1,6
DIF Jitter - Cycle to Cycle	DIFJ <sub>C2C</sub>	Differential Measurement,  Additive		25	ps	1
DIF[3:0] Skew	DIF <sub>SKEW</sub>	Differential Measurement		50	ps	1
Propagation Delay	t <sub>PD</sub>	Input to output Delay	2.5	3.5	ns	1
PCIe Gen2 Phase Jitter - Addtive	t <sub>phase_addHl</sub>	1.5MHz < fIN < Nyquist (50MHz)		0.8	ps rms	1
PCIe Gen2 Phase Jitter - Addtive	t <sub>phase_addLO</sub>	10KHz < fIN < 1.5MHz	-	0.1	ps rms	1

#### Notes on Electrical Characteristics:

<sup>&</sup>lt;sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>&</sup>lt;sup>2</sup> Slew rate measured through Vswing centered around differential zero

<sup>&</sup>lt;sup>3</sup> Vxabs is defined as the voltage where CLK = CLK#

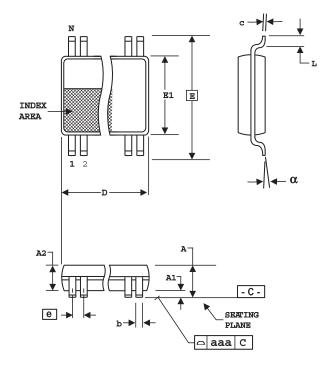
<sup>&</sup>lt;sup>4</sup> Only applies to the differential rising edge (CLK rising and CLK# falling)

<sup>&</sup>lt;sup>5</sup> Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

<sup>&</sup>lt;sup>6</sup> Tthis is the figure refers to the maximum distortion of the input wave form.

<sup>&</sup>lt;sup>7</sup> Operation under these conditions is neither implied, nor guaranteed.

<sup>&</sup>lt;sup>8</sup> Maximum input voltage is not to exceed maximum VDD



20-Lead, 4.40 mm. Body, 0.65 mm. Pitch TSSOP

	(17	3 IIIII <i>)</i>	(25.6 11111)	
	In Millimeters		In Inches	
SYMBOL	COMMON D	<b>IMENSIONS</b>	COMMON D	IMENSIONS
	MIN	MAX	MIN	MAX
Α		1.20		.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
С	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VAF	RIATIONS
E	6.40 BASIC		0.252	BASIC
E1	4.30	4.50	.169	.177
е	0.65 BASIC		0.0256	BASIC
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VAF	RIATIONS
а	0°	8°	0°	8°
aaa		0.10		.004

#### **VARIATIONS**

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
20	6.40	6.60	.252	.260

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

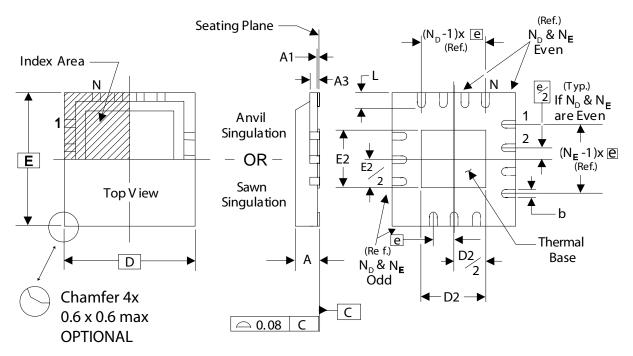
# **Ordering Information**

9DBL411yGLFT

Example:



IDT™/ICS™ Four Output Differential Buffer for PCI Express



THERMALLY ENHANCED, VERY THIN, FINE PITCH QUAD FLAT / NO LEAD PLASTIC PACKAGE

#### **DIMENSIONS**

SYMBOL	MIN.	MAX.	
Α	0.8	1.0	
A1	0	0.05	
A3	0.20 Re	ference	
b	0.18	0.3	
е	0.50 BASIC		

#### **DIMENSIONS**

SYMBOL	ICS 20L TOLERANCE		
N	20		
$N_D$	5		
N <sub>E</sub>	5		
D x E BASIC	4.00 x 4.00		
D2 MIN. / MAX.	2.00 / 2.25		
E2 MIN. / MAX.	2.00 / 2.25		
L MIN. / MAX.	0.45 / 0.65		

# **Ordering Information**

### 9DBL411yKLFT

Example:



IDT™/ICS™ Four Output Differential Buffer for PCI Express

**Revision History** 

Rev.	Issue Date	Description	Page #
0.1	08/01/06	Initial Release.	-
0.2	09/22/06	Updated MLF Package Dimensions.	8
		1. Updated electrical characteristics - additive jitter, cycle-to-cycle, tpd, skews,	
		slew rates, Idd, etc.	
		2. Corrected power grouping table for TSSOP pkg	
Α	07/31/07	3. Final Release	1,5,6
		1. Highlighted that V <sub>IHDIF</sub> and V <sub>ILDIF</sub> are single ended measurments.	
		2. Corrected VSWING paramater from 300mV to 1200mV.	
В	02/21/08	3. Updated duty cycle distortion table with a 3rd figure for speeds <=100MHz.	5

# Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

#### **For Sales**

800-345-7015 408-284-8200 Fax: 408-284-2775

#### For Tech Support

408-284-6578 pcclockhelp@idt.com

### **Corporate Headquarters**

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138 United States 800 345 7015 +408 284 8200 (outside U.S.)

#### **Asia Pacific and Japan**

Integrated Device Technology Singapore (1997) Pte. Ltd. Reg. No. 199707558G 435 Orchard Road #20-03 Wisma Atria Singapore 238877 +65 6 887 5505

#### **Europe**

IDT Europe, Limited Prime House Barnett Wood Lane Leatherhead, Surrey United Kingdom KT22 7DE +44 1372 363 339



© 2006 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice. IDT and the IDT logo are trademarks of Integrated Device Technology, Inc. Accelerated Thinking is a service mark of Integrated Device Technology, Inc. All other brands, product names and marks are or may be trademarks or registered trademarks used to identify products or services of their respective owners.

Printed in USA

IDT™/ICS™ Four Output Differential Buffer for PCI Express