

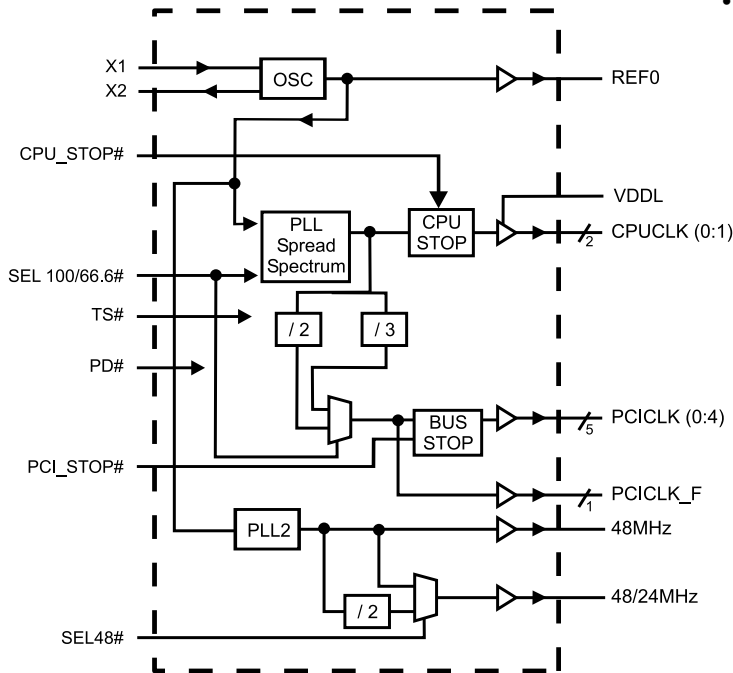
## Frequency Timing Generator for Pentium II Systems

### General Description

The **ICS9248-56** is the Main clock solution for Notebook designs using the Intel 440BX style chipset. Along with an SDRAM buffer such as the ICS9179-03, it provides all necessary clock signals for such a system.

Spread spectrum may be enabled by driving pin 26, SPREAD# active (Low) at power-on. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-56** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

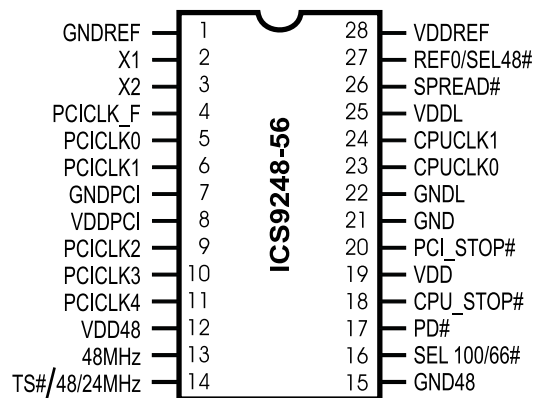
### Block Diagram



### Features

- Generates the following system clocks:
  - 2CPU(2.5V) up to 100MHz.
  - 6 PCI(3.3V) @ 33.3MHz (Includes one free running).
  - 1 REF clks (3.3V) at 14.318MHz.
  - 1 Fixed clock at 48MHz
  - 1 Fixed clock at 48 or 24MHz
- Skew characteristics:
  - CPU – CPU  $\leq 175$ ps
  - PCI – PCI  $\leq 500$ ps
  - CPU(early) – PCI = 1.5ns – 4ns.
- Supports Spread Spectrum modulation for CPU and PCI clocks, 0.5% down spread
- Efficient Power management scheme through stop clocks and power down modes.
- Uses external 14.318MHz crystal, no external load cap required for CL=18pF crystal.
- 28 pin 209mil SSOP and 173mil TSSOP

### Pin Configuration



### 28 pin SSOP and TSSOP

### Power Groups

VDD, GND= PLL core  
 VDDREF, GNDREF= REF(0:1), X1, X2  
 VDDPCI, GNDPCI= PCICLK\_F, PCICLK (0:4)  
 VDD48, GND48= 48MHz, 48/24MHz

Pentium is a trademark on Intel Corporation.



## Pin Descriptions

| Pin number  | Pin name     | Type   | Description   |
|-------------|--------------|--------|---|
| 1           | GNDREF       | Power  | Ground for 14.318 MHz reference clock outputs   |
| 2           | X1           | Input  | 14.318 MHz crystal input  |
| 3           | X2           | Output | 14.318 MHz crystal output   |
| 4           | PCICLK_F     | Output | 3.3 V free running PCI clock output, will not be stopped by the PCI_STOP#   |
| 5,6,9,10,11 | PCICLK (1:5) | Output | 3.3 V PCI clock outputs, generating timing requirements for Pentium II  |
| 7           | GNDPCI       | Power  | Ground for PCI clock outputs  |
| 8           | VDDPCI       | Power  | 3.3 V power for the PCI clock outputs   |
| 12          | VDD48        | Power  | 3.3 V power for 48/24 MHz clocks  |
| 13          | 48 MHz       | Output | 3.3 V 48 MHz clock output, fixed frequency clock typically used with USB devices  |
| 14          | TS#/48/24MHz | Output | 3.3 V 48 or 24 MHz output and Tri-state option, active low = tri state mode for testing, active high = normal operation   |
| 15          | GND48        | Power  | Ground for 48/24 MHz clocks   |
| 16          | SEL 100/66#  | Input  | control for the frequency of clocks at the CPU & PCICLK output pins. If logic "0" is used the 66.6 MHz frequency is selected. If Logic "1" is used, the 100 MHz frequency is selected. The PCI clock is multiplexed to run at 33.3 MHz for both selected cases. |
| 17          | PD#          | Input  | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.                                   |
| 18          | CPU_STOP#    | Input  | Asynchronous active low input pin used to stop the CPUCLK in active low state, all other clocks will continue to run. The CPUCLK will have a "Turnon " latency of at least 3 CPU clocks.  |
| 19          | VDD          | Power  | Isolated 3.3 V power for core   |
| 20          | PCI-Stop#    | Input  | Synchronous active low input used to stop the PCICLK in active low state. It will not effect PCICLK_F or any other outputs.   |
| 21          | GND          | Power  | Isolated ground for core  |
| 22          | GNDL         | Power  | Ground for CPU clock outputs  |
| 23,24       | CPUCLK(1:0)  | Output | 2.5 V CPU clock outputs   |
| 25          | VDDL         | Power  | 2.5 V power for CPU clock outputs   |
| 26          | SPREAD#      | Output | Power-on spread spectrum enable option. Active low = spread spectrum clocking enable. Active high = spread spectrum clocking disable.   |
| 27          | REF0/SEL48#  | Output | 3.3 V 14.318 MHz reference clock output and power-on 48/24 MHz select option. Active low = 48 MHz output at pin 14. Active high = 24 MHz output at pin 14.  |
| 28          | VDDREF       | Power  | 3.3 V power for 14.318 MHz reference clock outputs.   |



## Select Functions

(Functionality determined by TS# and SEL100/66# pin, see below)

| Functionality | CPUCLK              | PCI,<br>PCI_F       | REF0              |
|---------------|---------------------|---------------------|-------------------|
| Tristate      | HI - Z              | HI - Z              | HI - Z            |
| Testmode      | TCLK/2 <sup>1</sup> | TCLK/6 <sup>1</sup> | TCLK <sup>1</sup> |

Notes:

1. TCLK is a test clock driven on the X1 (crystal in pin) input during test mode.

| SEL 100/66# | TS# | Function                     |
|-------------|-----|------------------------------|
| 0           | 0   | Tri-State                    |
| 0           | -   | (Reserved)                   |
| 0           | -   | (Reserved)                   |
| 0           | 1   | Active 66.6MHz CPU, 33.3 PCI |
| 1           | 0   | Test Mode                    |
| 1           | -   | (Reserved)                   |
| 1           | -   | (Reserved)                   |
| 1           | 1   | Active 100MHz CPU, 33.3 PCI  |

## Power Management

### Clock Enable Configuration

| CPU_STOP# | PCI_STOP# | PWR_DWN# | CPUCLK      | PCICLK   | PCICLK_F | REF     | Crystal | VCOs    |
|-----------|-----------|----------|-------------|----------|----------|---------|---------|---------|
| X         | X         | 0        | Low         | Low      | Low      | Stopped | Off     | Off     |
| 0         | 0         | 1        | Low         | Low      | 33.3MHz  | Running | Running | Running |
| 0         | 1         | 1        | Low         | 33.3 MHz | 33.3MHz  | Running | Running | Running |
| 1         | 0         | 1        | 100/66.6MHz | Low      | 33.3MHz  | Running | Running | Running |
| 1         | 1         | 1        | 100/66.6MHz | 33.3 MHz | 33.3MHz  | Running | Running | Running |

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PD# pin will not cause clocks of a short or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

### ICS9248-56 Power Management Requirements

| SIGNAL    | SIGNAL STATE                      | Latency<br>No. of rising edges of free running<br>PCICLK |
|-----------|-----------------------------------|--|
| CPU_STOP# | 0 (Disabled) <sup>2</sup>         | 1  |
|           | 1 (Enabled) <sup>1</sup>          | 1  |
| PCI_STOP# | 0 (Disabled) <sup>2</sup>         | 1  |
|           | 1 (Enabled) <sup>1</sup>          | 1  |
| PD#       | 1 (Normal Operation) <sup>3</sup> | 3ms  |
|           | 0 (Power Down) <sup>4</sup>       | 2max   |

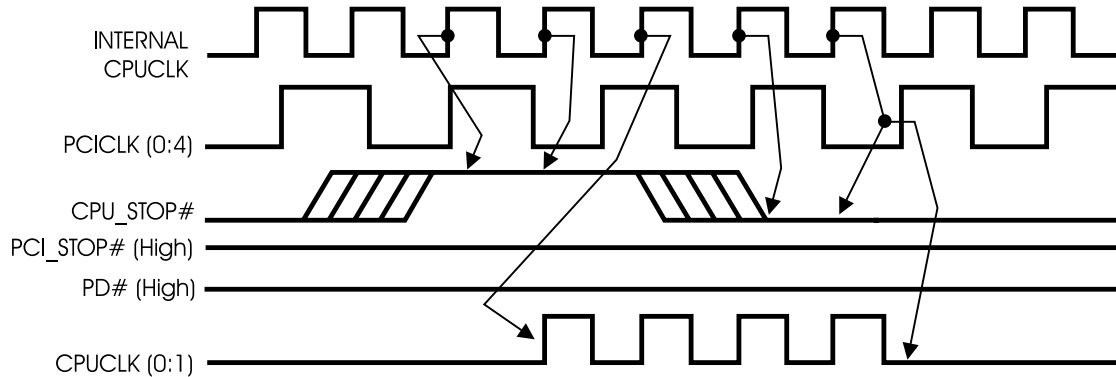
Notes.

1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.  
The REF will be stopped independent of these.



## CPU\_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU\_STOP# is synchronized by the **ICS9248-56**. The minimum that the CPUCLK is enabled (CPU\_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

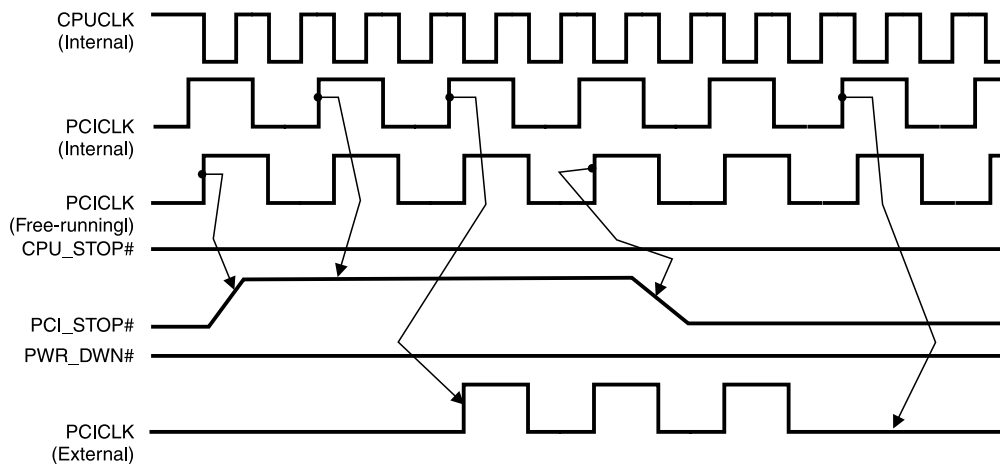


### Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-56**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI\_STOP# are shown in a high (true) state.

## PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the **ICS9248-56**. It is used to turn off the PCICLK (0:4) clocks for low power operation. PCI\_STOP# is synchronized by the **ICS9248-56** internally. The minimum that the PCICLK (0:4) clocks are enabled (PCI\_STOP# high pulse) is at least 10 PCICLK (0:4) clocks. PCICLK (0:4) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:4) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



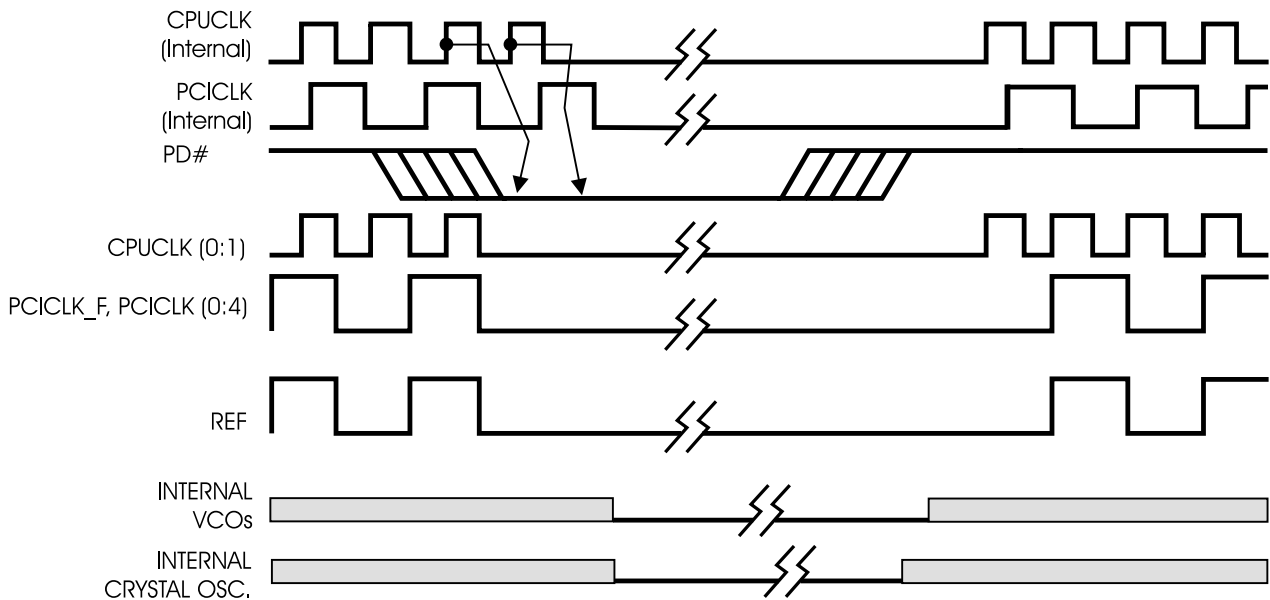
### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. PD# and CPU\_STOP# are shown in a high (true) state.



## PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internally by the ICS9248-56 prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI\_STOP# and CPU\_STOP# are don't care signals during the power down operations.



### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9248.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.



## Absolute Maximum Ratings

|                               |                                     |
|-------------------------------|-------------------------------------|
| Supply Voltage                | 7.0 V                               |
| Logic Inputs                  | GND-0.5 V to V <sub>DD</sub> +0.5 V |
| Ambient Operating Temperature | 0°C to +70°C                        |
| Storage Temperature           | -65°C to +150°C                     |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70C; Supply Voltage V<sub>DD</sub> = V<sub>DDL</sub> = 3.3 V +/-5% (unless otherwise stated)

| PARAMETER                      | SYMBOL                  | CONDITIONS  | MIN                  | TYP    | MAX                  | UNITS |
|--------------------------------|-------------------------|---|----------------------|--------|----------------------|-------|
| Input High Voltage             | V <sub>IH</sub>         |   | 2                    |        | V <sub>DD</sub> +0.3 | V     |
| Input Low Voltage              | V <sub>IL</sub>         |   | V <sub>SS</sub> -0.3 |        | 0.8                  | V     |
| Input High Current             | I <sub>IH</sub>         | V <sub>IN</sub> = V <sub>DD</sub>                                   |                      | 0.1    | 5                    | μA    |
| Input Low Current              | I <sub>IL1</sub>        | V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors             | -5                   | 2.0    |                      | μA    |
| Input Low Current              | I <sub>IL2</sub>        | V <sub>IN</sub> = 0 V; Inputs with pull-up resistors                | -200                 | -100   |                      | μA    |
| Operating Supply Current       | I <sub>DD3.3OP66</sub>  | C <sub>L</sub> = 0 pF; Select @ 66MHz                               |                      | 60     | 180                  | mA    |
|                                | I <sub>DD3.3OP100</sub> | C <sub>L</sub> = 0 pF; Select @ 100MHz                              |                      | 66     | 180                  | mA    |
| Power Down Supply Current      | I <sub>DD3.3PD</sub>    | C <sub>L</sub> = 0 pF; With input address to V <sub>DD</sub> or GND |                      | 70     | 600                  | μA    |
| Input frequency                | F <sub>i</sub>          | V <sub>DD</sub> = 3.3 V;  | 11                   | 14.318 | 16                   | MHz   |
| Input Capacitance <sup>1</sup> | C <sub>IN</sub>         | Logic Inputs  |                      |        | 5                    | pF    |
|                                | C <sub>INX</sub>        | X1 & X2 pins  | 27                   | 36     | 45                   | pF    |
| Transition Time <sup>1</sup>   | T <sub>trans</sub>      | To 1st crossing of target Freq.                                     |                      |        | 3                    | ms    |
| Clk Stabilization <sup>1</sup> | T <sub>STAB</sub>       | From V <sub>DD</sub> = 3.3 V to 1% target Freq.                     |                      |        | 3                    | ms    |
| Skew <sup>1</sup>              | T <sub>CPU-PCI</sub>    | V <sub>T</sub> = 1.5 V;   | 1.5                  | 2.4    | 4                    | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5% (unless otherwise stated)

| PARAMETER                | SYMBOL                  | CONDITIONS                                       | MIN | TYP | MAX | UNITS |
|--------------------------|-------------------------|--|-----|-----|-----|-------|
| Operating Supply Current | I <sub>DD2.5OP66</sub>  | C <sub>L</sub> = 0 pF; Select @ 66.8 MHz         |     | 16  | 72  | mA    |
|                          | I <sub>DD2.5OP100</sub> | C <sub>L</sub> = 0 pF; Select @ 100 MHz          |     | 23  | 100 | mA    |
| Skew <sup>1</sup>        | t <sub>CPU-PCI2</sub>   | V <sub>T</sub> = 1.5 V; V <sub>TL</sub> = 1.25 V | 1.5 | 3   | 4   | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**Electrical Characteristics - CPUCLK**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ,  $V_{DDL} = 2.5 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

| PARAMETER           | SYMBOL                    | CONDITIONS  | MIN  | TYP  | MAX  | UNITS |
|---------------------|---------------------------|---|------|------|------|-------|
| Output High Voltage | $V_{OH2B}$                | $I_{OH} = -12.0 \text{ mA}$                         | 1.8  | 2.3  |      | V     |
| Output Low Voltage  | $V_{OL2B}$                | $I_{OL} = 12 \text{ mA}$                            |      | 0.31 | 0.4  | V     |
| Output High Current | $I_{OH2B}$                | $V_{OH} = 1.7 \text{ V}$                            |      |      | -27  | mA    |
| Output Low Current  | $I_{OL2B}$                | $V_{OL} = 0.7 \text{ V}$                            | 27   |      |      | mA    |
| Rise Time           | $t_{r2B}^1$               | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.0 \text{ V}$ | 0.4  | 1.15 | 1.6  | ns    |
| Fall Time           | $t_{f2B}^1$               | $V_{OH} = 2.0 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ | 0.4  | 1.4  | 1.6  | ns    |
| Duty Cycle          | $d_{t2B}^1$               | $V_T = 1.25 \text{ V}$                              | 44   | 48   | 55   | %     |
| Skew                | $t_{sk2B}^1$              | $V_T = 1.25 \text{ V}$                              |      | 134  | 175  | ps    |
| Jitter              | $t_{j\text{cyc-cyc}2B}^1$ | $V_T = 1.25 \text{ V}$                              |      | 186  | 250  | ps    |
|                     | $t_{j1s2B}^1$             | $V_T = 1.25 \text{ V}$                              |      | 52   | 150  | ps    |
|                     | $t_{j\text{abs}2B}^1$     | $V_T = 1.25 \text{ V}$                              | -250 | 150  | +250 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - PCICLK**

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$

| PARAMETER               | SYMBOL                  | CONDITIONS  | MIN | TYP | MAX | UNITS |
|-------------------------|-------------------------|---|-----|-----|-----|-------|
| Output High Voltage     | $V_{OH1}$               | $I_{OH} = -18 \text{ mA}$                           | 2.1 | 3.3 |     | V     |
| Output Low Voltage      | $V_{OL1}$               | $I_{OL} = 9.4 \text{ mA}$                           |     | 0.1 | 0.4 | V     |
| Output High Current     | $I_{OH1}$               | $V_{OH} = 2.0 \text{ V}$                            |     |     | -22 | mA    |
| Output Low Current      | $I_{OL1}$               | $V_{OL} = 0.8 \text{ V}$                            | 16  |     | 57  | mA    |
| Rise Time <sup>1</sup>  | $t_{r1}$                | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ |     | 1.6 | 2   | ns    |
| Fall Time <sup>1</sup>  | $t_{f1}$                | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ |     | 1.8 | 2   | ns    |
| Duty Cycle <sup>1</sup> | $d_{t1}$                | $V_T = 1.5 \text{ V}$                               | 45  | 50  | 55  | %     |
| Skew <sup>1</sup>       | $t_{sk1}$               | $V_T = 1.5 \text{ V}$                               |     | 222 | 500 | ps    |
| Jitter                  | $t_{j\text{cyc-cyc}}^1$ | $V_T = 1.5 \text{ V}$                               |     | 186 | 500 | ps    |
|                         | $t_{j1s1}$              | $V_T = 1.5 \text{ V}$                               |     | 52  | 150 | ps    |
|                         | $t_{j\text{abs}1}$      | $V_T = 1.5 \text{ V}$                               |     | 200 | 500 | ps    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



## Electrical Characteristics - REF/48MHz/24MHz

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

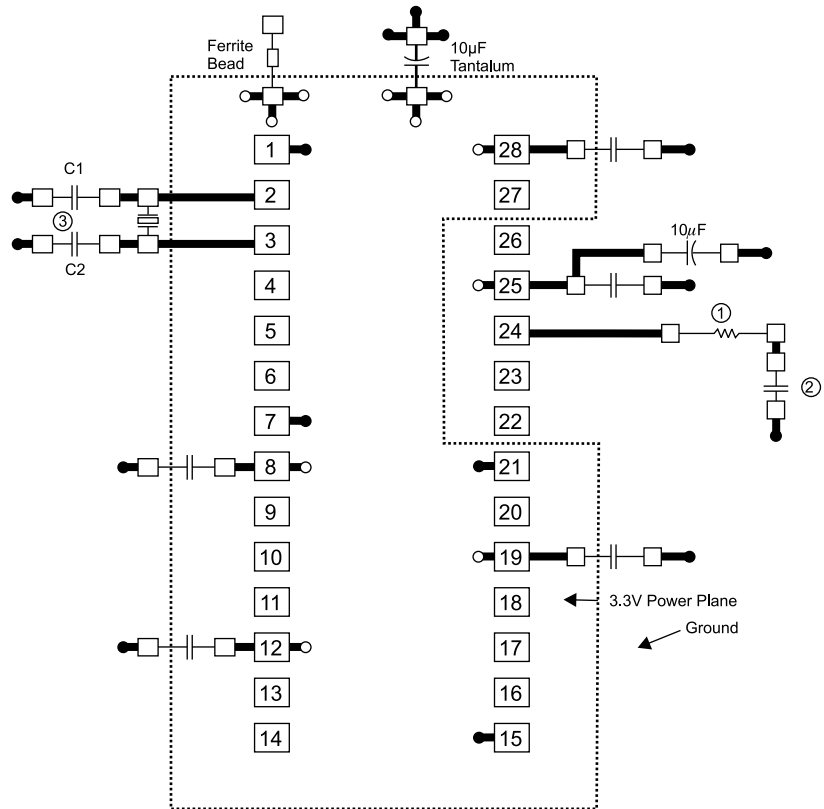
| PARAMETER               | SYMBOL          | CONDITIONS                                       | MIN | TYP  | MAX | UNITS |
|-------------------------|-----------------|--|-----|------|-----|-------|
| Output High Voltage     | $V_{OH5}$       | $I_{OH} = -12 \text{ mA}$                        | 2.6 | 3.1  |     | V     |
| Output Low Voltage      | $V_{OL5}$       | $I_{OL} = 9 \text{ mA}$                          |     | 0.17 | 0.4 | V     |
| Output High Current     | $I_{OH5}$       | $V_{OH} = 2.0 \text{ V}$                         |     | -44  | -22 | mA    |
| Output Low Current      | $I_{OL5}$       | $V_{OL} = 0.8 \text{ V}$                         | 16  | 42   |     | mA    |
| Rise Time <sup>1</sup>  | $t_{r5}$        | $V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$ |     | 1.4  | 4   | ns    |
| Fall Time <sup>1</sup>  | $t_{f5}$        | $V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$ |     | 1.1  | 4   | ns    |
| Duty Cycle <sup>1</sup> | $d_{t5}$        | $V_T = 1.5 \text{ V}$                            | 45  | 53   | 55  | %     |
| Jitter <sup>1</sup>     | $t_{j1\sigma5}$ | $V_T = 1.5 \text{ V}, \text{REF}$                |     | 185  | 250 | ps    |
|                         | $t_{jabs5}$     | $V_T = 1.5 \text{ V}, \text{REF}$                |     | 385  | 800 | ps    |
| Jitter <sup>1</sup>     | $t_{j1\sigma5}$ | $V_T = 1.5 \text{ V}, 48 \text{ MHz}$            |     | 169  | 250 | ps    |
|                         | $t_{jabs5}$     | $V_T = 1.5 \text{ V}, 48 \text{ MHz}$            |     | 469  | 800 | ps    |





**General Layout Precautions:**

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.



**Notes:**

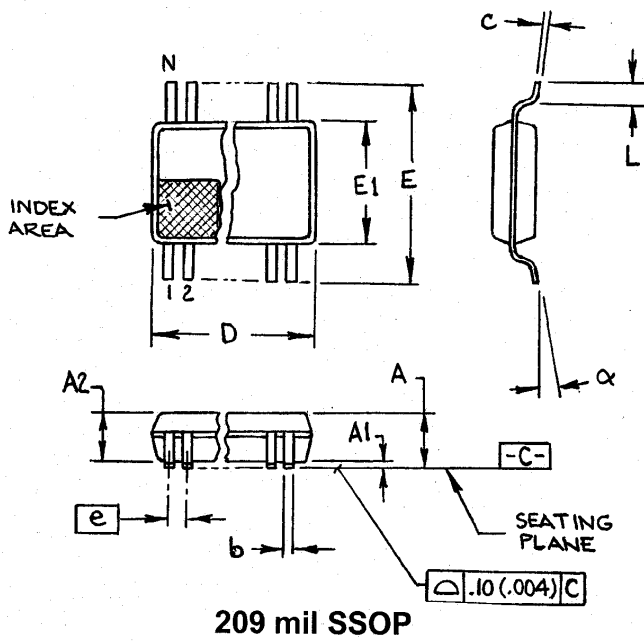
- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
- 3 Optional crystal load capacitors are recommended.

- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads

**Capacitor Values:**

C1, C2 : Crystal load values determined by user

All unmarked capacitors are 0.01 F ceramic



| SYMBOL   | In Millimeters<br>COMMON DIMENSIONS |      | In Inches<br>COMMON DIMENSIONS |      |
|----------|-------------------------------------|------|--------------------------------|------|
|          | MIN                                 | MAX  | MIN                            | MAX  |
| A        | -                                   | 2.00 | -                              | .079 |
| A1       | 0.05                                | -    | .002                           | -    |
| A2       | 1.65                                | 1.85 | .065                           | .073 |
| b        | 0.22                                | 0.38 | .009                           | .015 |
| c        | 0.09                                | 0.25 | .0035                          | .010 |
| D        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| E        | 7.40                                | 8.20 | .291                           | .323 |
| E1       | 5.00                                | 5.60 | .197                           | .220 |
| e        | 0.65 BASIC                          |      | 0.0256 BASIC                   |      |
| L        | 0.55                                | 0.95 | .022                           | .037 |
| N        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| $\alpha$ | 0°                                  | 8°   | 0°                             | 8°   |

VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 28 | 9.90  | 10.50 | .390     | .413 |

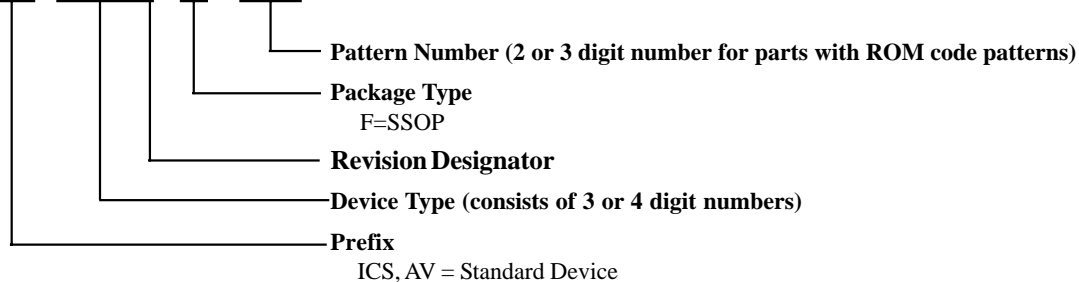
MO-150 JEDEC 6/100 Rev B  
Doc.# 10-0033

Ordering Information

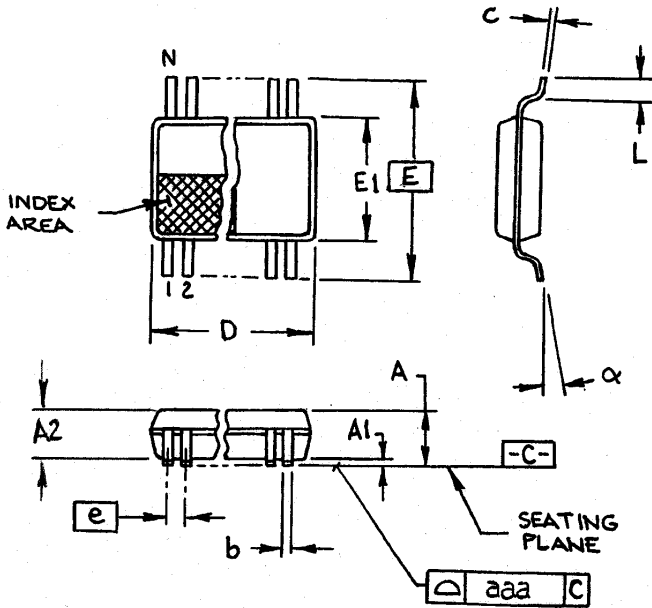
ICS9248F-56

Example:

**ICS XXXXy F - PPP**



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.



4.40 mm. Body, 0.65 mm. pitch TSSOP  
(173 mil) (0.0256 mil)

| SYMBOL   | In Millimeters<br>COMMON DIMENSIONS |      | In Inches<br>COMMON DIMENSIONS |      |
|----------|-------------------------------------|------|--------------------------------|------|
|          | MIN                                 | MAX  | MIN                            | MAX  |
| A        | -                                   | 1.20 | -                              | .047 |
| A1       | 0.05                                | 0.15 | .002                           | .006 |
| A2       | 0.80                                | 1.05 | .032                           | .041 |
| b        | 0.19                                | 0.30 | .007                           | .012 |
| c        | 0.09                                | 0.20 | .0035                          | .008 |
| D        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| E        | 6.40 BASIC                          |      | 0.252 BASIC                    |      |
| E1       | 4.30                                | 4.50 | .169                           | .177 |
| e        | 0.65 BASIC                          |      | 0.0256 BASIC                   |      |
| L        | 0.45                                | 0.75 | .018                           | .030 |
| N        | SEE VARIATIONS                      |      | SEE VARIATIONS                 |      |
| $\alpha$ | 0°                                  | 8°   | 0°                             | 8°   |
| aaa      | -                                   | 0.10 | -                              | .004 |

VARIATIONS

| N  | D mm. |      | D (inch) |      |
|----|-------|------|----------|------|
|    | MIN   | MAX  | MIN      | MAX  |
| 28 | 9.60  | 9.80 | .378     | .386 |

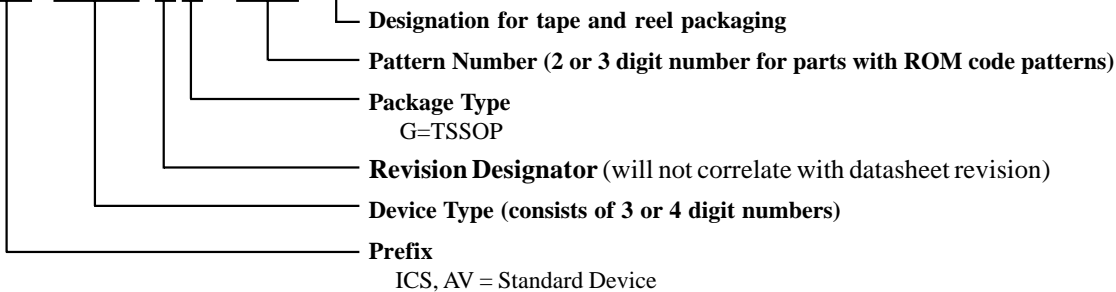
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Ordering Information

ICS9248yG-56-T

Example:

ICS XXXX y G - PPP - T



ICS reserves the right to make changes in the device data identified in this publication without further notice. ICS advises its customers to obtain the latest version of all device data to verify that any information being relied upon by the customer is current and accurate.