Integrated Circuit Systems, Inc.

ICS9248-72

Preliminary Product Preview

Frequency Timing Generator for PENTIUM II Systems

General Description

The **ICS9248-72** is a main clock synthesizer chip for Pentium II based systems using Rambus Interface DRAMs. This chip provides all the clocks required for such a system when used with a Direct Rambus Clock Generator(DRCG) chip such as the ICS9211-01.

Spread Spectrum may be enabled by driving the SPREAD# pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-72** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

The CPU/2 clocks are inputs to the DRCG.

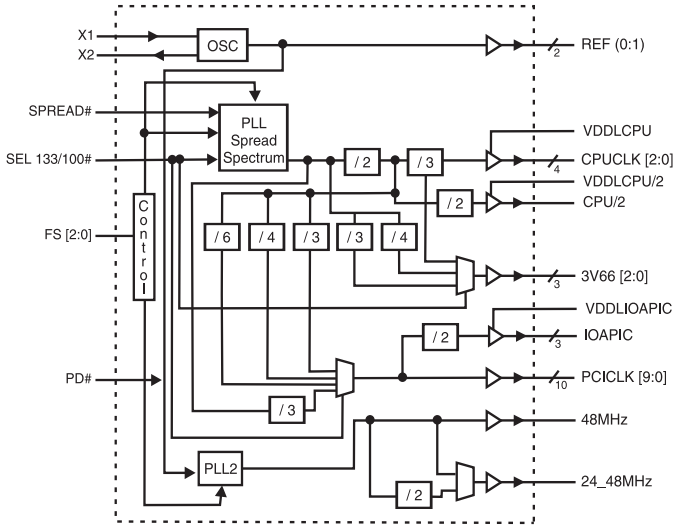
Features

- Up to 200MHz frequency support.
- Power Down feature.
- Spread Spectrum for EMI control (0 to –0.5% down spread , ± 0.25% center spread)
- I^2C interface.
- VDDL=2.5V,VDD=3.3V

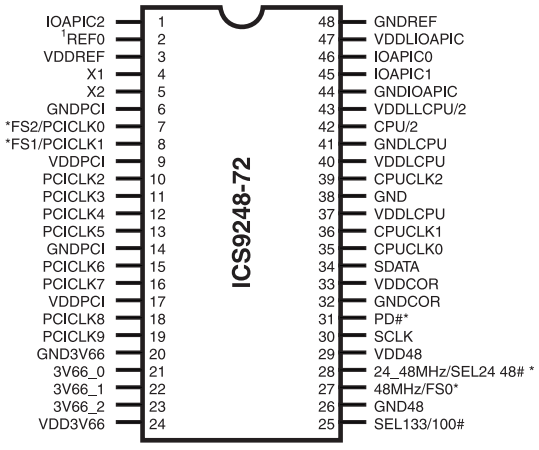
Key Specification

- CPU Output Jitter: <250ps
- CPU/2 Output Jitter. <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps
- Ref Output Jitter. <1000ps
- CPU Output Skew: <175ps
- IOAPIC Output Skew <250ps
- PCI Output Skew: <500ps
- 3V66 Output Skew <250ps
- CPU to 3V66 Output Offset: 0.0 - 1.5ns (CPU leads)
- 3V66 to PCI Output Offset: 1.5 - 4.0ns (3V66 leads)
- CPU to IOAPIC Output Offset 1.5 - 4.0ns (CPU leads)

Block Diagram



Pin Configuration



48-pin SSOP

* 250K ohm pull-up to VDD on indicated inputs.
1.These pins will have 2X drive strength

PRODUCT PREVIEW documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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Power Groups:

VDDREF, GNDREF = REF, X1, X2
GNDPCI, VDDPCI = PCICLK
VDD66, GND66 = 3V66
VDD48, GND48 = 48MHz
VDDCOR, GNDCOR = PLL Core
VDDLCPU/2 , GNDLCPU/2 = CPU/2
VDDLIOAPIC, GNDIOAPIC = IOAPIC

Pin Descriptions

Pin number	Pin name	Type	Description
1, 45, 46	IOAPIC[2:0]	Output	2.5V IOAPIC clock outputs
2	REF0	Output	3.3V, 14.318 MHz reference clock output.
3, 24, 29, 33	VDD	Power	3.3 V power
4	X1	Input	14.318 MHz crystal input
5	X2	Output	14.318 MHz crystal output
6, 14, 20, 26, 32	GND	Power	Ground
8, 7	FS [2:1]	IN	Frequency select pins. Latched Inputs determins the CPU & PCI frequencies.
	PCICLK [1:0]	Output	3.3 V PCI clock outputs, generating timing requirements for
9,17	VDDPCI	Power	3.3 V power for the PCI clock outputs
19, 18, 16, 15, 13, 12, 11, 10	PCICLK [9:2]	Output	3.3 V PCI clock outputs
23, 22, 21	3V66	Output	3.3 V 66 MHz clock output, fixed frequency clock typically used with AGP
25	SEL 133/100#	Input	control for the frequency of clocks at the CPU output pins. If logic "0" is used the 100 MHz frequency is selected. If Logic "1" is used, the 133 MHz frequency is selected. The PCI clock is multiplexed to run at 33.3 MHz for both selected cases.
27	FS0	IN	Frequency select pin. Latched Inputs determins the CPU & PCI frequencies.
	48 MHz	Output	3.3 V 48 MHz clock output, fixed frequency clock typically used with USB devices
28	SEL24/48	IN	48/24 MHz select option. Active low = 48 MHz output. Active High = 24 MHz
	24_48MHz#	Output	3.3V 48 or 24 MHz clock output, fixed frequency clock typically used with USB devices.
30	SCLK	IN	Clock input of I2C input
31	PD#	Input	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped.
34	SDATA	IN	Data input for I^2C serial input.
36, 35	CPUCLK [1:0]	0utput	2.5 V CPU and Host clock outputs
37, 40	VDDLCPU	Power	2.5 V power for the CPU and Host clock outputs
41	GNDLCPU/2	Power	Ground for the CPU and Host clock outputs
42	CPU/2	Output	output running at 1/2 CPU clock frequency.Synchronous to the CPU outputs.
43	VDDLCPU/2	Power	2.5 V power for the CPU/2 clock outputs
47	GNDLIOAPIC	Power	Ground for IOAPIC clocks
48	GNDREF	Power	Ground for 14.318 MHz reference clock outputs

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Functionality

V_{DD} = 3.3V±5%, V_{DDL} = 2.5V±5% TA= 0 to 70°C
Crystal (X1, X2) = 14.31818MHz

SEL133/100#	FS2 (MHz)	FS1 (MHz)	FS0 (MHz)	CPU (MHz)	CPU/2 (MHz)	PCI (MHz)	3V66 (MHz)	IOAPIC (MHz)
1	1	1	1	133.30	66.65	33.325	66.65	16.66
1	1	1	0	138.01	69.01	34.505	69.01	17.25
1	1	0	1	142.91	71.45	35.725	71.45	17.86
1	1	0	0	147.95	73.98	36.99	73.98	18.49
1	0	1	1	152.49	76.24	38.12	76.24	19.06
1	0	1	0	156.99	78.49	39.245	78.49	19.62
1	0	0	1	162.02	81.01	40.505	81.01	20.25
1	0	0	0	180.00	89.99	30.00	60.00	15.00
0	1	1	1	100.23	50.11	33.405	66.81	16.70
0	1	1	0	105.00	52.49	35	70.00	17.50
0	1	0	1	113.99	56.99	37.83	75.66	18.91
0	1	0	0	120.00	59.99	40.00	80.00	20.00
0	0	1	1	128.51	64.25	32.125	64.25	16.06
0	0	1	0	200.01	100.00	33.33	66.66	16.66
0	0	0	1	170.03	85.01	28.33	56.66	14.16
0	0	0	0	66.82	33.40	33.40	66.80	16.7

ICS9248-72 Power Management Features:

PD#	CPUCLK	CPU/2	IOAPIC	3V66	PCI	PCI_F	REF. 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON	ON

Note:
1. LOW means outputs held static LOW as per latency requirement next page.
2. On means active.
3. PD# pulled Low, impacts all outputs including REF and 48 MHz outputs.

Power Management Requirements:

Singal	Singal State	Latency
		No. of rising edges of PCICLK
PD#	1 (normal operation)	3mS
	0 (power down)	2max.

Note:
1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/ high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high to when the first valid clocks are dirven from the device.

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General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

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Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description									PWD
Bit (7:4)	Bit				CPUCLK	CPU/2	3V66	PCICLK	IOAPIC	0
	7	6	5	4						
	1	1	1	1	133.30	66.65	66.65	33.325	16.66	XXXX Note1
	1	1	1	0	138.01	69.01	69.01	34.505	17.25	
	1	1	0	1	142.91	71.45	71.45	35.725	17.86	
	1	1	0	0	147.95	73.98	73.98	36.99	18.49	
	1	0	1	1	152.49	76.24	76.24	38.12	19.06	
	1	0	1	0	156.99	78.49	78.49	39.245	19.62	
	1	0	0	1	162.02	81.01	81.01	40.505	20.25	
	1	0	0	0	180.00	89.99	60.00	30.00	15.00	
	0	1	1	1	100.23	50.11	66.81	33.405	16.70	
	0	1	1	0	105.00	52.49	70.00	35	17.50	
	0	1	0	1	113.99	56.99	75.66	37.83	18.91	
	0	1	0	0	120.00	59.99	80.00	40.00	20.00	
	0	0	1	1	128.51	64.25	64.25	32.125	16.06	
	0	0	1	0	200.01	100.00	66.66	33.33	16.66	
	0	0	0	1	170.03	85.01	56.66	28.33	14.16	
	0	0	0	0	66.82	33.40	66.80	33.40	16.7	
Bit3	0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 7:4									0
Bit2	0- Spread spectrum center spread type ±0.25% 1- Spread spectrum down spread type 0 to - 0.5%									1
Bit1	0- Normal 1- Spread spectrum enable									1
Bit0	0= Running 1= Tristate all outputs									0

Note1: Default at power-up will be for latched logic inputs to define frequency.

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Byte 1: CPU, CPU/2, 48MHz Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	27	1	48MHz
Bit 6	28	1	24_48 MHz
Bit 5	-	-	(Reserved)
Bit 4	42	1	CPU/2
Bit 3	-	-	(Reserved)
Bit 2	39	1	CPUCLK 2
Bit 1	36	1	CPUCLK 1
Bit 0	35	1	CPUCLK 0

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 2: PCICLK Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	16	1	PCICLK7
Bit 6	15	1	PCICLK6
Bit 5	13	1	PCICLK5
Bit 4	12	1	PCICLK4
Bit 3	11	1	PCICLK3
Bit 2	10	1	PCICLK2
Bit 1	8	1	PCICLK1
Bit 0	7	1	PCICLK0

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 3: 3V66, REF Register Active/Inactive
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	0	(Reserved)
Bit 6	23	1	3V66_2
Bit 5	22	1	3V66_1
Bit 4	21	1	3V66_0
Bit 3	-	X	FS2#
Bit 2	-	X	(SEL24 48#)#
Bit 1	19	1	PCICLK9
Bit 0	18	1	PCICLK8

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 4: IOAPIC, REF Register Active/Inactive
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7		0	(Reserved)
Bit 6	1	1	IOAPIC2
Bit 5	45	1	IOAPIC1
Bit 4	46	1	IOAPIC0
Bit 3	-	0	(Reserved)
Bit 2	-	X	FS0#
Bit 1	-	X	FS1#
Bit 0	2	1	REF (X2)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 5: CPU, IOAPIC Register Active/Inactive
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	0	(Reserved)
Bit 6	-	0	(Reserved)
Bit 5	-	0	(Reserved)
Bit 4	-	0	(Reserved)
Bit 3	-	0	(Reserved)
Bit 2	-	0	(Reserved)
Bit 1	-	0	(Reserved)
Bit 0	-	0	(Reserved)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

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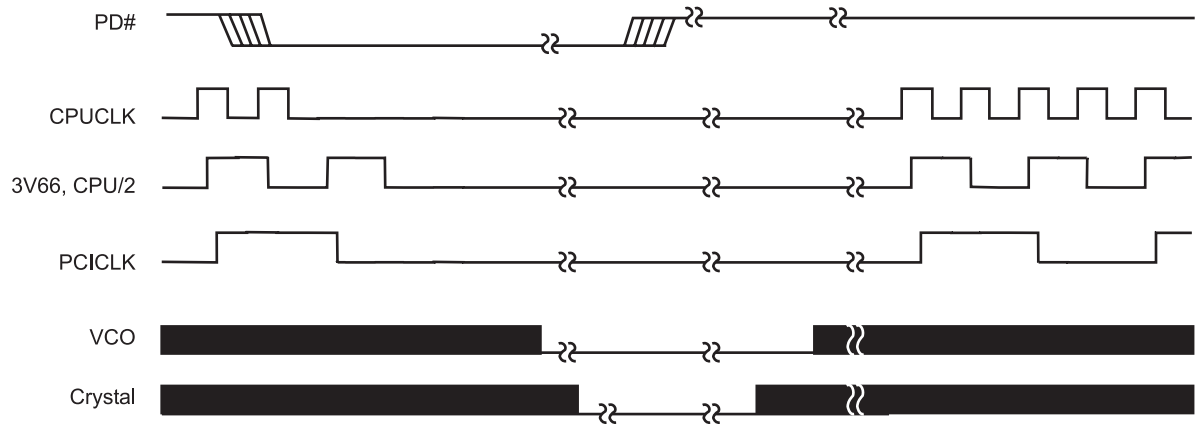
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.

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Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Offset

Group	Offset	Measurement Loads	Measure Points
CPU to 3V66	0.0-1.5ns CPU leads	CPU @ 20pF, 3V66 @ 30pF	CPU @1.25V, 3V66 @ 1.5V
3V66 to PCI	1.5-4.0ns 3V66 leads	3V66 @ 30pF, PCI @ 30pF	3V66 @ 1.5V, PCI @ 1.5V
CPU to IOAPIC	1.5-4.0ns CPU leads	CPU @ 20pF, IOAPIC @ 20pF	CPU @1.25V, IOAPIC @ 1.5V

Note: 1. All offsets are to be measured at rising edges.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%, VDDL=2.5 V± 5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors				µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors				µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select				mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND				µA
Input frequency	F_i	V_{DD} = 3.3 V;		14.318		MHz
Pin Inductance	L_{pin}			7		nH
Input Capacitance[1]	C_{IN}	Logic Inputs		5		pF
	C_{out}	Out put pin capacitance		6		pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.				mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

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Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Electrical Characteristics - CPU/2

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	ns
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

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Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2.0	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2.0	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

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Electrical Characteristics - 48M, REF

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/-5%; C_L = 10 -20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = 1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = -1 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH@MIN}$=1 V, $V_{OH@MAX}$= 3.135 V	-29		-23	mA
Output Low Current	I_{OL5}	$V_{OL@MIN}$=1.95 V, $V_{OL@MIN}$=0.4 V	29		27	mA
Duty Cycle	d_{t5}[1]	V_T = 1.5 V	45		55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Fixed Clocks			500	ps
	$t_{jcyc-cyc}$[1]	V_T = 1.5 V; Ref Clocks			1000	ps
Skew	T_{sk}	V_T = 1.5 V,Fixed Clocks			N/A	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C, V_{DDL} = 2.5 V +/-5%; C_L = 40 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 0.4 V, V_{OL} = 2.0 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45		55	ns
Skew	t_{sk2B}[1]	V_T = 1.25 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V			500	ps

[1]Guarenteed by design, not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

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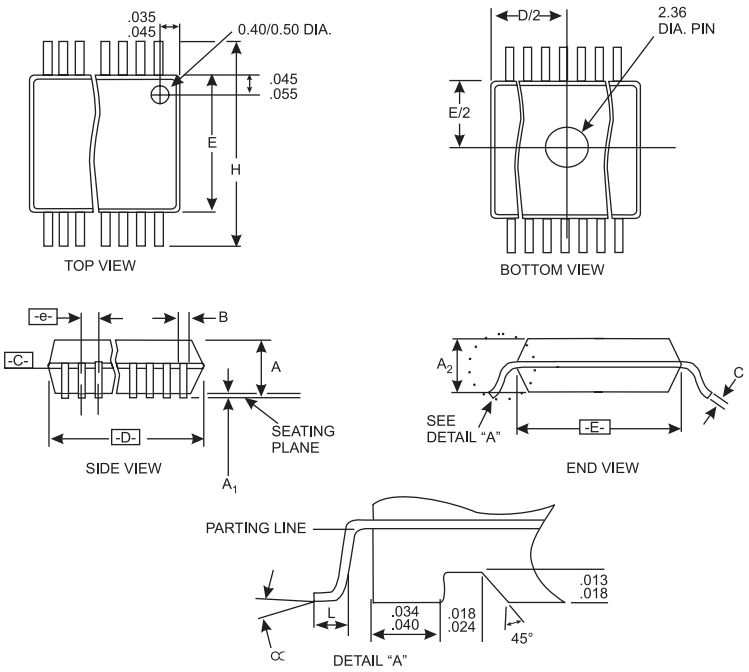

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

48 Pin SSOP Package

Ordering Information

ICS9248yF-72

Example:

ICS XXXX y F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator**
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

PRODUCT PREVIEW documents contain information on new products in the sampling or preproduction phase of development. Characteristic data and other specifications are subject to change without notice.

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