Integrated Circuit Systems, Inc.

ICS9248-73

Frequency Timing Generator for Pentium II Systems

General Description

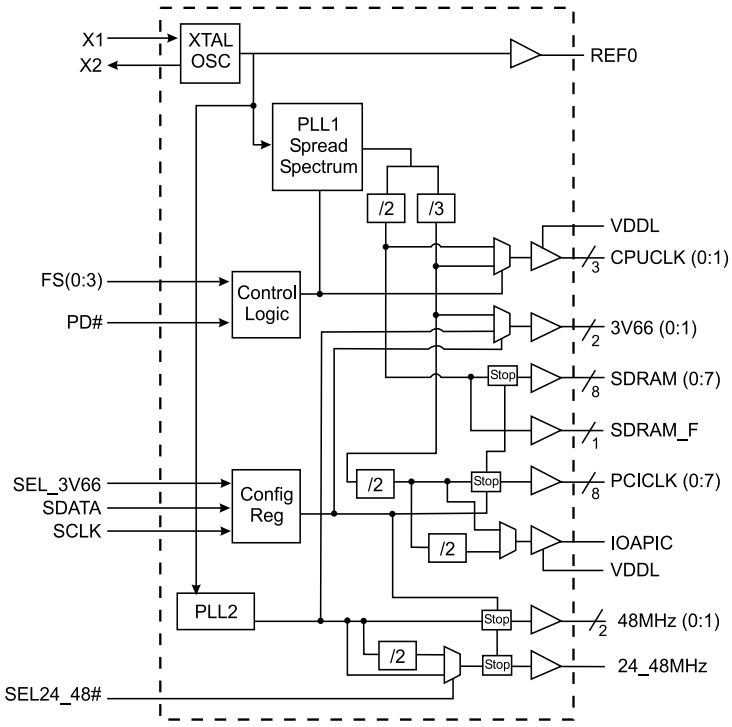
The **ICS9248-73** is a single chip clock for Intel Pentium II. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-73 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

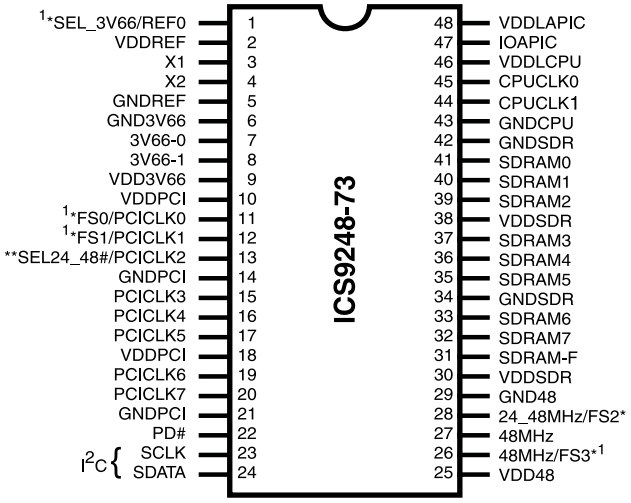
Features

- Generates the following system clocks:
  - 2 - CPUs @ 2.5V , up to 150MHz.
  - 1 - IOAPIC @ 2.5V, PCI/2MHz.
  - 9 - SDRAMs @ 3.3V, up to 150MHz.
  - 2 - 3V66 @ 3.3V, 2x PCI MHz.
  - 8 - PCIs @ 3.3V.
  - 2 - 48MHz, @ 3.3V fixed.
  - 1 - REF @ 3.3V, 14.318MHz.
  - 1 - 24_48MHz, @ 3.3V fixed.
- Supports spread spectrum modulation , down spread 0 to -0.5%, ±0.25% center spread.
- I^2C support for power management
- Efficient power management scheme through PD#
- Uses external 14.138 MHz crystal

Block Diagram



Pin Configuration



48-Pin 300 mil SSOP

*120K ohm pull-up to VDD on indicated inputs.
**60K ohm pull-up to VDD on indicated inputs.
1. These pins will have 2x drive strength

Power Groups

GNDREF, VDDREF = REF & Crystal
GND3V66, VDD3V66 = 3V66
GNDPCI, VDDPCI = PCICLK
GNDCOR, VDDCOR = PLL core
GND48, VDD48 = 48MHz
GNDSDR, VDDSDR = SDRAM
GNDLCPU, VDDLCPU = CPUCLK
GNDAPIC, VDDAPIC = IOAPIC

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I^2C is a trademark of Philips Corporation

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	SEL_3V66	IN	This pin selects the 3V66 output frequency.
	REF0	OUT	3.3V, 14.318MHz reference clock output.
2, 9, 10, 18, 25, 30, 38	VDD	PWR	3.3V power supply
3	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
5, 6, 14, 21, 29, 42, 34,	GND	PWR	Ground pins for 3.3V supply
7, 8	3V66 (0:1)	OUT	3.3V clock outputs for HUB running at 2XPCI MHz
11	PCICLK0	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
	FS0	IN	Logic input frequency select bit. Input latched at power on.
12	PCICLK1	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
	FS1	IN	Logic input frequency select bit. Input latched at power on.
13	PCICLK2	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
	SEL24_48#	IN	Logic input to select output.
15, 16, 17, 19, 20	PCICLK (3:7)	OUT	3.3V PCI clock outputs, with Synchronous CPUCLKS
22	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
23	SCLK	IN	Clock input of I^2C input
24	SDATA	IN	Data input for I^2C serial input.
26	48MHz	OUT	3.3V Fixed 48MHz clock output for USB
	FS3	IN	Logic input frequency select bit. Input latched at power on.
27	48MHz	OUT	3.3V Fixed 48MHz clock output for USB
28	24_48MHz	OUT	24 or 48MHz output controlled by SEL24_48#.
	FS2	IN	Logic input frequency select bit. Input latched at power on.
29	GND48	PWR	Ground for 48MHz outputs
31	SDRAM_F	OUT	3.3V free running 100MHz SDRAM not affected by I^2C
41, 40, 39, 37, 36, 35, 33, 32,	SDRAM (0:7)	OUT	3.3V output running 100MHz. All SDRAM outputs can be turned off through I^2C
43	GNDL	PWR	Ground for 2.5V power supply for CPU & APIC
45, 44	CPUCLK (0:1)	OUT	2.5V Host bus clock output, up to 150MHz depending on FS (0:3) pins Refer page 3.
47	IOAPIC	OUT	2.5V clock outputs running at PCI/2 MHz.
48, 46	VDDL	PWR	2.5V power suypply for CPU, IOAPIC

Frequency Selection

FS3	FS2	FS1	FS0	CPU MHz	SDRAM MHz	PCI MHz	3V66 MHz		IOAPIC MHz
							SEL_3V66=0	SEL_3V66=1	
0	0	0	0	100.23	100.23	33.41	66.82	66.82	16.70
0	0	0	1	100.90	100.90	33.63	67.26	67.26	16.81
0	0	1	0	105.00	105.00	35.00	70.00	70.00	17.50
0	0	1	1	66.89	100.33	33.44	66.89	66.89	16.72
0	1	0	0	120.00	120.00	40.00	64.00*	80.00	20.00
0	1	0	1	124.00	124.00	41.33	64.00*	82.66	20.67
0	1	1	0	133.30	133.30	44.43	64.00*	88.86	22.21
0	1	1	1	133.30	133.30	33.32	66.65	66.65	16.66
1	0	0	0	140.00	140.00	35.00	70.00	70.00	17.50
1	0	0	1	150.00	150.00	37.50	64.00*	75.00	18.75
1	0	1	0	114.99	114.99	38.33	64.00*	76.66	19.16
1	0	1	1	70.00	105.00	35.00	70.00	70.00	17.50
1	1	0	0	75.00	112.50	37.50	64.00*	75.00	18.75
1	1	0	1	83.31	124.96	41.65	64.00*	83.31	20.83
1	1	1	0	90.00	90.00	30.00	60.00	60.00	15.00
1	1	1	1	95.00	95.00	31.67	63.33	63.33	15.83

Note:
* These output frequencies are not synchronous to CPUCLK and do not have spread spectrum modulation.

Clock Enable Configuration

PD#	CPUCLK	SDRAM	IOAPIC	66MHz	PCICLK	REF, 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

Byte 0: Functionality and frequency select register (Default=0)
(1 = enable, 0 = disable)

Bit	Description							PWD
Bit 7	0 - ±0.25% Center Sperad Spectrum							
	1-Down Spread Spectrum 0 to -0.5%							0
Bit (2, 6:4)	Bit (2, 6:4)	CPUCLK MHz	SDRAM MHz	PCICLK MHz	3V66 MHz		IOAPIC MHz	XXXX Note 1
					SEL_3V66=0	SEL_3V66=1		
	0000	100.23	100.23	33.41	66.82	66.82	16.70	
	0001	100.90	100.90	33.63	67.26	67.26	16.81	
	0010	105.00	105.00	35.00	70.00	70.00	17.50	
	0011	66.89	100.33	33.44	66.89	66.89	16.72	
	0100	120.00	120.00	40.00	64.00*	80.00	20.00	
	0101	124.00	124.00	41.33	64.00*	82.66	20.67	
	0110	133.30	133.30	44.43	64.00*	88.86	22.21	
	0111	133.30	133.30	33.32	66.65	66.65	16.66	
	1000	140.00	140.00	35.00	70.00	70.00	17.50	
	1001	150.00	150.00	37.50	64.00*	75.00	18.75	
	1010	114.99	114.99	38.33	64.00*	76.66	19.16	
	1011	70.00	105.00	35.00	70.00	70.00	17.50	
	1100	75.00	112.50	37.50	64.00*	75.00	18.75	
	1101	83.31	124.96	41.65	64.00*	83.31	20.83	
	1110	90.00	90.00	30.00	60.00	60.00	15.00	
	1111	95.00	95.00	31.67	63.33	63.33	15.83	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2, 6:4							0
Bit 1	0 - Normal 1 - Spread spectrum enable							0
Bit 0	0 - Running 1 - Tristate all outputs							0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, Bit 2, 6:4 are default to 0000.

* These output frequencies are not synchronous to CPUCLK and do not have spread spectrum modulation.

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	X	FS3#
Bit 6	-	X	FS0#
Bit 5	-	X	FS2#
Bit 4	28	1	24-48MHz
Bit 3	27	1	48MHz
Bit 2	26	1	48MHz
Bit 1	-	0	(Reserved)
Bit 0	31	1	SDRAM_F

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	32	1	SDRAM7
Bit 6	33	1	SDRAM6
Bit 5	35	1	SDRAM5
Bit 4	36	1	SDRAM4
Bit 3	37	1	SDRAM3
Bit 2	39	1	SDRAM2
Bit 1	40	1	SDRAM1
Bit 0	41	1	SDRAM0

Byte 3: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	20	1	PCICLK7
Bit 6	19	1	PCICLK6
Bit 5	17	1	PCICLK5
Bit 4	16	1	PCICLK4
Bit 3	15	1	PCICLK3
Bit 2	13	1	PCICLK2
Bit 1	12	1	PCICLK1
Bit 0	11	1	PCICLK0

Byte 4: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	PWD	Description
Bit 7	-	0	(Reserved)
Bit 6	7	1	3V66_0
Bit 5	8	1	3V66_1
Bit 4	-	X	SEL_3V66#
Bit 3	47	1	IOAPIC
Bit 2	-	X	FS1#
Bit 1	44	1	CPUCLK1
Bit 0	45	1	CPUCLK0

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Absolute Maximum Ratings

Core Supply Voltage . . . . . 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP66}$	Select @ 66MHz; Max discrete cap loads		300	380	mA
	$I_{DD3.3OP100}$	Select @ 100MHz; Max discrete cap loads		300		
	$I_{DD2.5OP66}$	Select @ 66MHz; Max discrete cap loads		14	70	mA
	$I_{DD2.5OP100}$	Select @ 100MHz; Max discrete cap loads		21	100	
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; PWRDWN# = 0		5	10	mA
Input frequency	F_i	V_{DD} = 3.3 V	12	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{Trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_S	From 1st crossing to 1% target Freq.		1	3	ms
Clk Stabilization[1]	T_{Stab}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Delay	t_{PZH}, t_{PZH}	Output enable delay (all outputs)	1		10	ns
	t_{PLZ}, t_{PZH}	Output diable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.36		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA		0.33	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-34	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	25		mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.5	2	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.4	1.8	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V; Freq>= 140MHz	40	48	50	%
		V_T = 1.25 V; Freq< 140MHz	43	48	53	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		50	175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V; CPU @ 66.8 MHz		500	250	ps
		V_T = 1.25 V; CPU @ 100.23 MHz		130		

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L =30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.18	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-55	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	43		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.55	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.4	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	48	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		50	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V; 3V66 Freq > 75MHz		100	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V; 3V66 Freq < 75MHz		350	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH4B}	I_{OH} = -8 mA	2	2.3		V
Output Low Voltage	V_{OL4B}	I_{OL} = 12 mA		0.36	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-24	-16	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	23		mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.4	2.1	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.45	2.2	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc4B}$	V_T = 1.25 V		140	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -25 mA	2.4	2.9		V
Output Low Voltage	V_{OL3}	I_{OL} = 20 mA		0.32	0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V		-73	-40	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8 V	41	50		mA
Rise Time	T_{r3}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	0.95	2	ns
Fall Time	T_{f3}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1	2	ns
Duty Cycle	D_{t3}[1]	V_T = 1.5 V	45	53	55	%
Skew[1]	T_{sk1}	V_T = 1.5 V		85	250	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc3B}$[1]	V_T = 1.25 V		110	250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz/FS3; REF0

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4	3.1		V
Output Low Voltage	V_{OL5}	I_{OL} = 10 mA		0.19	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-55	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	25	42		mA
Rise Time[1]	t_{r5}	VOL = 0.4 V, VOH = 2.4 V		1.1	4	ns
Fall Time[1]	t_{f5}	VOH = 2.4 V, VOL = 0.4 V		1	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V, 48MHz/FS3	45	51	55	%
Duty Cycle[1]	d_{t5}	VT = 1.5 V, REF	45	52	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, 48MHz/FS3		190	500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, REF		310	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz; 24_48MHz

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4	2.9		V
Output Low Voltage	V_{OL5}	I_{OL} = 10 mA		0.35	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-28	-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1.5	2.4	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1.5	2.2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	50	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V		240	500	ps

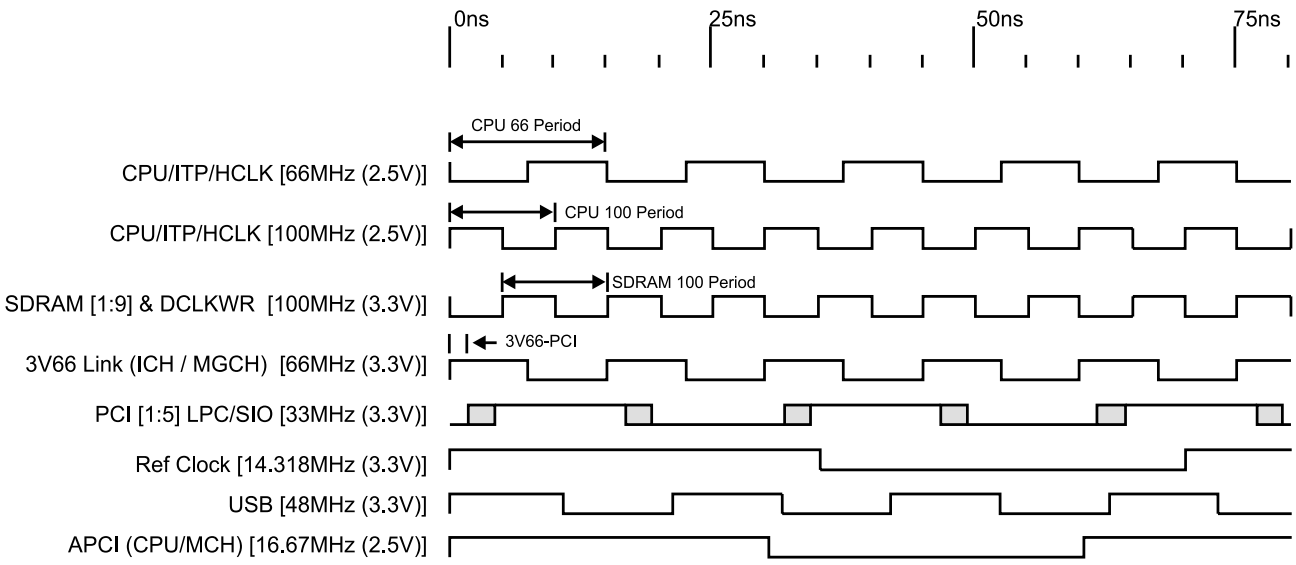
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 60 pF for PCI0 & PCI1, CL = 30 pF for other PCIs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	IOH = -11 mA; Pci0 & Pci1	2.4	3.2		V
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA; Pci0 & Pci1		0.12	0.4	V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.2	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V; Pci0 & Pci1		-110	-22	mA
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-55	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V; Pci0 & Pci1	25	82		mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25	42		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V; PCI0:1, C_L=60pF	0.5	1.5	2.3	ns
		V_{OL} = 0.4 V, V_{OH} = 2.4 V; PCI2:7	0.5	1.7	2.3	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V; PCI0:1, C_L=60pF	0.5	1.4	2	ns
		V_{OH} = 2.4 V, V_{OL} = 0.4 V; PCI2:7	0.5	1.7	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V; C_L=60pF for Pci0 & PCI1		545	500	ps
		V_T = 1.5 V; C_L=50pF for Pci0 & PCI1		360		ps
		V_T = 1.5 V; C_L=40pF for Pci0 & PCI1		455		ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		130	500	ps

[1]Guaranteed by design, not 100% tested in production.



Group Offset Waveforms

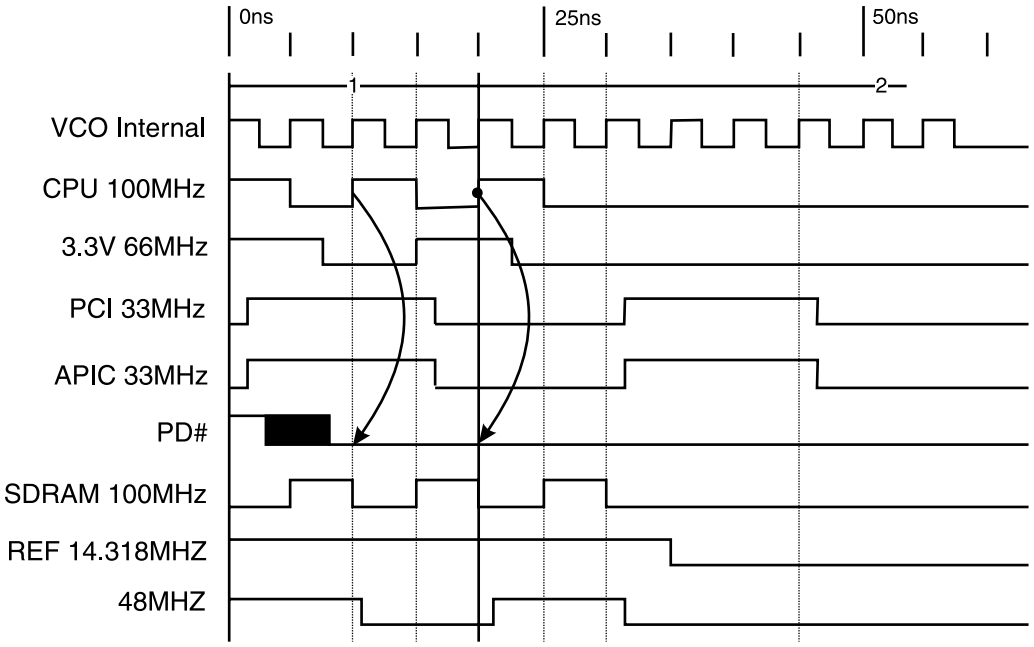
Group Skews at common Transition Edges

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)
CL = 20 pF for CPU and IOAPIC
CL = 50 pF for PCI0 & PCI1, CL = 30 pF for other PCIs, SDRAM and 3V66

GROUP	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CPU to SDRAM	$t_{CPU-SDRAM}$	V_T = 1.5 V; V_{TL} = 1.25 V SDRAM leads CPU by 2.5ns for CPU66 CPU leads SDRAM by 5.0ns for CPU100	0	100	500	ps
CPU to 3V66	$t_{CPU-3V66}$	V_T = 1.5 V; V_{TL} = 1.25 V CPU leads 3V66 by 7.5ns for CPU66 CPU leads 3V66 by 0.0ns for CPU100	0	100	500	ps
IOAPIC to PCI	$t_{IOAPIC-PCI}$	VT = 1.5 V; V_{TL} = 1.25 V	0	360	500	ps
3V66 to PCI	$t_{3V66-PCI}$	V_T = 1.5 V	1.5	2.5	4	ns

Guaranteed by design, not 100% tested in production.

Power Down Waveform



Note

1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-73 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

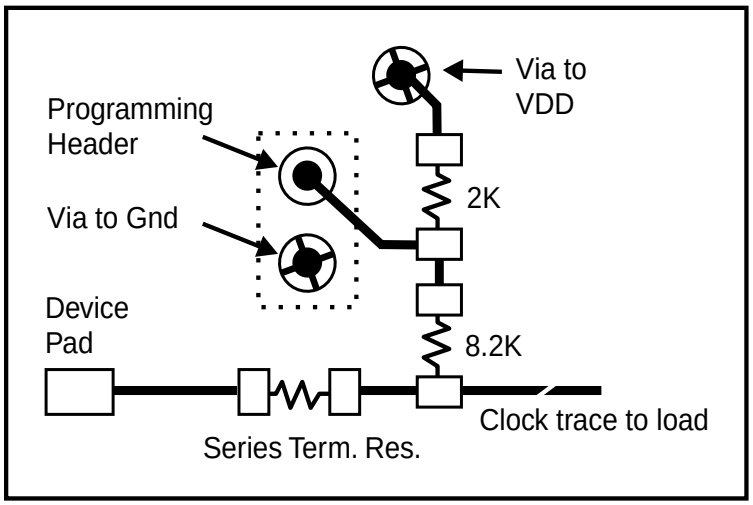
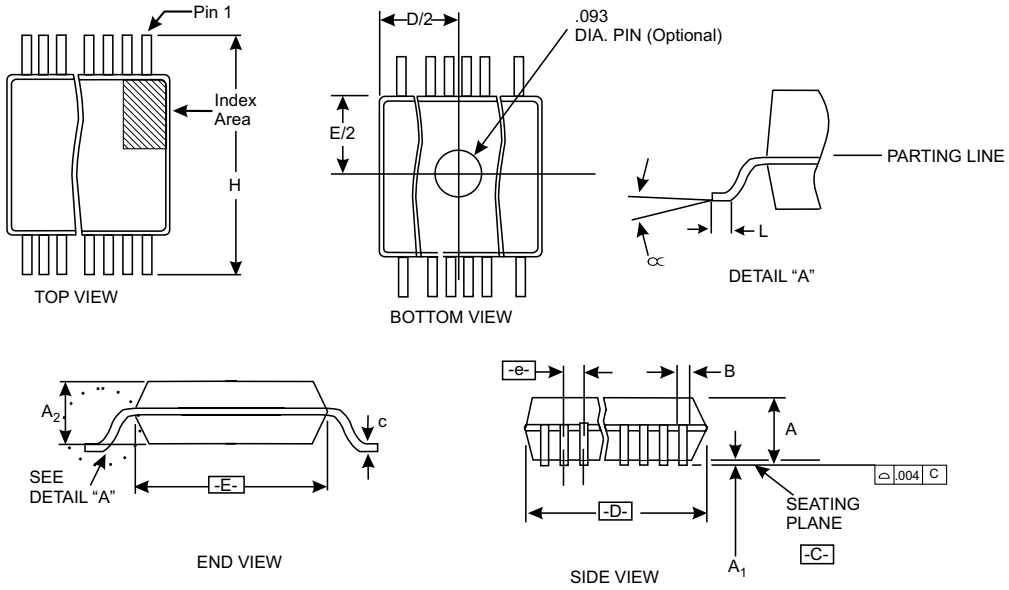


Fig. 1



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.087	.090	.094					
B	.008	-	.0135					
c	.005	-	.010					
D	See Variations							
E	.291	.295	.299	"For current dimensional specifications, see JEDEC 95."				
e	0.025 BSC							
H	.395	-	.420					
h	.010	.013	.016					
L	.020	-	.040	Dimensions in inches				
N	See Variations							
∝	0°	-	8°					

48 Pin 300 mil SSOP Package

Ordering Information

ICS9248yF-73-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device