



Frequency Generator for SIS 735/740 with AMD K7 Processor

Recommended Application:

Main system clock for SIS 735/740 with AMD K7 chipset.

Output Features:

- 1 - CPU @ 2.5V
- 1 - Differential pair open drain CPU clock
- 1 - IOAPIC @ 2.5V
- 1 - SDRAM @ 3.3V
- 6- PCI @3.3V
- 2 - AGP @ 3.3V
- 1- 48MHz, @3.3V fixed
- 1- 24/48MHz, @3.3V selectable by I²C (Default is 24MHz)
- 2- REF @3.3V, 14.318MHz

Features:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I²C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Skew Specifications:

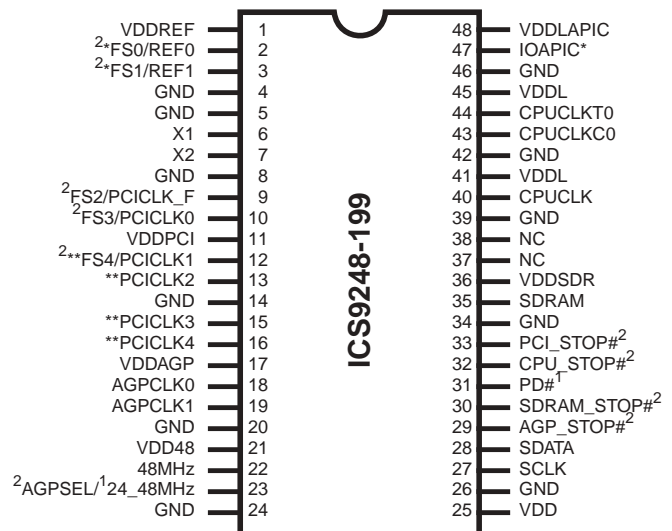
- CPU - CPU: < 175ps
- PCI - PCI: < 500ps
- CPU - SDRAM: < 250ps
- AGP - AGP: <175ps
- CPU - AGP, PCI: 1-4ns

Frequency Table

Bit 2	Bit 7	Bit 6	Bit 5	Bit 4	CPU	SDRAM	PCI	AGP SEL = 0	AGP SEL = 1
FS4	FS3	FS2	FS1	FS0					
0	0	0	0	0	66.66	66.66	33.33	66.66	50.00
0	0	0	0	1	100.00	100.00	33.33	66.66	50.00
0	0	0	1	0	166.66	166.66	33.33	66.66	55.60
0	0	0	1	1	133.33	133.33	33.33	66.66	50.00
0	0	1	0	0	66.66	100.00	33.33	66.66	50.00
0	0	1	0	1	100.00	66.66	33.33	66.66	50.00
0	0	1	1	0	100.00	133.33	33.33	66.66	50.00
0	0	1	1	1	133.33	100.00	33.33	66.66	50.00
0	1	0	0	0	112.00	112.00	33.60	67.20	56.00
0	1	0	0	1	124.00	124.00	31.00	62.00	46.50
0	1	0	1	0	138.00	138.00	34.50	69.00	46.00
0	1	0	1	1	150.00	150.00	30.00	60.00	50.00
0	1	1	0	0	100.00	166.66	31.25	62.50	50.00
0	1	1	0	1	133.33	166.66	33.33	66.66	55.30
0	1	1	1	0	150.00	100.00	30.00	60.00	50.00
0	1	1	1	1	160.00	120.00	30.00	60.00	48.00
1	0	0	0	0	90.00	90.00	30.00	60.00	45.00
1	0	0	0	1	100.90	100.90	33.63	67.27	50.45
1	0	0	1	0	103.00	103.00	34.33	68.67	51.50
1	0	0	1	1	133.90	133.90	33.48	68.67	51.56
1	0	1	0	0	137.33	103.00	34.33	66.95	51.45
1	0	1	0	1	137.33	137.33	34.33	68.67	50.21
1	0	1	1	0	100.90	133.90	33.48	66.95	50.21
1	0	1	1	1	133.90	100.90	33.48	66.95	50.21
1	1	0	0	0	107.00	107.00	35.66	71.33	53.50
1	1	0	0	1	107.00	142.66	35.66	71.33	53.50
1	1	0	1	0	142.66	142.66	35.66	71.33	53.50
1	1	0	1	1	110.00	110.00	36.66	73.33	55.00
1	1	1	0	0	110.00	146.66	36.66	73.33	55.00
1	1	1	0	1	146.66	146.66	36.66	73.33	55.00
1	1	1	1	0	166.70	125.00	31.25	66.68	55.57
1	1	1	1	1	200.00	200.00	33.33	66.66	50.00

Note: Please see full table on page 4.

Pin Configuration



48-Pin 300mil SSOP

- * These are double strength.
- ** (1X/2X) have single or double strength to drive 2 loads.
- 1. Internal pull-up, of 120K to V_{DD}.
- 2. These inputs have a 120K pull down to GND.



Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 11, 17, 21, 25, 36	VDD	PWR	3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output.
2	FS0	IN	Frequency select pin.
	REF0	OUT	14.318 MHz reference clock.
3	FS1	IN	Frequency select pin.
	REF1	OUT	14.318 MHz reference clock.
4, 5, 8, 14, 20, 24, 26, 34, 39, 42, 46	GND	PWR	Ground pin for outputs.
6	X1	IN	Crystal input, nominally 14.318MHz.
7	X2	OUT	Crystal output, nominally 14.318MHz.
9	FS2	IN	Frequency select pin.
	PCICLK_F	OUT	PCI clock output, not affected by PCI_STOP#.
10	FS3	IN	Frequency select pin.
	PCICLK0	OUT	PCI clock output.
12	FS4	IN	Frequency select pin.
	PCICLK1	OUT	PCI clock output.
16, 15, 13	PCICLK (4:2)	OUT	PCI clock outputs.
19, 18	AGPCLK (1:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
22	48MHz	OUT	48MHz output clock.
23	AGPSEL	IN	AGP frequency select pin.
	24_48MHz	OUT	Clock output for super I/O/USB default is 24MHz.
27	SCLK	IN	Clock pin of I ² C circuitry 5V tolerant.
28	SDATA	I/O	Data pin for I ² C circuitry 5V tolerant.
29	AGP_STOP#	IN	Stops all AGP clocks besides the AGP_F clocks at logic 0 level, when input low.
30	SDRAM_STOP#	IN	Stops all SDRAM clocks at logic 0 level, when input low (when MODE active).
31	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
32	CPU_STOP#	IN	Stops all CPUCLKs clocks at logic 0 level, when input low.
33	PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low.
35	SDRAM	OUT	SDRAM clock output.
37, 38	NC	-	No connect pins.
40	CPUCLK	OUT	CPU clock output.
41, 45, 48	VDDL	PWR	Supply for CPU and IOAPIC clocks at 2.5V nominal.
43	CPUCLKC0	OUT	Complementary clocks of differential pair CPU outputs. This clock is 180° out of phase with SDRAM clocks. These open drain outputs need an external 1.5V pull-up.
44	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. This clock is in phase with SDRAM clocks. This open drain output needs an external 1.5V pull-up.
47	IOAPIC	OUT	2.5V clock output.

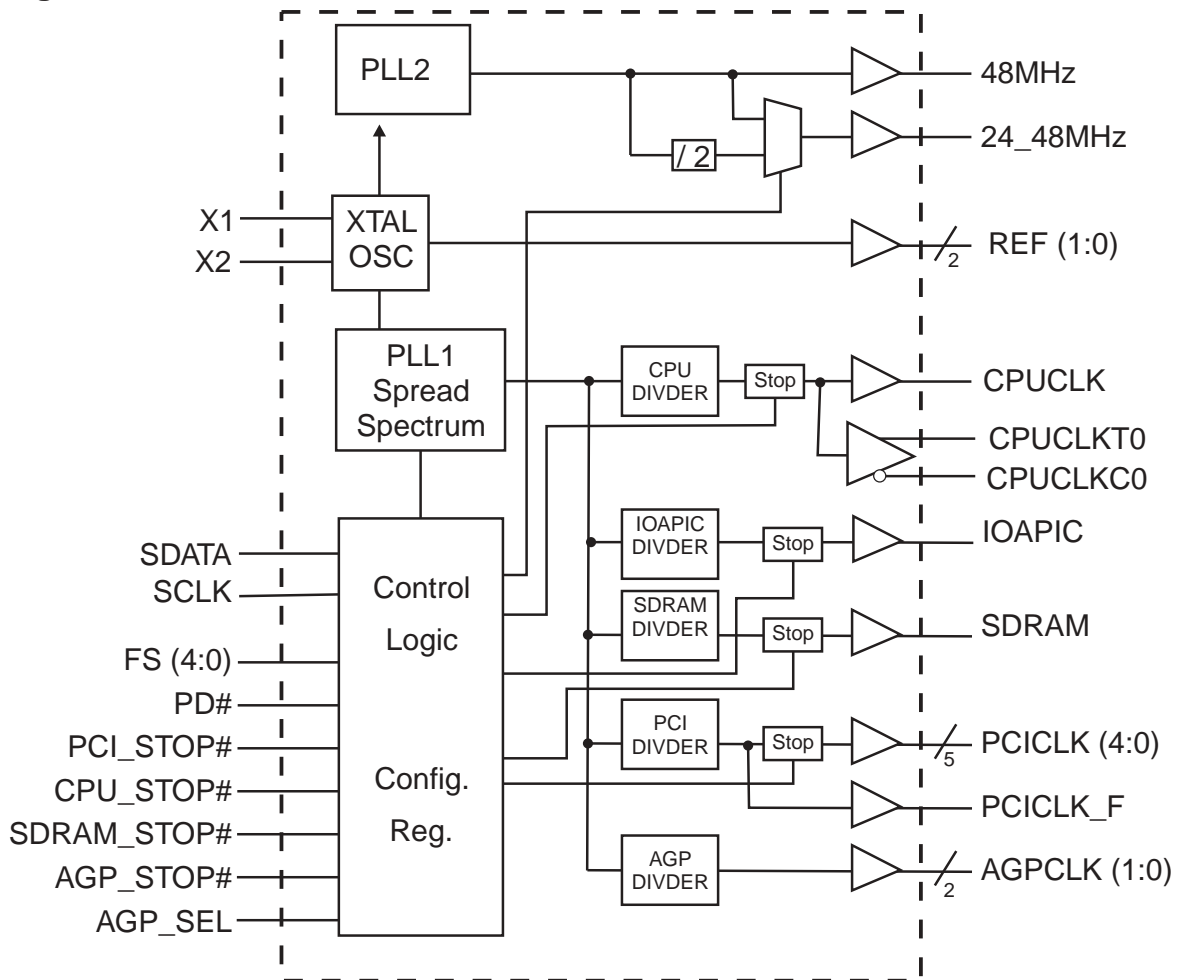


General Description

The ICS9248-199 is a single chip clock solution for desktop designs using the Intel Brookdale chipset with PC133 or DDR memory. It provides all necessary clock signals for such a system.

The ICS9248-199 is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I²C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Power Groups

- VDDCPU = CPU
- VDDPCI = PCICLK_F, PCICLK
- VDDSDR = SDRAM
- VDD48 = 48MHz, 24MHz, fixed PLL
- VDDA = Core, PLL, X1, X2
- VDDAGP=AGP, REF

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Serial Configuration Command Bitmap

Bytes 0-3: Are reserved for external clock buffer.

Byte4: Functionality and Frequency Select Register (default = 0)

Bit	Description					CPU	SDRAM	PCI	AGP SEL = 0	AGP SEL = 1	Spread Percentage	PWD
	Bit 2 FS4	Bit 7 FS3	Bit 6 FS2	Bit 5 FS1	Bit 4 FS0							
Bit 2 Bit 7:4	0	0	0	0	0	66.66	66.66	33.33	66.66	50.00	0 to -0.5% Down Spread	0000 Note1
	0	0	0	0	1	100.00	100.00	33.33	66.66	50.00	0 to -0.5% Down Spread	
	0	0	0	1	0	166.66	166.66	33.33	66.66	55.60	+/- 0.25% Center Spread	
	0	0	0	1	1	133.33	133.33	33.33	66.66	50.00	0 to -0.5% Down Spread	
	0	0	1	0	0	66.66	100.00	33.33	66.66	50.00	0 to -0.5% Down Spread	
	0	0	1	0	1	100.00	66.66	33.33	66.66	50.00	0 to -0.5% Down Spread	
	0	0	1	1	0	100.00	133.33	33.33	66.66	50.00	0 to -0.5% Down Spread	
	0	0	1	1	1	133.33	100.00	33.33	66.66	50.00	0 to -0.5% Down Spread	
	0	1	0	0	0	112.00	112.00	33.60	67.20	56.00	+/- 0.25% Center Spread	
	0	1	0	0	1	124.00	124.00	31.00	62.00	46.50	+/- 0.25% Center Spread	
	0	1	0	1	0	138.00	138.00	34.50	69.00	46.00	+/- 0.25% Center Spread	
	0	1	0	1	1	150.00	150.00	30.00	60.00	50.00	+/- 0.25% Center Spread	
	0	1	1	0	0	100.00	166.66	31.25	62.50	50.00	0 to -0.5% Down Spread	
	0	1	1	0	1	133.33	166.66	33.33	66.66	55.30	0 to -0.5% Down Spread	
	0	1	1	1	0	150.00	100.00	30.00	60.00	50.00	+/- 0.25% Center Spread	
	0	1	1	1	1	160.00	120.00	30.00	60.00	48.00	+/- 0.25% Center Spread	
	1	0	0	0	0	90.00	90.00	30.00	60.00	45.00	+/- 0.25% Center Spread	
	1	0	0	0	1	100.90	100.90	33.63	67.27	50.45	+/- 0.25% Center Spread	
	1	0	0	1	0	103.00	103.00	34.33	68.67	51.50	+/- 0.25% Center Spread	
	1	0	0	1	1	133.90	133.90	33.48	68.67	51.56	+/- 0.25% Center Spread	
1	0	1	0	0	137.33	103.00	34.33	66.95	51.45	+/- 0.25% Center Spread		
1	0	1	0	1	137.33	137.33	34.33	68.67	50.21	+/- 0.25% Center Spread		
1	0	1	1	0	100.90	133.90	33.48	66.95	50.21	+/- 0.25% Center Spread		
1	0	1	1	1	133.90	100.90	33.48	66.95	50.21	+/- 0.25% Center Spread		
1	1	0	0	0	107.00	107.00	35.66	71.33	53.50	+/- 0.25% Center Spread		
1	1	0	0	1	107.00	142.66	35.66	71.33	53.50	+/- 0.25% Center Spread		
1	1	0	1	0	142.66	142.66	35.66	71.33	53.50	+/- 0.25% Center Spread		
1	1	0	1	1	110.00	110.00	36.66	73.33	55.00	+/- 0.25% Center Spread		
1	1	1	0	0	110.00	146.66	36.66	73.33	55.00	+/- 0.25% Center Spread		
1	1	1	0	1	146.66	146.66	36.66	73.33	55.00	+/- 0.25% Center Spread		
1	1	1	1	0	166.70	125.00	31.25	66.68	55.57	+/- 0.25% Center Spread		
1	1	1	1	1	200.00	200.00	33.33	66.66	50.00	+/- 0.25% Center Spread		
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit , 2 7:4											0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled											1
Bit 0	0 - Running 1- Tristate all outputs											0

Note1:
Default at power-up will be for latched logic inputs to define frequency, as defined by Bit 3.

Note: PWD = Power-Up Default

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Byte 5: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	23	1	24M_48M (1: On, 0: Off)
Bit 6	2,3	0	REF_1X2X_Control (0: 1x, 1: 2x)
Bit 5	47	1	APIC1X2X_Control (0: 1x, 1: 2x)
Bit 4	19	1	AGPCLK1 (Act/Inactive)
Bit 3	18	1	AGPCLK0 (Act/Inactive)
Bit 2	-	0	IOAPIC Select (0:16.67 MHz, 1:33.33 MHz)
Bit 1	23	1	24M_48M Select (1: 24 MHz, 0: 48 MHz)
Bit 0	22	0	Reserved

Byte 6: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	19	1	Reserved
Bit 6	18	1	Reserved
Bit 5	16	1	PCICLK4 (Act/Inactive)
Bit 4	15	1	PCICLK3 (Act/Inactive)
Bit 3	13	1	PCICLK2 (Act/Inactive)
Bit 2	12	1	PCICLK1 (Act/Inactive)
Bit 1	10	1	PCICLK0 (Act/Inactive)
Bit 0	23	X	AGPSEL (read back)

Byte 7: Control, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	12	0	PCLCLK1_1X2X_Control (1: 2x, 0: 1x)
Bit 6	13	0	PCLCLK2_1X2X_Control (1: 2x, 0: 1x)
Bit 5	10	X	FS3 (read back)
Bit 4	9	X	FS2 (read back)
Bit 3	3	X	FS1 (read back)
Bit 2	2	X	FS0 (read back)
Bit 1	15	X	PCLCLK3_1X2X_Control (1: 2x, 0: 1x)
Bit 0	16	X	PCLCLK4_1X2X_Control (1: 2x, 0: 1x)


Byte 8: Byte Count Read Back Register

Bit	Name	PWD	Description
Bit 7	Byte7	0	Note: Writing to this register will configure byte count and how many bytes will be read back, default is $0F_H = 15$ bytes.
Bit 6	Byte6	0	
Bit 5	Byte5	0	
Bit 4	Byte4	0	
Bit 3	Byte3	1	
Bit 2	Byte2	1	
Bit 1	Byte1	1	
Bit 0	Byte0	1	

Byte 9: Watchdog Timer Count Register*

Bit	Name	PWD	Description
Bit 7	WD7	0	The decimal representation of these 8 bits correspond to $X \cdot 290ms$ the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is $16 \cdot 290ms = 4.6$ seconds.
Bit 6	WD6	0	
Bit 5	WD5	0	
Bit 4	WD4	1	
Bit 3	WD3	0	
Bit 2	WD2	0	
Bit 1	WD1	0	
Bit 0	WD0	0	

Byte 10: Programming Enable bit 8 Watchdog Control Register*

Bit	Name	PWD	Description
Bit 7	Program Enable	0	Programming Enable bit 0 = no programming. Frequencies are selected by HW latches or Byte0 1 = enable all I ² C programing.
Bit 6	WD Enable	0	Watchdog Enable bit
Bit 5	WD Alarm	0	Watchdog Alarm Status 0 = normal 1= alarm status
Bit 4	SF4	0	Watchdog safe frequency bits. Writing to these bits will configure the safe frequency corresponding to Byte 0 Bit 2, 7:4 table
Bit 3	SF3	1	
Bit 2	SF2	0	
Bit 1	SF1	0	
Bit 0	SF0	0	

Byte 11: VCO Frequency M Divider (Reference divider) Control Register*

Bit	Name	PWD	Description
Bit 7	Ndiv 8	X	N divider bit 8
Bit 6	Mdiv 6	X	The decimal representation of Mdiv (6:0) correspond to the reference divider value. Default at power up is equal to the latched inputs selection.
Bit 5	Mdiv 5	X	
Bit 4	Mdiv 4	X	
Bit 3	Mdiv 3	X	
Bit 2	Mdiv 2	X	
Bit 1	Mdiv 1	X	
Bit 0	Mdiv 0	X	

* These bytes are not available in ICS9248A/B/CF-199.
Programmable features on these bytes are only for ICS9248D/EF-199.



Byte 12: VCO Frequency N Divider (VCO divider) Control Register*

Bit	Name	PWD	Description
Bit 7	Ndiv 7	X	The decimal representation of Ndiv (8:0) correspond to the VCO divider value. Default at power up is equal to the latched inputs selecton. Notice Ndiv 8 is located in Byte 11.
Bit 6	Ndiv 6	X	
Bit 5	Ndiv 5	X	
Bit 4	Ndiv 4	X	
Bit 3	Ndiv 3	X	
Bit 2	Ndiv 2	X	
Bit 1	Ndiv 1	X	
Bit 0	Ndiv 0	X	

Byte 13: Spread Spectrum Control Register*

Bit	Name	PWD	Description
Bit 7	SS 7	X	The Spread Spectrum (12:0) bit will program the spread precentage. Spread precent needs to be calculated based on the VCO frequency, spreading profile, spreading amount and spread frequency. It is recommended to use ICS software for spread programming. Default power on is latched FS divider.
Bit 6	SS 6	X	
Bit 5	SS 5	X	
Bit 4	SS 4	X	
Bit 3	SS 3	X	
Bit 2	SS 2	X	
Bit 1	SS 1	X	
Bit 0	SS 0	X	

Byte 14: Spread Spectrum Control Register*

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	Reserved	X	Reserved
Bit 4	SS 12	X	Spread Spectrum Bit 12
Bit 3	SS 11	X	Spread Spectrum Bit 11
Bit 2	SS 10	X	Spread Spectrum Bit 10
Bit 1	SS 9	X	Spread Spectrum Bit 9
Bit 0	SS 8	X	Spread Spectrum Bit 8

Byte 15: Output Divider Control Register*

Bit	Name	PWD	Description
Bit 7	SD Div 3	X	SDRAM clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 6	SD Div 2	X	
Bit 5	SD Div 1	X	
Bit 4	SD Div 0	X	
Bit 3	CPU Div 3	X	CPU clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	CPU Div 2	X	
Bit 1	CPU Div 1	X	
Bit 0	CPU Div 0	X	

* These bytes are not available in ICS9248A/B/CF-199. Programmable features on these bytes are only for ICS9248D/EF-199.



Byte 16: Output Divider Control Register*

Bit	Name	PWD	Description
Bit 7	PCI Div 3	X	PCI clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 2. Default at power up is latched FS divider.
Bit 6	PCI Div 2	X	
Bit 5	PCI Div 1	X	
Bit 4	PCI Div 0	X	
Bit 3	AGP 50MHz Div 3	X	AGP clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to Table 1. Default at power up is latched FS divider.
Bit 2	AGP 50MHz Div 2	X	
Bit 1	AGP 50MHz Div 1	X	
Bit 0	AGP 50MHz Div 0	X	

Byte 17: Output Divider Control Register*

Bit	Name	PWD	Description
Bit 7	Reserved	X	Reserved
Bit 6	Reserved	X	Reserved
Bit 5	SD_INV	X	SDRAM Phase Inversion bit
Bit 4	CPU_INV	X	CPUCLK Phase Inversion bit
Bit 3	AGP 66MHz Div 3	X	AGP clock divider ratio can be configured via these 4 bits individually. For divider selection table refer to table 1. Default at power up is latched FS divider.
Bit 2	AGP 66MHz Div 2	X	
Bit 1	AGP 66MHz Div 1	X	
Bit 0	AGP 66MHz Div 0	X	

Table 1

Div (3:2)	00	01	10	11
Div (1:0)				
00	/2	/4	/8	/16
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

Table 2

Div (3:2)	00	01	10	11
Div (1:0)				
00	/4	/8	/16	/32
01	/3	/6	/12	/24
10	/5	/10	/20	/40
11	/7	/14	/28	/56

* These bytes are not available in ICS9248A/B/CF-199. Programmable features on these bytes are only for ICS9248D/EF-199.



Byte 18: Group Skew Control Register*

Bit	Name	PWD	Description
Bit 7	CPU_Skew 1	1	These 2 bits delay the CPUclocks with respect to all other clocks. 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 6	CPU_Skew 0	0	
Bit 5	SD_Skew 1	0	These 2 bits delay the SDRAM_OUT with respect to CPUCLK 00 = 0ps 01 = 250ps 10 = 500ps 11 = 750ps
Bit 4	SD_Skew 0	0	
Bit 3	PCI_Skew 3	0	These 4 bits can change the CPUCLK to PCICLK skew from 1.4ns - 2.9ns. Each binary increment or decrement of PCI_SKEW (3:0) will increase or decrease the delay of the PCI (F,0:1) clocks by 100ps.
Bit 2	PCI_Skew 2	0	
Bit 1	PCI_Skew 1	1	
Bit 0	PCI_Skew 0	0	

Byte 19: Group Skew Control Register*

Bit	Name	PWD	Description
Bit 7	AGP_Skew 3	0	These 4 bits can change the CPUCLK to AGP skew from 1.4ns - 2.9ns. Default at power up is - 2.5ns. Each binary increment or decrement of AGP_SKEW (3:0) will increase or decrease the delay of the AGP clocks by 100ps.
Bit 6	AGP_Skew 2	0	
Bit 5	AGP_Skew 1	1	
Bit 4	AGP_Skew 0	0	
Bit 3	PCI_Skew 3	0	These 4 bits can change the CPUCLK to PCI skew from 1.4ns - 2.9ns. Each binary increment or decrement of PCI_SKEW (3:0) will increase or decrease the delay of the PCI (2:4) clocks by 100ps.
Bit 2	PCI_Skew 2	0	
Bit 1	PCI_Skew 1	1	
Bit 0	PCI_Skew 0	0	

Byte 20: Group Skew Control Register*

Bit	Name	PWD	Description
Bit 7	APIC_Skew 3	0	These 4 bits can change the CPUCLK to APIC skew from 1.4ns - 2.9ns. Default at power up is - 2.5ns. Each binary increment or decrement of APIC_SKEW (3:0) will increase or decrease the delay of the CPU clocks by 100ps.
Bit 6	APIC_Skew 2	0	
Bit 5	APIC_Skew 1	1	
Bit 4	APIC_Skew 0	0	
Bit 3	REF0	1	REF1 (Act/Inactive)
Bit 2	REF1	1	REF0 (Act/Inactive)
Bit 1	IOAPIC	1	IOAPIC (Act/Inactive)
Bit 0	48MHz	1	48MHz (Act/Inactive)

* These bytes are not available in ICS9248A/B/CF-199.
Programmable features on these bytes are only for ICS9248D/EF-199.



Byte 21: Slew Rate Control Register*

Bit	Name	PWD	Description
Bit 7	24/48_Slew 1	0	24/48 MHz clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 6	24/48_Slew 0	1	
Bit 5	AGP_Slew 1	0	AGP clock slew rate control bits. 10 = strong; 00, 11 = normal; 01 = weak
Bit 4	AGP_Slew 0	1	
Bit 3	APIC_Slew 1	0	IOAPIC clock slew rate control bits. 00 = strong; 00, 11 = normal; 10 = weak
Bit 2	APIC_Slew 0	1	
Bit 1	REF_Slew 1	0	REF clock slew rate control bits. 10 = strong; 00, 11 = normal; 00 = weak
Bit 0	REF_Slew 0	1	

Byte 22: Slew Rate Control Register*

Bit	Name	PWD	Description
Bit 7	Reserved	0	Reserved
Bit 6	Reserved	0	Reserved
Bit 5	PCICLK_F 1x2x	0	0:1x, 1:2x
Bit 4	PCICLK0	0	0:1x, 1:2x
Bit 3	Reserved	0	Reserved
Bit 2	Reserved	0	Reserved
Bit 1	Reserved	0	Reserved
Bit 0	Reserved	0	Reserved

Byte 23: Slew Rate Control Register*

Bit	Name	PWD	Description
Bit 7	48MHz Slew 1	0	48MHz clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 6		1	
Bit 5	CPUCLKT/C Slew 1	0	CPUCLKT/C0 clock slew rate control bit. 01 = strong; 00, 11 = normal; 10 = weak
Bit 4		1	
Bit 3	CPUCLK Slew 1	0	CPUCLK clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 2		1	
Bit 1	SD Slew 1	0	SDRAM clock slew rate control bits. 01 = strong; 00, 11 = normal; 10 = weak
Bit 0		1	

Bit 24: Control, Active/Inactive Register*

(1 = enable, 0 = disable)

Bit	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	9	0	PCICLK_F (Act/Inactive)
Bit 2	44	0	CPUCLKT0 (Act/Inactive)
Bit 1	43	0	CPUCLK_C0 (Act/Inactive)
Bit 0	40	1	CPUCLK (Act/Inactive)

* These bytes are not available in ICS9248A/B/CF-199.
Programmable features on these bytes are only for ICS9248D/EF-199.



Absolute Maximum Ratings

Supply Voltage 5.5 V
 Logic Inputs GND -0.5 V to $V_{DD} + 0.5$ V
 Ambient Operating Temperature 0°C to +70°C
 Case Temperature 115°C
 Storage Temperature -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3$ V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		$V_{SS} - 0.3$		0.8	V
Operating Supply Current	I_{DD}	$C_L = 30$ pF PCI, SDRAM, 20 pF other outputs		134	180	mA
	I_{DDL}			27	39	mA
Power Down	PD			280	600	uA
Input frequency	F_i	$V_{DD} = 3.3$ V	12	14.318	16	MHz
Input Capacitance ¹	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transistion Time ¹	T_{trans}	To 1st crossing of target frequency			3	ms
Settling Time ¹	T_s	From 1st crossing to 1% of target frequency				ms
Clk Stabilization ¹	T_{STAB}	From $V_{DD} = 3.3$ V to 1% of target frequency		11	15	ms
Skew ¹	$T_{CPU - PCI}$	$V_T = 1.5$ V; $V_{TL} = 50\%$ V_{DD}	1	1.8	4	ns
Skew ¹	$T_{CPU - AGP}$	$V_T = 1.5$ V; $V_{TL} = 50\%$ V_{DD}	1	1.6	4	ns

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPUCLK (Open Drain)

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O^1	$V_O = V_X$		50		Ω
Output High Voltage	V_{OH2B}	Termination to Vpull-up(external)	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to Vpull-up(external)			0.4	V
Output Low Current	I_{OL2B}	$V_{OL} = 0.3 \text{ V}$	18			mA
Fall Time ¹	t_{f2B}^1	$V_{OH} = 1.1\text{V}, V_{OL} = 2.0\text{V}$		1.7	2	ns
		$V_{OH} = 80\% V_{DD}, V_{OL} = 20\% V_{DD}$		1.1	1.2	
Differential voltage-AC ¹	V_{DIF}	Note 2	0.4		Vpull-up(ext) + 0.6	V
Differential voltage-DC ¹	V_{DIF}	Note 2	0.2		Vpull-up(ext) + 0.6	V
Diff Crossover Voltage ¹	V_X	Note 3	1.2	1.45	1.6	V
Duty Cycle ¹	d_{t2B}^1	CPUT0,C0 between crossing point	45	53	55	%
		CPUT0,C0 $V_T = 50\% V_{DD}$	44	47	55	
Skew CPUCLK to CPUT0 ¹	t_{sk2B}^1	$V_T = 50\%$		40	175	ps
Jitter, Cycle-to-cycle ¹	$t_{jyc-cyc2B}^1$	$V_T = V_X$		105	250	ps
Jitter, Absolute ¹	t_{jabs2B}^1	$V_T = 50\%$	-250		250	ps

Notes:

- 1 - Guaranteed by design, not 100% tested in production.
- 2 - V_{DIF} specifies the minimum input differential voltages ($V_{TR} - V_{CP}$) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.
- 3 - $V_{pull-up(external)} = 2.7\text{V}$, $\text{Min} = V_{pull-up(external)}/2 - 150\text{mV}$; $\text{Max} = V_{pull-up(external)}/2 + 150\text{mV}$

Electrical Characteristics - 24MHz, 48MHz, AGP, REF

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	R_{DSP5B}	$V_O = V_{DD} * (0.5)$	20		60	Ω
Output Impedance ¹	R_{DSN5B}	$V_O = V_{DD} * (0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	$I_{OH} = -14 \text{ mA}$	2.4			V
Output Low Voltage	V_{OL5}	$I_{OL} = 6 \text{ mA}$			0.4	V
Output High Current	I_{OH5}	$V_{OH} = 2.0 \text{ V}$			-20	mA
Output Low Current	I_{OL5}	$V_{OL} = 0.8 \text{ V}$	10			mA
Rise Time ¹	t_{r5}^1	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$		1.3	2	ns
Fall Time ¹	t_{f5}^1	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$		1.3	2	ns
Duty Cycle ¹	d_{t5}^1	$V_T = 1.5 \text{ V}$ 24_48 MHz, AGP	45	52	55	%
		$V_T = 1.5 \text{ V}$ REF	45	55	56	
Skew AGP to AGP ¹	t_{sk5}^1	$V_T = 1.5 \text{ V}$ AGP		100	175	ps
Jitter, Cycle-to-Cycle ¹	$t_{jyc-cyc5}^1$	$V_T = 1.5 \text{ V}$ 24_48 MHz		110	500	ps
		$V_T = 1.5 \text{ V}$ AGP		220		
		$V_T = 1.5 \text{ V}$ REF		375	500	

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3V +/-5%; C_L = 30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	R _{DSP1B}	V _O =V _{DD} *(0.5)	12		55	Ω
Output Impedance ¹	R _{DSN1B}	V _O =V _{DD} *(0.5)	12		55	Ω
Output High Voltage	V _{OH1}	I _{OH} = -18 mA	2.6			V
Output Low Voltage	V _{OL1}	I _{OL} = 9.4 mA			0.4	V
Output High Current	I _{OH1}	V _{OH} = 2.0 V			-22	mA
Output Low Current	I _{OL1}	V _{OL} = 0.8 V	25			mA
Rise Time ¹	t _{r1}	V _{OL} = 0.4 V, V _{OH} = 2.4 V		1.7	2.0	ns
Fall Time ¹	t _{f1}	V _{OH} = 2.4 V, V _{OL} = 0.4 V		1.8	2.0	ns
Duty Cycle ¹	d _{t1}	V _T = 1.5 V	45	51	55	%
Skew Window ¹	t _{sk1}	V _T = 1.5 V		170	500	ps
Jitter, Cycle-to-Cycle ¹	t _{cyc-cyc1}	V _T = 1.5 V		265	500	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD}=3.3V +/-5%; C_L = 30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	R _{DSP3}	V _O =V _{DD} *(0.5)	10		20	Ω
Output Impedance ¹	R _{DSN3}	V _O =V _{DD} *(0.5)	10		20	Ω
Output High Voltage	V _{OH3}	I _{OH} = -28 mA	2.4			V
Output Low Voltage	V _{OL3}	I _{OL} = 19 mA			0.4	V
Output High Current	I _{OH3}	V _{OH} = 2.0 V			-42	mA
Output Low Current	I _{OL3}	V _{OL} = 0.8 V	33			mA
Rise Time ¹	t _{r3}	V _{OL} = 0.4 V, V _{OH} = 2.4 V		0.8	1.5	ns
Fall Time ¹	t _{f3}	V _{OH} = 2.4 V, V _{OL} = 0.4 V		0.6	1.5	ns
Duty Cycle ¹	d _{t3}	V _T = 1.5 V	45	50	55	%
Jitter, Cycle-to-Cycle ¹	t _{cyc-cyc3}	V _T = 1.5 V 100, 133 MHz		150	250	ps
		166 MHz		280	350	

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - IOAPIC

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{V} \pm 5\%$; $C_L = 20 \text{ pF}$ (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance ¹	R_{DSP4B}	$V_O = V_{DD} * (0.5)$	20		60	Ω
Output Impedance ¹	R_{DSN4B}	$V_O = V_{DD} * (0.5)$	20		60	Ω
Output High Voltage	V_{OH4}	$I_{OH} = -14 \text{ mA}$	2.4			V
Output Low Voltage	V_{OL4}	$I_{OL} = 6 \text{ mA}$			0.4	V
Output High Current	I_{OH4}	$V_{OH} = 2.0 \text{ V}$			-20	mA
Output Low Current	I_{OL4}	$V_{OL} = 0.8 \text{ V}$	10			mA
Rise Time ¹	t_{r4}	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$		0.7	2	ns
Fall Time ¹	t_{f4}	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$		0.8	2	ns
Duty Cycle ¹	d_{t4}	$V_T = 1.5 \text{ V}$ 24_48 MHz, AGP	45	50	55	%
Jitter, Cycle-to-Cycle ¹	$t_{j\text{cyc-cyc}4}$	$V_T = 1.5 \text{ V}$ 24_48 MHz		235	500	ps

¹Guaranteed by design, not 100% tested in production.



General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X_(H) was written to byte 0).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2 _(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
Data Byte Count = X			
		ACK	
Beginning Byte N		X Byte	
			ACK
○			○
○			○
○			○
Byte N + X - 1		ACK	
P	stoP bit		

Index Block Read Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D2 _(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D3 _(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK		X Byte	
ACK			Beginning Byte N
○			○
○			○
○			○
		Byte N + X - 1	
N	Not acknowledge		
P	stoP bit		



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-199 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

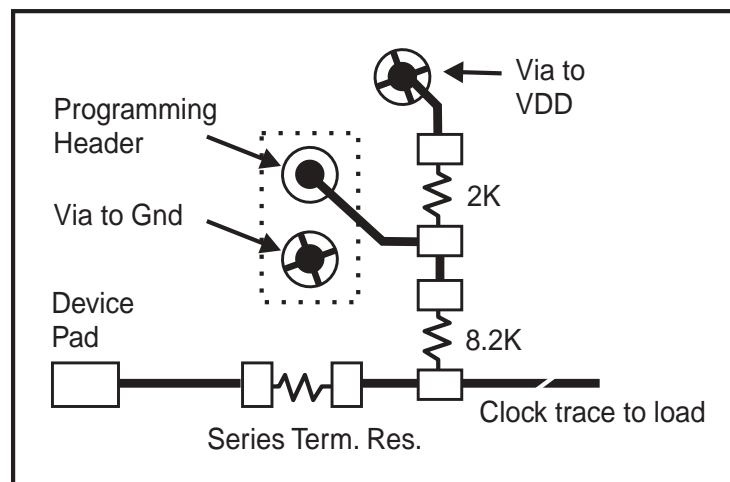
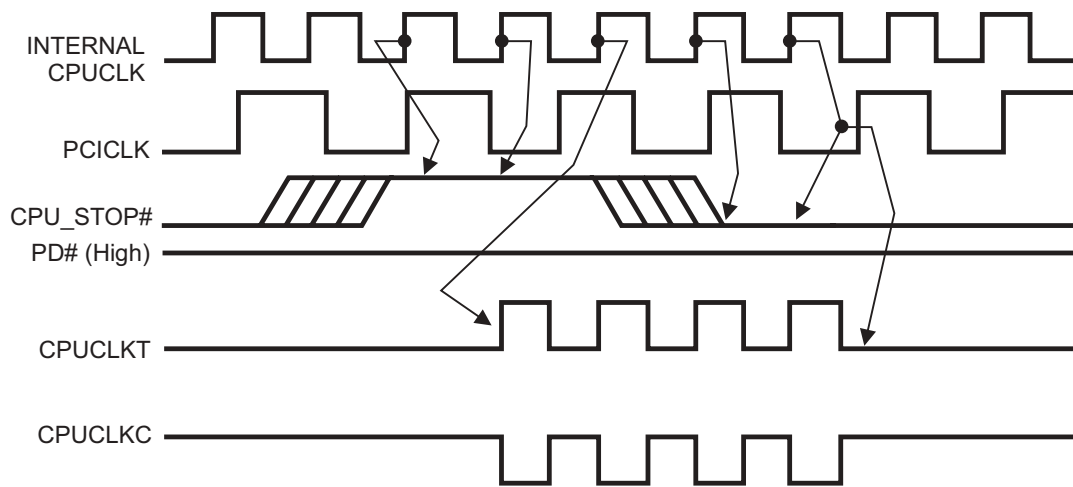


Fig. 1



CPU_STOP# Timing Diagram

CPU_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the ICS9248-199. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



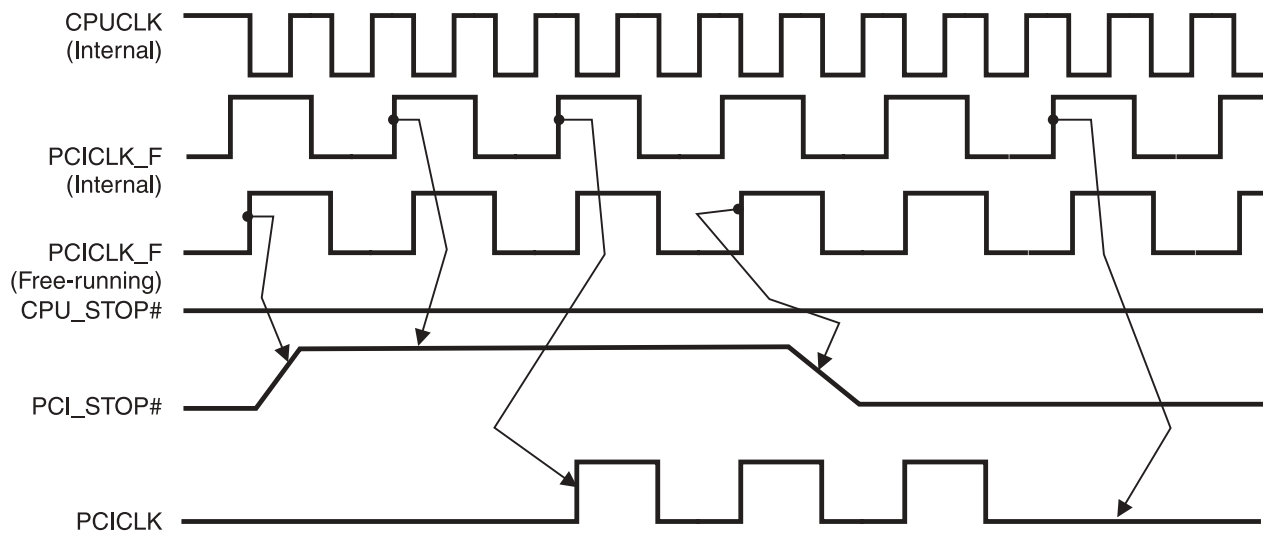
Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-199.
3. All other clocks continue to run undisturbed.



PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-199**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-199** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



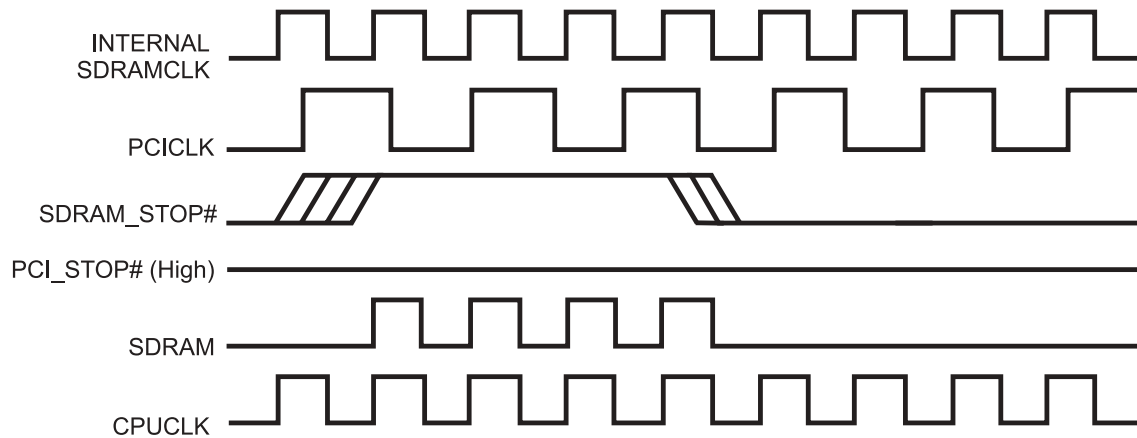
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-199 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-199.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.



SDRAM_STOP# Timing Diagram

SDRAM_STOP# is an asynchronous input to the clock synthesizer. It is used to stop SDRAM clocks for low power operation. SDRAM_STOP# is synchronized to complete its current cycle, by the **ICS9248-199**. All other clocks will continue to run while the SDRAM clocks are disabled. The SDRAM clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse.



Notes:

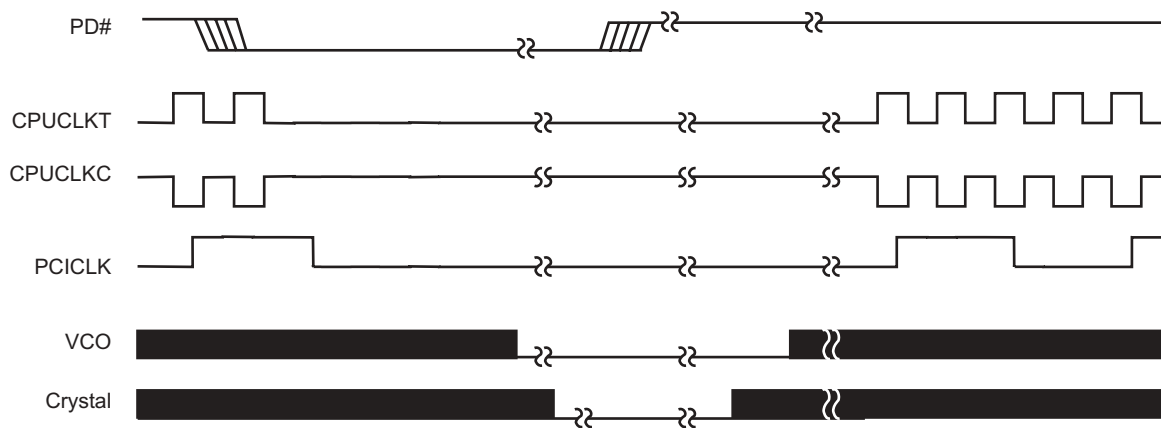
1. All timing is referenced to the internal CPU clock.
2. SDRAM is an asynchronous input and metastable conditions may exist. This signal is synchronized to the SDRAM clocks inside the ICS9248-199.
3. All other clocks continue to run undisturbed.



PD# Timing Diagram

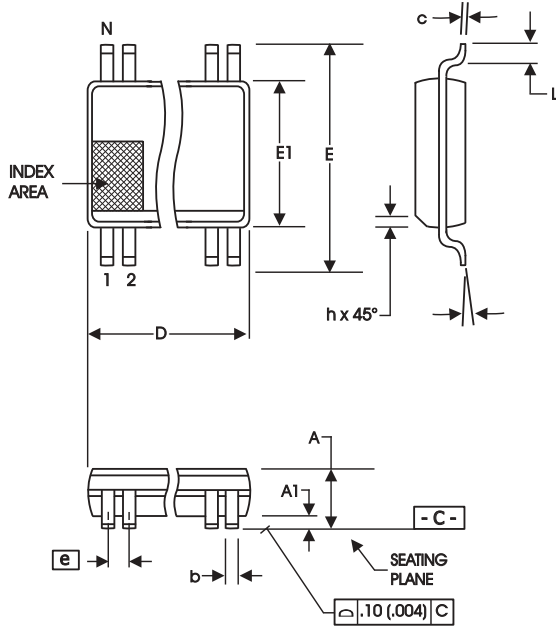
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-199 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

300 mil SSOP Package

Ordering Information

ICS9248yF-199-T

Example:

ICS XXXX y F - PPP - T

