



Frequency Generator & Integrated Buffers for PENTIUM II/III™ & K6

Recommended Application:

440BX, MX, VIA PM/PL/PLE 133 style chip set, with Coppermine or Tualatin processor, for note book applications.

Output Features:

- 4 - CPUs @ 2.5V/3.3V including 1 free running CPUCLK_F
- 9 - SDRAM @ 3.3V
- 7 - PCI @ 3.3V, including 1 free running PCICLK_F
- 1 - PCI Early @ 3.3V
- 1 - 48MHz, @ 3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 2 - REF @3.3V, 14.318MHz.

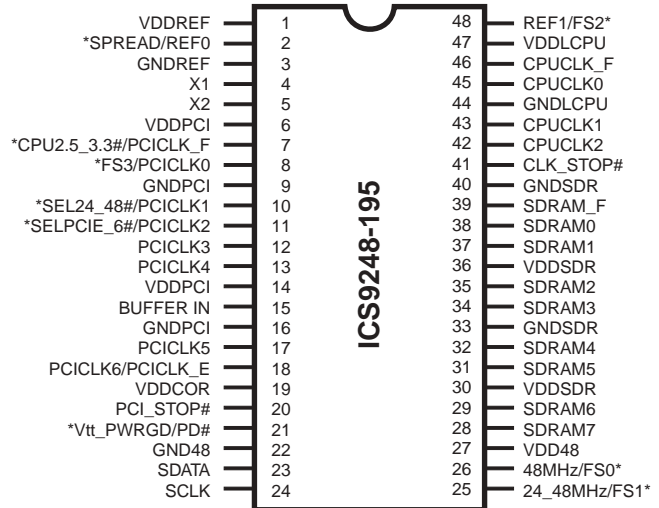
Features:

- Up to 137MHz frequency support
- 97MHz to support high-end AMD processor.
- Support power management: CLK, PCI, stop and Power down Mode from I²C programming.
- Spread spectrum for EMI control
- Uses external 14.318MHz crystal
- FS pins for frequency select

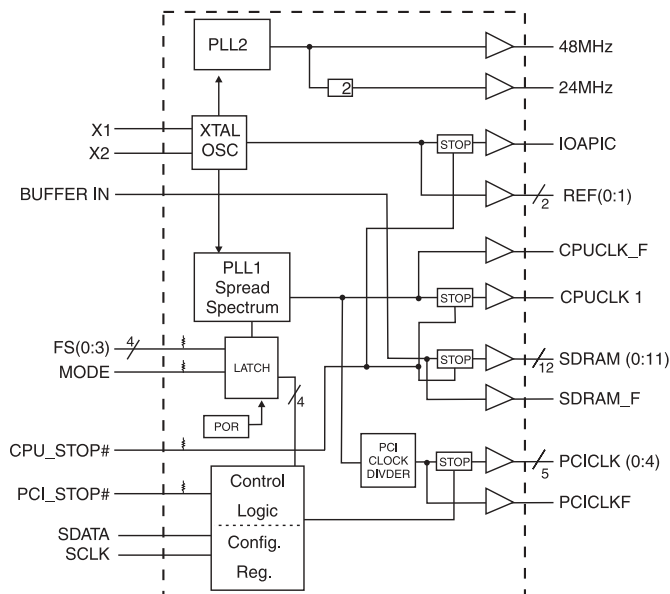
Key Specifications:

- CPU Output Jitter @ 2.5V: <300ps
- CPU Output Jitter @ 3.3V: <250ps
- PCI Output Jitter @ 3.3V: <250ps
- CPU Output Skew @ 2.5V: <175ps
- CPU Output Skew @ 3.3V: <175ps
- PCI Output Skew @ 3.3V: <500ps
- PCI Early to PCI Skew @ 3.3V: typ = 3ns
- SDRAM Output Skew @ 3.3V: <500ps

Pin Configuration



Block Diagram



0375D—02/02/04

48-Pin SSOP and TSSOP

* Internal Pull-up Resistor of 120K to VDD

Functionality

Bit2	Bit6	Bit5	Bit4	CPUCLK	PCICLK
0	0	0	0	66.67	33.33
0	0	0	1	100.00	33.33
0	0	1	0	66.67	33.33
0	0	1	1	133.33	33.33
0	1	0	0	66.67	33.33
0	1	0	1	100.00	33.33
0	1	1	0	100.00	33.33
0	1	1	1	133.33	33.33
1	0	0	0	66.67	33.33
1	0	0	1	100.00	33.33
1	0	1	0	90.00	30.00
1	0	1	1	133.33	33.33
1	1	0	0	70.00	35.00
1	1	0	1	105.00	35.00
1	1	1	0	133.33	33.33
1	1	1	1	140.00	35.00



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	SPREAD ^{1,2}	IN	Active High Spread Spectrum enable input. Power-up default is "High", spreading is "on"
	REF0	OUT	14.318 Mhz reference clock. This REF output is the STRONGER buffer for ISA BUS loads
20	PCI_STOP#	IN	Halts PCICLK clocks at logic 0 level, when input low (In mobile mode, MODE=0)
3, 9, 16, 33, 40, 44	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz.
6,14	VDDPCI	PWR	Supply for PCICLK_F and PCICLK nominal 3.3V
7	CPU2.5_3.3# ^{1,2}	IN	Indicates whether VDDL CPU is 2.5 or 3.3V. High=2.5V CPU, LOW=3.3V CPU. Latched Input.
	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
8	FS3 ^{1,2}	IN	Frequency select pin. Latched Input.
	PCICLK0	OUT	PCI clock output. Synchronous to CPU clocks with 1-4ns skew (CPU early)
10	SEL24_48# ^{1,2}	IN	Selects either 24 or 48MHz when Low =48 MHz
	PCICLK1	OUT	PCI clock output. Synchronous to CPU clocks with 1-4ns skew (CPU early)
11	SELPCIE_6# ^{1,2}	IN	PCI Early or normal PCI select latch input. (for pin 18 power-up default is "High" early PCICLK.)
	PCICLK2	OUT	PCICLK clock output.
17, 13, 12	PCICLK (5:3)	OUT	PCI clock outputs. Synchronous to CPU clocks with 1-4ns skew (CPU early)
15	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
18	PCICLK6/PCICLK_E	OUT	PCI clock output or early PCI clock output selectable by SELPCIE_6#
19	VDDCOR	PWR	Power pin for the PLL core. 3.3V
21	Vtt_PWRGND	IN	This pin acts as a dual function input pin for Vtt_PWRGD and PD# signal. When Vtt_PWRGD goes high the frequency select will be latched at power on thereafter the pin is an asynchronous active low power down pin.
	PD# ¹	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 4ms.
22	GND48	PWR	Ground pin for the 24 & 48MHz output buffers & fixed PLL core.
28, 29, 31, 32, 34, 35, 37, 38	SDRAM (7:0)	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset).
30, 36	VDDSDR	PWR	Supply for SDRAM and CPU PLL Core, nominal 3.3V.
23	SDATA	IN	Data input for I ² C serial input, 5V tolerant input
24	SCLK	IN	Clock input of I ² C input, 5V tolerant input
25	24_48MHz	OUT	24MHz or 48MHz output clock selectable by pin 10
	FS1 ^{1,2}	IN	Frequency select pin. Latched Input.
26	48MHz	OUT	48MHz output clock
	FS0 ^{1,2}	IN	Frequency select pin. Latched Input
27	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
39	SDRAM_F	OUT	Free running SDRAM clock output. Not affected by CPU_STOP#
41	CLK_STOP#	IN	This asynchronous input halts CPUCLK, & SDRAM at logic "0" level when driven low.
42, 43, 45	CPUCLK (2:0)	OUT	CPU clock outputs, powered by VDDL CPU
46	CPUCLK_F	OUT	Free running CPU clock. Not affected by the CPU_STOP#
47	VDDL CPU	PWR	Supply for CPU clocks 2.5V
48	REF1	OUT	14.318 MHz reference clock.
	FS2 ^{1,2}	IN	Frequency select pin. Latched Input

Notes:

- 1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs
- 2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



General Description

The **ICS9248-195** is the single chip clock solution for Notebook designs using the 440BX, MX, VIA PM/PL/PLE 133 style chip set, with Coppermine or Tualatin processor, for Note book applications. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I²C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-195** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description								PWD
Bit 7	0 = Center Spread Spectrum Modulation 1 = Down Spread Spectrum Modulation								1
Bit 2, 6:4	FS3 Bit2	FS2 Bit6	FS1 Bit5	FS0 Bit4	CPUCLK	PCICLK	Center Spread %	Down Spread%	Note1 0011
	0	0	0	0	66.67	33.33	±0.35%	-0.70%	
	0	0	0	1	100.00	33.33	±0.35%	-0.70%	
	0	0	1	0	66.67	33.33	±0.60%	-1.20%	
	0	0	1	1	133.33	33.33	±0.35%	-0.70%	
	0	1	0	0	66.67	33.33	±0.23%	-0.45%	
	0	1	0	1	100.00	33.33	±0.23%	-0.45%	
	0	1	1	0	100.00	33.33	±0.60%	-1.20%	
	0	1	1	1	133.33	33.33	±0.23%	-0.45%	
	1	0	0	0	66.67	33.33	±0.45%	-0.90%	
	1	0	0	1	100.00	33.33	±0.45%	-0.90%	
	1	0	1	0	90.00	30.00	±0.35%	-0.70%	
	1	0	1	1	133.33	33.33	±0.45%	-0.90%	
	1	1	0	0	70.00	35.00	±0.35%	-0.70%	
	1	1	0	1	105.00	35.00	±0.35%	-0.70%	
1	1	1	0	133.33	33.33	±0.60%	-1.20%		
1	1	1	1	140.00	35.00	±0.35%	-0.70%		
Bit 3	0 - Frequency is selected by hardware select pins. Latched inputs. 1 - Frequency is controlled by I ² C programming.								0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled								1
Bit 0	0 - Running 1 - Tristate all outputs								0

Notes:

- 1, Default at Power-up will be for latched logic inputs to define frequency. Bit [2, 6:4] are default to 0011.
- 2, PWD = Power-Up Default


Byte 1: Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	46	1	CPUCLK_F (En/Dis)
Bit 5	-	0	(Reserved)
Bit 4	-	0	(Reserved)
Bit 3	39	1	SDRAM_F (En/Dis)
Bit 2	42	1	CPUCLK2 (En/Dis)
Bit 1	43	1	CPUCLK1 (En/Dis)
Bit 0	45	1	CPUCLK0 (En/Dis)

Byte 2: Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	7	1	PCICLK_F (En/Dis)
Bit 6	18	1	PCICLK6 (En/Dis)
Bit 5	17	1	PCICLK5 (En/Dis)
Bit 4	13	1	PCICLK4 (En/Dis)
Bit 3	12	1	PCICLK3 (En/Dis)
Bit 2	11	1	PCICLK2 (En/Dis)
Bit 1	10	1	PCICLK1 (En/Dis)
Bit 0	8	1	PCICLK0 (En/Dis)

Byte 3: Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	0	(Reserved)
Bit 5	-	0	(Reserved)
Bit 4	-	0	(Reserved)
Bit 3	28	1	SDRAM7 (En/Dis)
Bit 2	29	1	SDRAM6 (En/Dis)
Bit 1	31	1	SDRAM5 (En/Dis)
Bit 0	32	1	SDRAM4 (En/Dis)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched register values will be inverted from pin values. Default latch condition is for all latched inputs to be floating (pulled up via internal resistor) at power-up.


Byte 4: Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	0	(Reserved)
Bit 5	-	0	(SEL24_48)#
Bit 4	-	0	Latched FS0#
Bit 3	-	0	Latched FS1#
Bit 2	-	0	Latched FS2#
Bit 1	-	0	Latched FS3#
Bit 0	-	1	(Reserved)

Byte 5: Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	34	1	SDRAM3 (En/Dis)
Bit 6	35	1	SDRAM2 (En/Dis)
Bit 5	37	1	SDRAM1 (En/Dis)
Bit 4	38	1	SDRAM0 (En/Dis)
Bit 3	26	1	48MHz (En/Dis)
Bit 2	25	1	24MHz (En/Dis)
Bit 1	48	1	REF1 (En/Dis)
Bit 0	2	1	REF0 (En/Dis)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched register values will be inverted from pin values. Default latch condition is for all latched inputs to be floating (pulled up via internal resistor) at power-up.



Absolute Maximum Ratings

Supply Voltage	5.5 V
Logic Inputs	GND -0.5 V to $V_{DD} + 0.5$ V
Ambient Operating Temperature	0°C to +70°C
Case Temperature	115°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = V_{DDL} = 3.3$ V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}		$V_{SS} - 0.3$		0.8	V
Operating Supply Current	$I_{DD3.30P}$	$C_L = 0$ pF; Select @ 66MHz			150	mA
		$C_L = 0$ pF; Select @ 100MHz			170	
		$C_L = 0$ pF; Select @ 133MHz			180	
Powerdown Current	I_{DDPD}	$C_L = 0$ pF; Input address VDD or GND			600	μA
Input Frequency	F_i	$V_{DD} = 3.3$ V		14.32		MHz
Input Capacitance ¹	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization ¹	T_{STAB}	From $V_{DD} = 3.3$ V to 1% target Freq.			5.5	ms
Skew ¹	$t_{CPU-PCI1}$	$V_T = 1.5$ V	1		4	ns

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3$ V +/-5%, $V_{DDL} = 2.5$ V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DDL2.5}$	$C_L = 0$ pF; Select @ 66.8 MHz			15	mA
		$C_L = 0$ pF; Select @ 100 MHz			18	
		$C_L = 0$ pF; Select @ 133 MHz			25	
Powerdown Current	I_{DDLDPD}	$C_L = 0$ pF; Input address VDD or GND			10	mA
Skew ¹	$t_{CPU-PCI2}$	$V_T = 1.5$ V; $V_{TL} = 1.25$ V	1		4	ns

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2A}	$I_{OH} = -20\text{ mA}$	2.4			V
Output Low Voltage	V_{OL2A}	$I_{OL} = 12\text{ mA}$			0.4	V
Output High Current	I_{OH2A}	$V_{OH} = 2.0\text{ V}$			-27	mA
Output Low Current	I_{OL2A}	$V_{OL} = 0.8\text{ V}$	22			mA
Rise Time ¹	t_{r2A}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$		1.35	2	ns
Fall Time ¹	t_{f2A}	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$		1.44	2	ns
Duty Cycle ¹	d_{t2A}	$V_T = 1.5\text{ V}$	45	50.3	55	%
Skew window ¹	t_{sk2A}	$V_T = 1.5\text{ V}$		70	175	ps
Jitter, Cycle-to-cycle ¹	$t_{jyc-cyc2A}$	$V_T = 1.5\text{ V}$		160	250	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

$T_A = 0 - 70^\circ\text{C}$; $V_{DDL} = 2.5\text{ V} \pm 5\%$; $C_L = 20\text{ pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	$I_{OH} = -12\text{ mA}$	2			V
Output Low Voltage	V_{OL2B}	$I_{OL} = 12\text{ mA}$			0.4	V
Output High Current	I_{OH2B}	$V_{OH} = 1.7\text{ V}$			-21	mA
Output Low Current	I_{OL2B}	$V_{OL} = 0.7\text{ V}$	22			mA
Rise Time ¹	t_{r2B}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.0\text{ V}$		1.40	1.8	ns
Fall Time ¹	t_{f2B}	$V_{OH} = 2.0\text{ V}$, $V_{OL} = 0.4\text{ V}$		1.70	1.8	ns
Duty Cycle ¹	d_{t2B}	$V_T = 1.25\text{ V}$, $< 133\text{ MHz}$	45	52	55	%
		$V_T = 1.25\text{ V}$, $\geq 133\text{ MHz}$	42	51	52	
Skew window ¹	t_{sk2B}	$V_T = 1.25\text{ V}$		60	175	ps
Jitter, Cycle-to-cycle ¹	$t_{jyc-cyc2B}$	$V_T = 1.25\text{ V}$		143	250	ps

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - PCI

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 30 \text{ pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	$I_{OH} = -18 \text{ mA}$	2.4			V
Output Low Voltage	V_{OL1}	$I_{OL} = 9.4 \text{ mA}$			0.4	V
Output High Current	I_{OH1}	$V_{OH} = 2.0 \text{ V}$			-33	mA
Output Low Current	I_{OL1}	$V_{OL} = 0.8 \text{ V}$	38			mA
Rise Time ¹	t_{r1}	$V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$		1.60	2.2	ns
Fall Time ¹	t_{f1}	$V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$		1.50	2.2	ns
Duty Cycle ¹	d_{t1}	$V_T = 1.5 \text{ V}$	45	51.5	55	%
Skew window ¹	t_{sk1}	$V_T = 1.5 \text{ V}$		380	500	ps
Skew window ¹	t_{sk2}	$V_T = 1.5 \text{ V}$ PCICLKE to PCI [5:0]	2	2.71	4	ns
Jitter, Absolute ¹	t_{jabs1}	$V_T = 1.5 \text{ V}$		120	250	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3 \text{ V} \pm 5\%$; $C_L = 30 \text{ pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	$I_{OH} = -28 \text{ mA}$	2.4			V
Output Low Voltage	V_{OL3}	$I_{OL} = 19 \text{ mA}$			0.4	V
Output High Current	I_{OH3}	$V_{OH} = 2.0 \text{ V}$			-46	mA
Output Low Current	I_{OL3}	$V_{OL} = 0.8 \text{ V}$	32			mA
Rise Time ¹	T_{r3}	$V_{OL} = 0.4 \text{ V}$, $V_{OH} = 2.4 \text{ V}$		1.17	1.6	ns
Fall Time ¹	T_{f3}	$V_{OH} = 2.4 \text{ V}$, $V_{OL} = 0.4 \text{ V}$		1.20	1.6	ns
Duty Cycle ¹	D_{t3}	$V_T = 1.5 \text{ V}$	42	50	52	%
Skew window ¹	T_{sk3}	$V_T = 1.5 \text{ V}$		210	250	ps
Propagation Time ¹ (Buffer In to output)	T_{sk3}	$V_T = 1.5 \text{ V}$		4.10	5	ns

¹Guaranteed by design, not 100% tested in production.



Electrical Characteristics - 24,48MHz

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 10 - 20\text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	$I_{OH} = -14\text{ mA}$	2.4			V
Output Low Voltage	V_{OL5}	$I_{OL} = 6\text{ mA}$			0.4	V
Output High Current	I_{OH5}	$V_{OH} = 2.0\text{ V}$			-20	mA
Output Low Current	I_{OL5}	$V_{OL} = 0.8\text{ V}$	16			mA
Rise Time ¹	t_{r5}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$		1.93	4	ns
Fall Time ¹	t_{f5}	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$		2.63	4	ns
Duty Cycle ¹	d_{t5}	$V_T = 1.5\text{ V}$	45	50.9	55	%
Jitter, Absolute ¹	t_{CYCLE}	$V_T = 1.5\text{ V}$		436	600	ps

¹Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 10 - 20\text{ pF}$ (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	$I_{OH} = -14\text{ mA}$	2.4	2.6		V
Output Low Voltage	V_{OL5}	$I_{OL} = 6\text{ mA}$		0.22	0.4	V
Output High Current	I_{OH5}	$V_{OH} = 2.0\text{ V}$		-32	-20	mA
Output Low Current	I_{OL5}	$V_{OL} = 0.8\text{ V}$	16	22		mA
Rise Time ¹	t_{r5}	$V_{OL} = 0.4\text{ V}$, $V_{OH} = 2.4\text{ V}$		2.11	4	ns
Fall Time ¹	t_{f5}	$V_{OH} = 2.4\text{ V}$, $V_{OL} = 0.4\text{ V}$		2.14	4	ns
Duty Cycle ¹	d_{t5}	$V_T = 1.5\text{ V}$	45	52.1	55	%
Jitter, cycle to cycle ¹	$t_{jcycle5}$	$V_T = 1.5\text{ V}$	-600	848	1000	ps

¹Guaranteed by design, not 100% tested in production.



General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2_(H)
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 _(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3_(H)
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte (*Byte 0*) through byte 5
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 _(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PII/PIII "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

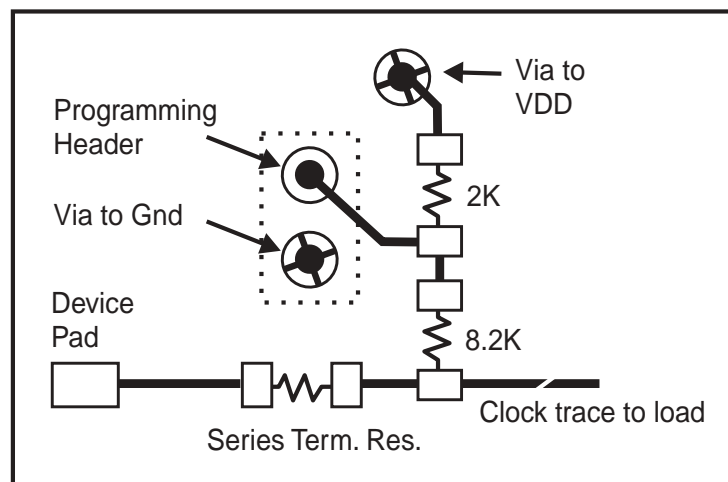


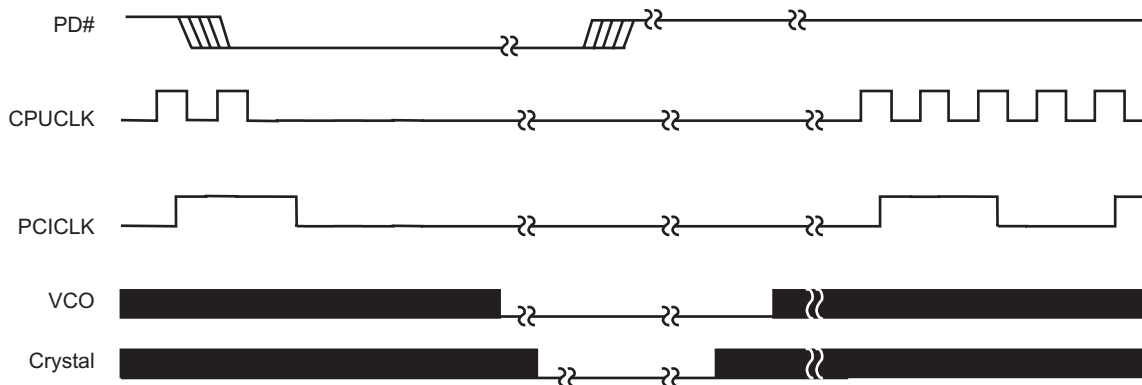
Fig. 1



PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 4 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CLK_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



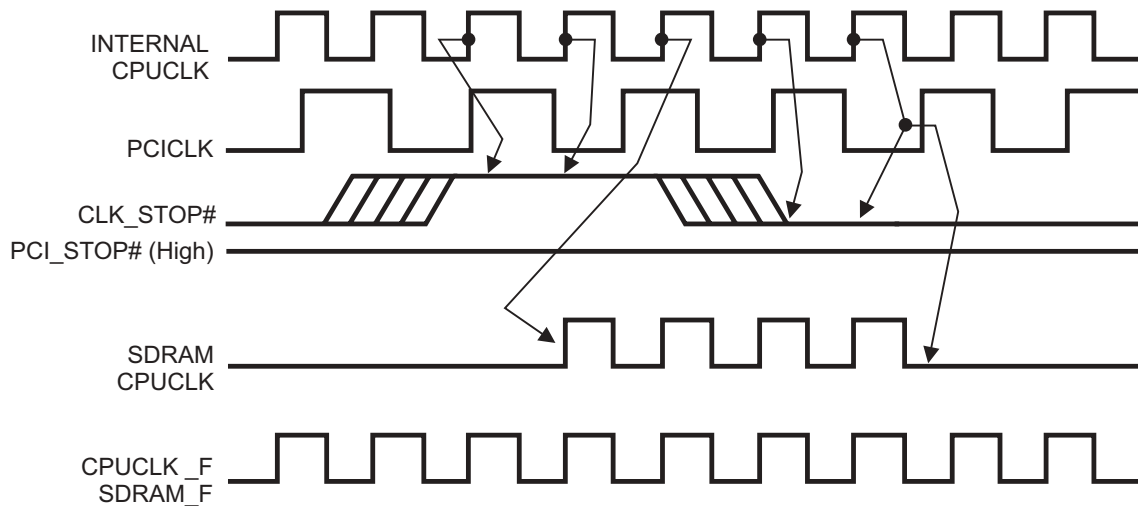
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



CLK_STOP# Timing Diagram

CLK_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CLK_STOP# is synchronized by the ICS9248-195. The minimum that the CPU clock is enabled (CLK_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



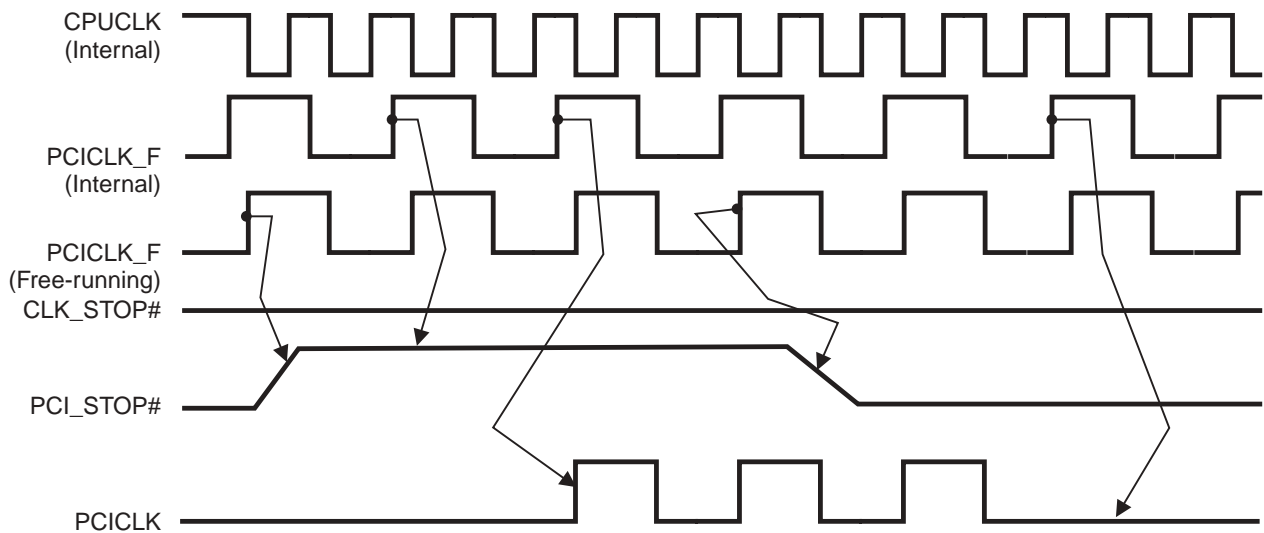
Notes:

1. All timing is referenced to the internal CPU clock.
2. CLK_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-195.
3. SDRAM-F output is controlled by Buffer in signal, not affected by the ICS9248-195 CLK_STOP# signal. SDRAM are controlled as shown.
4. All other clocks continue to run undisturbed.



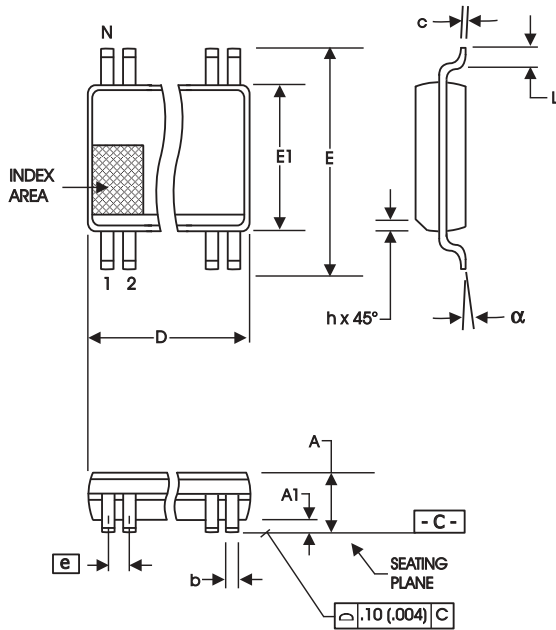
PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-195**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-195** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only three rising PCICLK clocks, off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248.
3. All other clocks continue to run undisturbed.
4. CLK_STOP# is shown in a high (true) state.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

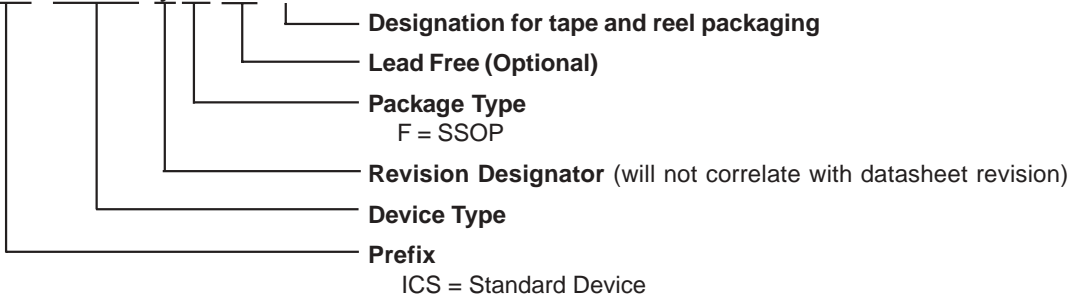
Reference Doc.: JEDEC Publication 95, MO-118
10-0034

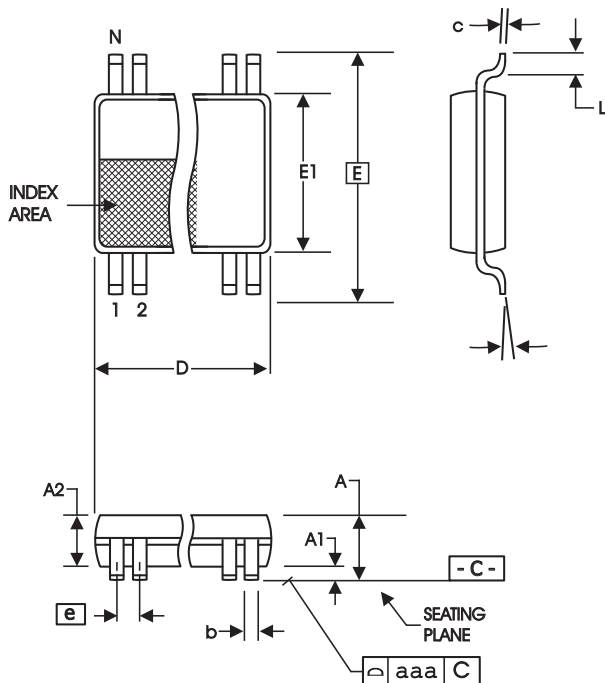
Ordering Information

ICS9248yF-195LF-T

Example:

ICS XXXX y F LF-T





(240 mil) (0.020 mil)
6.10 mm. Body, 0.50 mm. pitch TSSOP

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS9248yG-195LF-T

Example:

ICS XXXX y G LF-T

