

## Frequency Generator for Intel Pentium III Celeron Processor

### Recommended Application:

Single chip clock solution for SIS 635/640 Intel Pentium III Celeron chipset.

### Output Features:

- 2 - CPUs @ 2.5V.
- 1 - IOAPIC @ 2.5V.
- 1 - SDRAM @ 3.3V
- 6- PCI @3.3V
- 2 - AGP @ 3.3V
- 1- 48MHz, @3.3V fixed.
- 1- 24/48MHz, @3.3V selectable by I<sup>2</sup>C (Default is 24MHz)
- 2- REF @3.3V, 14.318MHz.

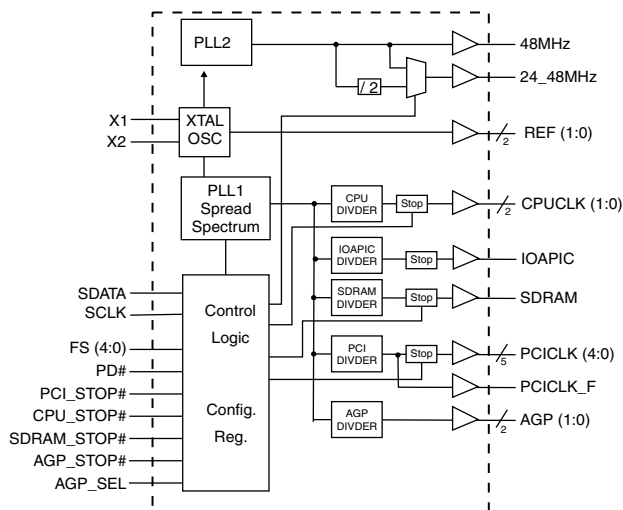
### Features:

- Up to 166MHz frequency support
- Support FS0-FS3 trapping status bit for I<sup>2</sup>C read back.
- Support power management: CPU, PCI, SDRAM stop and Power down Mode from I<sup>2</sup>C programming.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%).
- Uses external 14.318MHz crystal

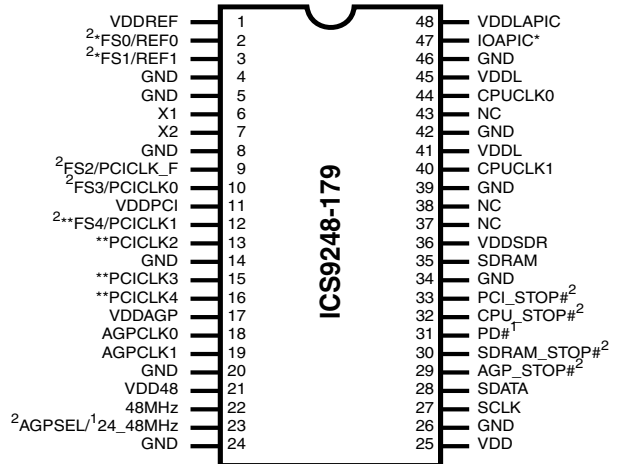
### Skew Specifications:

- CPU - CPU: < 175ps
- PCI - PCI: < 500ps
- CPU - SDRAM: < 250ps
- CPU (early) - PCI: 1-4ns (typ. 2ns)
- AGP - AGP: <175ps
- CPU - AGP: 1-4ns

### Block Diagram



### Pin Configuration



### 48-Pin 300mil SSOP

- \* These are double strength.
- \*\* (1X/2X) have single or double strength to drive 2 loads.
- 1. Internal pull-up, of 120K to V<sub>DD</sub>.
- 2. These inputs have a 120K pull down to GND.

### Functionality

| FS3 | FS2 | FS1 | FS0 | CPU    | SDRAM  | PCICLK | AGP SEL = 0 | AGP SEL = 1 |
|-----|-----|-----|-----|--------|--------|--------|-------------|-------------|
| 0   | 0   | 0   | 0   | 66.66  | 66.66  | 33.33  | 66.66       | 50          |
| 0   | 0   | 0   | 1   | 100    | 100    | 33.33  | 66.66       | 50          |
| 0   | 0   | 1   | 0   | 166.66 | 166.66 | 33.33  | 66.66       | 55.6        |
| 0   | 0   | 1   | 1   | 133.33 | 133.33 | 33.33  | 66.66       | 50          |
| 0   | 1   | 0   | 0   | 66.66  | 100    | 33.33  | 66.66       | 50          |
| 0   | 1   | 0   | 1   | 100    | 66.66  | 33.33  | 66.66       | 50          |
| 0   | 1   | 1   | 0   | 100    | 133.33 | 33.33  | 66.66       | 50          |
| 0   | 1   | 1   | 1   | 133.33 | 100    | 33.33  | 66.66       | 50          |
| 1   | 0   | 0   | 0   | 112    | 112    | 33.6   | 67.2        | 56          |
| 1   | 0   | 0   | 1   | 124    | 124    | 31     | 62          | 46.5        |
| 1   | 0   | 1   | 0   | 138    | 138    | 34.5   | 69          | 46.0        |
| 1   | 0   | 1   | 1   | 150    | 150    | 30     | 60          | 50          |
| 1   | 1   | 0   | 0   | 66.66  | 133.33 | 33.33  | 66.66       | 49.84       |
| 1   | 1   | 0   | 1   | 133.33 | 166.66 | 33.33  | 66.66       | 55.3        |
| 1   | 1   | 1   | 0   | 150    | 100    | 30     | 60          | 50          |
| 1   | 1   | 1   | 1   | 160    | 120    | 30     | 60          | 48          |

**Note:** Please see full table on page 4.



### Pin Configuration

| PIN NUMBER                              | PIN NAME     | TYPE | DESCRIPTION   |
|---|--------------|------|---|
| 1, 11, 17, 21, 25, 36                   | VDD          | PWR  | 3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output.  |
| 2                                       | FS0          | IN   | Frequency select pin.   |
|   | REF0         | OUT  | 14.318 MHz reference clock.   |
| 3                                       | FS1          | IN   | Frequency select pin.   |
|   | REF1         | OUT  | 14.318 MHz reference clock.   |
| 4, 5, 8, 14, 20, 24, 26, 34, 39, 42, 46 | GND          | PWR  | Ground pin for outputs.   |
| 6                                       | X1           | IN   | Crystal input, nominally 14.318MHz.   |
| 7                                       | X2           | OUT  | Crystal output, nominally 14.318MHz.  |
| 9                                       | FS2          | IN   | Frequency select pin.   |
|   | PCICLK_F     | OUT  | PCI clock output, not affected by PCI_STOP#.  |
| 10                                      | FS3          | IN   | Frequency select pin.   |
|   | PCICLK0      | OUT  | PCI clock output.   |
| 12                                      | FS4          | IN   | Frequency select pin.   |
|   | PCICLK1      | OUT  | PCI clock output.   |
| 16, 15, 13                              | PCICLK (4:2) | OUT  | PCI clock outputs.  |
| 19, 18                                  | AGPCLK (1:0) | OUT  | AGP outputs defined as 2X PCI. These may not be stopped.  |
| 22                                      | 48MHz        | OUT  | 48MHz output clock.   |
| 23                                      | AGPSEL       | IN   | AGP frequency select pin.   |
|   | 24_48MHz     | OUT  | Clock output for super I/O/USB default is 24MHz.  |
| 27                                      | SCLK         | IN   | Clock pin of I <sup>2</sup> C circuitry 5V tolerant.  |
| 28                                      | SDATA        | I/O  | Data pin for I <sup>2</sup> C circuitry 5V tolerant.  |
| 29                                      | AGP_STOP#    | IN   | Stops all AGP clocks besides the AGP_F clocks at logic 0 level, when input low.   |
| 30                                      | SDRAM_STOP#  | IN   | Stops all SDRAM clocks at logic 0 level, when input low.  |
| 31                                      | PD#          | IN   | Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms. |
| 32                                      | CPU_STOP#    | IN   | Stops all CPUCLKs clocks at logic 0 level, when input low   |
| 33                                      | PCI_STOP#    | IN   | Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low.   |
| 35                                      | SDRAM        | OUT  | SDRAM clock output.   |
| 37, 38, 43                              | NC           | -    | No connect pins.  |
| 40, 44                                  | CPUCLK (1:0) | OUT  | CPU clock outputs.  |
| 41, 45, 48                              | VDDL         | PWR  | Supply for CPU and IOAPIC clocks at 2.5V nominal.   |



### General Description

The **ICS9248-179** is the single chip clock solution for Desktop/Notebook designs using the SIS 635/640 style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I<sup>2</sup>C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-179 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I<sup>2</sup>C interface allows changing functions, stop clock programming and frequency selection.

### Power Groups

VDDCPU = CPU

VDDPCI = PCICLK\_F, PCICLK

VDDSDR = SDRAM

VDD48 = 48MHz, 24MHz, fixed PLL

VDDA = Core, PLL, X1, X2

VDDAGP=AGP, REF



## Preliminary Product Preview

### Serial Configuration Command Bitmap

Bytes 0-3: Are reserved for external clock buffer.

Byte4: Functionality and Frequency Select Register (default = 0)

| Bit              | Description  |              |              |              |              | CPU    | SDRAM  | PCI   | AGP<br>SEL = 0 | AGP<br>SEL = 1          | Spread Percentage       | PWD            |
|------------------|--|--------------|--------------|--------------|--------------|--------|--------|-------|----------------|-------------------------|-------------------------|----------------|
|                  | Bit 2<br>FS4   | Bit 7<br>FS3 | Bit 6<br>FS2 | Bit 5<br>FS1 | Bit 4<br>FS0 |        |        |       |                |                         |                         |                |
| Bit 2<br>Bit 7:4 | 0  | 0            | 0            | 0            | 0            | 66.66  | 66.66  | 33.33 | 66.66          | 50                      | 0 to -0.5% Down Spread  | 00000<br>Note1 |
|                  | 0  | 0            | 0            | 0            | 1            | 100    | 100    | 33.33 | 66.66          | 50                      | 0 to -0.5% Down Spread  |                |
|                  | 0  | 0            | 0            | 1            | 0            | 166.66 | 166.66 | 33.33 | 66.66          | 55.6                    | +/- 0.25% Center Spread |                |
|                  | 0  | 0            | 0            | 1            | 1            | 133.33 | 133.33 | 33.33 | 66.66          | 50                      | 0 to -0.5% Down Spread  |                |
|                  | 0  | 0            | 1            | 0            | 0            | 66.66  | 100    | 33.33 | 66.66          | 50                      | 0 to -0.5% Down Spread  |                |
|                  | 0  | 0            | 1            | 0            | 1            | 100    | 66.66  | 33.33 | 66.66          | 50                      | 0 to -0.5% Down Spread  |                |
|                  | 0  | 0            | 1            | 1            | 0            | 100    | 133.33 | 33.33 | 66.66          | 50                      | 0 to -0.5% Down Spread  |                |
|                  | 0  | 0            | 1            | 1            | 1            | 133.33 | 100    | 33.33 | 66.66          | 50                      | 0 to -0.5% Down Spread  |                |
|                  | 0  | 1            | 0            | 0            | 0            | 112    | 112    | 33.6  | 67.2           | 56                      | +/- 0.25% Center Spread |                |
|                  | 0  | 1            | 0            | 0            | 1            | 124    | 124    | 31    | 62             | 46.5                    | +/- 0.25% Center Spread |                |
|                  | 0  | 1            | 0            | 1            | 0            | 138    | 138    | 34.5  | 69             | 46.0                    | +/- 0.25% Center Spread |                |
|                  | 0  | 1            | 0            | 1            | 1            | 150    | 150    | 30    | 60             | 50                      | +/- 0.25% Center Spread |                |
|                  | 0  | 1            | 1            | 0            | 0            | 66.66  | 133.33 | 33.33 | 66.66          | 49.84                   | 0 to -0.5% Down Spread  |                |
|                  | 0  | 1            | 1            | 0            | 1            | 133.33 | 166.66 | 33.33 | 66.66          | 55.3                    | 0 to -0.5% Down Spread  |                |
|                  | 0  | 1            | 1            | 1            | 0            | 150    | 100    | 30    | 60             | 50                      | +/- 0.25% Center Spread |                |
|                  | 0  | 1            | 1            | 1            | 1            | 160    | 120    | 30    | 60             | 48                      | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 0            | 0            | 0            | 90     | 90     | 30    | 60             | 45                      | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 0            | 0            | 1            | 100.9  | 100.9  | 33.63 | 67.27          | 50.45                   | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 0            | 1            | 0            | 103    | 103    | 34.33 | 68.67          | 51.5                    | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 0            | 1            | 1            | 133.9  | 133.9  | 33.48 | 68.67          | 51.56                   | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 1            | 0            | 0            | 137.33 | 103    | 34.33 | 66.95          | 51.45                   | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 1            | 0            | 1            | 137.33 | 137.33 | 34.33 | 68.67          | 50.21                   | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 1            | 1            | 0            | 100.9  | 133.9  | 33.48 | 66.95          | 50.21                   | +/- 0.25% Center Spread |                |
|                  | 1  | 0            | 1            | 1            | 1            | 133.9  | 100.9  | 33.48 | 66.95          | 50.21                   | +/- 0.25% Center Spread |                |
| 1                | 1  | 0            | 0            | 0            | 107          | 107    | 35.66  | 71.33 | 53.5           | +/- 0.25% Center Spread |                         |                |
| 1                | 1  | 0            | 0            | 1            | 107          | 142.66 | 35.66  | 71.33 | 53.5           | +/- 0.25% Center Spread |                         |                |
| 1                | 1  | 0            | 1            | 0            | 142.66       | 142.66 | 35.66  | 71.33 | 53.5           | +/- 0.25% Center Spread |                         |                |
| 1                | 1  | 0            | 1            | 1            | 110          | 110    | 36.66  | 73.33 | 55             | +/- 0.25% Center Spread |                         |                |
| 1                | 1  | 1            | 0            | 0            | 110          | 146.66 | 36.66  | 73.33 | 55             | +/- 0.25% Center Spread |                         |                |
| 1                | 1  | 1            | 0            | 1            | 146.66       | 146.66 | 36.66  | 73.33 | 55             | +/- 0.25% Center Spread |                         |                |
| 1                | 1  | 1            | 1            | 0            | 166.7        | 125    | 31.25  | 66.68 | 55.57          | +/- 0.25% Center Spread |                         |                |
| 1                | 1  | 1            | 1            | 1            | 200.0        | 200.0  | 33.33  | 66.66 | 50             | +/- 0.25% Center Spread |                         |                |
| Bit 3            | 0 - Frequency is selected by hardware select, Latched Inputs<br>1 - Frequency is selected by Bit , 2 7:4 |              |              |              |              |        |        |       |                |                         |                         | 0              |
| Bit 1            | 0 - Normal<br>1 - Spread Spectrum Enabled  |              |              |              |              |        |        |       |                |                         |                         | 1              |
| Bit 0            | 0 - Running<br>1- Tristate all outputs   |              |              |              |              |        |        |       |                |                         |                         | 0              |

**Note1:**

Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

**Note:** PWD = Power-Up Default



**Byte 5: CPU, Active/Inactive Register**  
(1= enable, 0 = disable)

| BIT   | PIN# | PWD | DESCRIPTION                              |
|-------|------|-----|--|
| Bit 7 | 23   | 1   | 24M_48M (1: On, 0: Off)                  |
| Bit 6 | 2,3  | 0   | REF_1X2X_Control (0: 1x, 1: 2x)          |
| Bit 5 | 47   | 1   | APIC1X2X_Control (0: 1x, 1: 2x)          |
| Bit 4 | 3    | 1   | REF1 (Act/Inactive)                      |
| Bit 3 | 2    | 1   | REF0 (Act/Inactive)                      |
| Bit 2 | -    | 0   | IOAPIC Select (0:16.67 MHz, 1:33.33 MHz) |
| Bit 1 | 23   | 1   | 24M_48M Select (1: 24 MHz, 0: 48 MHz)    |
| Bit 0 | 22   | 1   | 48MHz (Act/Inactive)                     |

**Byte 6: PCI, Active/Inactive Register**  
(1= enable, 0 = disable)

| BIT   | PIN# | PWD | DESCRIPTION            |
|-------|------|-----|------------------------|
| Bit 7 | 19   | 1   | AGPCLK1 (Act/Inactive) |
| Bit 6 | 18   | 1   | AGPCLK0 (Act/Inactive) |
| Bit 5 | 16   | 1   | PCICLK4 (Act/Inactive) |
| Bit 4 | 15   | 1   | PCICLK3 (Act/Inactive) |
| Bit 3 | 13   | 1   | PCICLK2 (Act/Inactive) |
| Bit 2 | 12   | 1   | PCICLK1 (Act/Inactive) |
| Bit 1 | 10   | 1   | PCICLK0 (Act/Inactive) |
| Bit 0 | 23   | X   | AGPSEL (read back)     |

**Byte 7: Control, Active/Inactive Register**  
(1= enable, 0 = disable)

| BIT   | PIN# | PWD | DESCRIPTION                         |
|-------|------|-----|-------------------------------------|
| Bit 7 | 12   | 0   | PCLCLK1_1X2X_Control (1: 2x, 0: 1x) |
| Bit 6 | 13   | 0   | PCLCLK2_1X2X_Control (1: 2x, 0: 1x) |
| Bit 5 | 10   | X   | FS3 (read back)                     |
| Bit 4 | 9    | X   | FS2 (read back)                     |
| Bit 3 | 3    | X   | FS1 (read back)                     |
| Bit 2 | 2    | X   | FS0 (read back)                     |
| Bit 1 | 15   | X   | PCLCLK3_1X2X_Control (1: 2x, 0: 1x) |
| Bit 0 | 16   | X   | PCLCLK4_1X2X_Control (1: 2x, 0: 1x) |

**Byte 8: Vendor ID Register**  
(1= enable, 0 = disable)

| BIT   | PIN# | PWD | DESCRIPTION |
|-------|------|-----|-------------|
| Bit 7 | -    | 0   | Reserved    |
| Bit 6 | -    | 0   | Reserved    |
| Bit 5 | -    | 0   | Reserved    |
| Bit 4 | -    | 0   | Reserved    |
| Bit 3 | -    | 0   | Reserved    |
| Bit 2 | -    | 0   | Reserved    |
| Bit 1 | -    | 0   | Reserved    |
| Bit 0 | -    | 1   | Reserved    |



## Preliminary Product Preview

### Absolute Maximum Ratings

|                                     |                                |
|-------------------------------------|--------------------------------|
| Supply Voltage .....                | 5.5 V                          |
| Logic Inputs .....                  | GND -0.5 V to $V_{DD} + 0.5$ V |
| Ambient Operating Temperature ..... | 0°C to +70°C                   |
| Case Temperature .....              | 115°C                          |
| Storage Temperature .....           | -65°C to +150°C                |

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ\text{C}$ ; Supply Voltage  $V_{DD} = 3.3$  V +/-5% (unless otherwise stated)

| PARAMETER                      | SYMBOL           | CONDITIONS                               | MIN            | TYP | MAX            | UNITS |
|--------------------------------|------------------|--|----------------|-----|----------------|-------|
| Input High Voltage             | $V_{IH}$         |  | 2              |     | $V_{DD} + 0.3$ | V     |
| Input Low Voltage              | $V_{IL}$         |  | $V_{SS} - 0.3$ |     | 0.8            | V     |
| Supply Current                 | $I_{DD}$         | $C_L = 0$ pF; Select @ 66M               |                |     | 180            | mA    |
|                                | $I_{DDL}$        |  |                |     | 30             | mA    |
| Input frequency                | $F_i$            | $V_{DD} = 3.3$ V;                        |                |     |                | MHz   |
| Input Capacitance <sup>1</sup> | $C_{IN}$         | Logic Inputs                             |                |     | 5              | pF    |
|                                | $C_{INX}$        | X1 & X2 pins                             | 27             |     | 45             | pF    |
| Transition Time <sup>1</sup>   | $T_{trans}$      | To 1st crossing of target Freq.          |                |     | 3              | ms    |
| Settling Time <sup>1</sup>     | $T_s$            | From 1st crossing to 1% target Freq.     |                |     |                | ms    |
| Clk Stabilization <sup>1</sup> | $T_{STAB}$       | From $V_{DD} = 3.3$ V to 1% target Freq. |                |     | 3              | ms    |
| Skew <sup>1</sup>              | $T_{CPU-PCI}$    | $V_T = 1.5$ V; $V_{TL} = 1.25$ V         | 1.0            |     | 4.0            | ms    |
| Skew <sup>1</sup>              | $T_{CPU-SPREAD}$ | $V_T = 1.5$ V; $V_{TL} = 1.25$ V         | 1.0            |     | 4.0            | ns    |

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**Electrical Characteristics - CPUCLK (Open Drain)**

T<sub>A</sub> = 0 - 70° C; V<sub>DD</sub> = 3.3 V +/-5%; C<sub>L</sub> = 20 pF (unless otherwise stated)

| PARAMETER                                   | SYMBOL                 | CONDITIONS                                       | MIN  | TYP | MAX                                 | UNITS |
|---|------------------------|--|------|-----|-------------------------------------|-------|
| Output Impedance                            | Z <sub>O</sub>         | V <sub>O</sub> = V <sub>X</sub>                  |      |     |                                     | Ω     |
| Output High Voltage                         | V <sub>OH2B</sub>      | Termination to V <sub>pull-up(external)</sub>    | 1    |     | 1.2                                 | V     |
| Output Low Voltage                          | V <sub>OL2B</sub>      | Termination to V <sub>pull-up(external)</sub>    |      |     | 0.4                                 | V     |
| Output Low Current                          | I <sub>OL2B</sub>      | V <sub>OL</sub> = 0.3 V                          | 18   |     |                                     | mA    |
| Rise Time <sup>1</sup>                      | t <sub>r2B</sub>       | V <sub>OL</sub> = 0.3 V, V <sub>OH</sub> = 1.2 V |      |     | 0.9                                 | ns    |
| Fall Time <sup>1</sup>                      | t <sub>f2B</sub>       | V <sub>OH</sub> = 1.2 V, V <sub>OL</sub> = 0.3 V |      |     | 0.9                                 | ns    |
| Differential voltage-AC <sup>1</sup>        | V <sub>DIF</sub>       | Note 2   | 0.4  |     | V <sub>pullup(external)</sub> + 0.6 | V     |
| Differential voltage-DC <sup>1</sup>        | V <sub>DIF</sub>       | Note 2   | 0.2  |     | V <sub>pullup(external)</sub> + 0.6 | V     |
| Differential Crossover Voltage <sup>1</sup> | V <sub>X</sub>         | Note 3   | 550  |     | 1100                                | mV    |
| Duty Cycle <sup>1</sup>                     | d <sub>t2B</sub>       | V <sub>T</sub> = 50%                             | 45   |     | 55                                  | %     |
| Skew <sup>1</sup>                           | t <sub>sk2B</sub>      | V <sub>T</sub> = 50%                             |      |     | 200                                 | ps    |
| Jitter, Cycle-to-cycle <sup>1</sup>         | t <sub>jcc-cyc2B</sub> | V <sub>T</sub> = V <sub>X</sub>                  |      |     | 250                                 | ps    |
| Jitter, Absolute <sup>1</sup>               | t <sub>jabs2B</sub>    | V <sub>T</sub> = 50%                             | -250 |     | +250                                | ps    |

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V<sub>DIF</sub> specifies the minimum input differential voltages (V<sub>TR</sub>-V<sub>CP</sub>) required for switching, where V<sub>TR</sub> is the "true" input level and V<sub>CP</sub> is the "complement" input level.

3 - V<sub>pullup(external)</sub> = 1.5V, Min = V<sub>pullup(external)</sub>/2-150mV; Max=(V<sub>pullup(external)</sub>/2)+150mV

**Electrical Characteristics - 24M, 48M, REF, AGP**

T<sub>A</sub> = 0 - 70C; V<sub>DD</sub> = V<sub>DDL</sub> = 3.3 V +/-5%; C<sub>L</sub> = 20 pF (unless otherwise stated)

| PARAMETER           | SYMBOL                         | CONDITIONS                                       | MIN  | TYP | MAX  | UNITS |
|---------------------|--------------------------------|--|------|-----|------|-------|
| Output Impedance    | R <sub>DSP5</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 20   |     | 60   | Ω     |
| Output Impedance    | R <sub>DSN5</sub> <sup>1</sup> | V <sub>O</sub> = V <sub>DD</sub> *(0.5)          | 20   |     | 60   | Ω     |
| Output High Voltage | V <sub>OH5</sub>               | I <sub>OH</sub> = -14 mA                         | 2.4  |     |      | V     |
| Output Low Voltage  | V <sub>OL5</sub>               | I <sub>OL</sub> = 6.0 mA                         |      |     | 0.4  | V     |
| Output High Current | I <sub>OH5</sub>               | V <sub>OH</sub> = 2.0 V                          |      |     | -20  | mA    |
| Output Low Current  | I <sub>OL5</sub>               | V <sub>OL</sub> = 0.8 V                          | 10   |     |      | mA    |
| Rise Time           | t <sub>r5</sub> <sup>1</sup>   | V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V |      |     | 4.0  | ns    |
| Fall Time           | t <sub>f5</sub> <sup>1</sup>   | V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V |      |     | 4.0  | ns    |
| Duty Cycle          | d <sub>t5</sub> <sup>1</sup>   | V <sub>T</sub> = 1.5 V                           | 45.0 |     | 55.0 | %     |
| Jitter              | t <sub>j1s5</sub> <sup>1</sup> | V <sub>T</sub> = 1.5 V                           |      |     | 500  | ps    |

<sup>1</sup>Guarenteed by design, not 100% tested in production.



## Preliminary Product Preview

## Electrical Characteristics - PCI

 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$  (unless otherwise stated)

| PARAMETER           | SYMBOL       | CONDITIONS  | MIN  | TYP | MAX  | UNITS    |
|---------------------|--------------|---|------|-----|------|----------|
| Output Impedance    | $R_{DSP1}^1$ | $V_O = V_{DD}^*(0.5)$                               | 12   |     | 55   | $\Omega$ |
| Output Impedance    | $R_{DSN1}^1$ | $V_O = V_{DD}^*(0.5)$                               | 12   |     | 55   | $\Omega$ |
| Output High Voltage | $V_{OH1}$    | $I_{OH} = -18 \text{ mA}$                           | 2.4  |     |      | V        |
| Output Low Voltage  | $V_{OL1}$    | $I_{OL} = 9.4 \text{ mA}$                           |      |     | 0.4  | V        |
| Output High Current | $I_{OH1}$    | $V_{OH} = 2.0 \text{ V}$                            |      |     | -22  | mA       |
| Output Low Current  | $I_{OL1}$    | $V_{OL} = 0.8 \text{ V}$                            | 25   |     |      | mA       |
| Rise Time           | $t_{r1}^1$   | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ |      |     | 2.0  | ns       |
| Fall Time           | $t_{f1}^1$   | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ |      |     | 2.0  | ns       |
| Duty Cycle          | $d_{t1}^1$   | $V_T = 1.5 \text{ V}$                               | 45.0 |     | 55.0 | %        |
| Skew Window         | $t_{sk1}^1$  | $V_T = 1.5 \text{ V}$                               |      |     | 500  | ps       |
| Jitter              | $t_{j1s1}^1$ | $V_T = 1.5 \text{ V}$                               |      |     | 250  | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.

## Electrical Characteristics - SDRAM

 $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$  (unless otherwise stated)

| PARAMETER           | SYMBOL        | CONDITIONS  | MIN | TYP | MAX   | UNITS    |
|---------------------|---------------|---|-----|-----|-------|----------|
| Output Impedance    | $R_{DSP2A}^1$ | $V_O = V_{DD}^*(0.5)$                               | 10  |     | 20    | $\Omega$ |
| Output Impedance    | $R_{DSN2A}^1$ | $V_O = V_{DD}^*(0.5)$                               | 10  |     | 20    | $\Omega$ |
| Output High Voltage | $V_{OH2A}$    | $I_{OH} = -28 \text{ mA}$                           | 2.4 |     |       | V        |
| Output Low Voltage  | $V_{OL2A}$    | $I_{OL} = 19 \text{ mA}$                            |     |     | 0.4   | V        |
| Output High Current | $I_{OH2A}$    | $V_{OH} = 2.0 \text{ V}$                            |     |     | -42   | mA       |
| Output Low Current  | $I_{OL2A}$    | $V_{OL} = 0.8 \text{ V}$                            | 33  |     |       | mA       |
| Rise Time           | $t_{r2A}^1$   | $V_{OL} = 0.4 \text{ V}$ , $V_{OH} = 2.4 \text{ V}$ | 0.5 |     | 2.0   | ns       |
| Fall Time           | $t_{f2A}^1$   | $V_{OH} = 2.4 \text{ V}$ , $V_{OL} = 0.4 \text{ V}$ | 0.5 |     | 2     | ns       |
| Duty Cycle          | $d_{t2A}^1$   | $V_T = 1.5 \text{ V}$                               | 45  |     | 55    | %        |
| Jitter <sup>1</sup> | $t_{cyc-cyc}$ | $V_T = 1.5 \text{ V}$                               |     |     | 250.0 | ps       |

<sup>1</sup>Guaranteed by design, not 100% tested in production.





## General I<sup>2</sup>C serial interface information

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**  
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8)**.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation     |           |                      |
|---------------------------------|-----------|----------------------|
| Controller (Host)               |           | ICS (Slave/Receiver) |
| T                               | starT bit |                      |
| Slave Address D2 <sub>(H)</sub> |           |                      |
| WR                              | WRite     |                      |
|                                 |           | ACK                  |
| Beginning Byte = N              |           |                      |
|                                 |           | ACK                  |
| Data Byte Count = X             |           |                      |
|                                 |           | ACK                  |
| Beginning Byte N                |           | X Byte               |
| ○                               |           |                      |
| ○                               |           |                      |
| ○                               |           |                      |
| Byte N + X - 1                  |           |                      |
|                                 |           | ACK                  |
| P                               | stoP bit  |                      |

| Index Block Read Operation      |                 |                      |
|---------------------------------|-----------------|----------------------|
| Controller (Host)               |                 | ICS (Slave/Receiver) |
| T                               | starT bit       |                      |
| Slave Address D2 <sub>(H)</sub> |                 |                      |
| WR                              | WRite           |                      |
|                                 |                 | ACK                  |
| Beginning Byte = N              |                 |                      |
|                                 |                 | ACK                  |
| RT                              | Repeat starT    |                      |
| Slave Address D3 <sub>(H)</sub> |                 |                      |
| RD                              | ReaD            |                      |
|                                 |                 | ACK                  |
|                                 |                 | Data Byte Count = X  |
| ACK                             |                 | X Byte               |
| ACK                             |                 |                      |
| ○                               |                 |                      |
| ○                               |                 |                      |
| ○                               |                 |                      |
| Byte N + X - 1                  |                 |                      |
| N                               | Not acknowledge |                      |
| P                               | stoP bit        |                      |

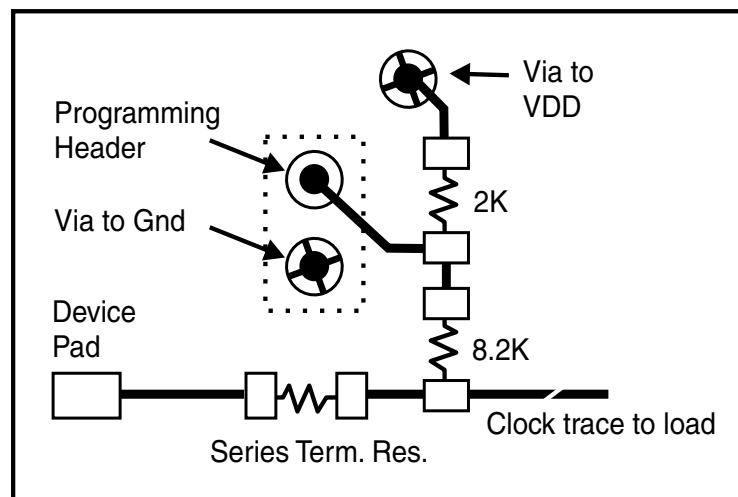


### Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-179 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

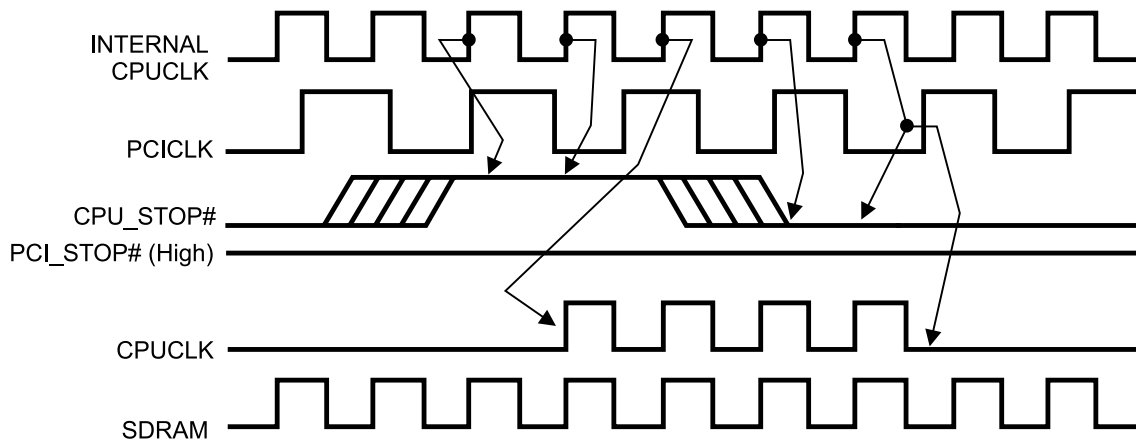


**Fig. 1**



### CPU\_STOP# Timing Diagram

CPU\_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU\_STOP# is synchronized by the ICS9248-179. The minimum that the CPU clock is enabled (CPU\_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



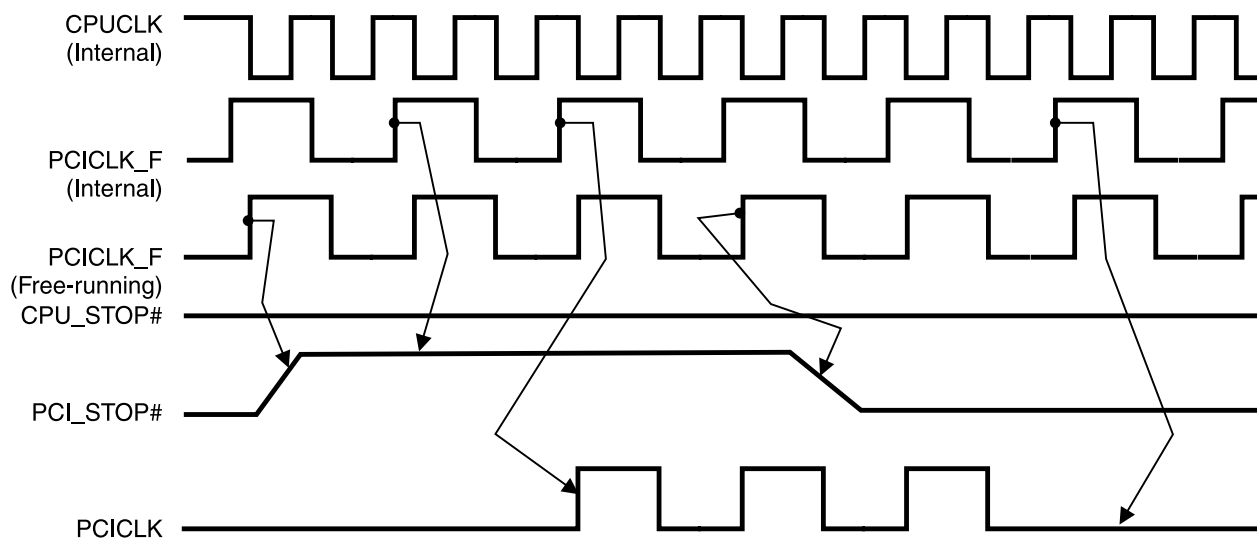
**Notes:**

1. All timing is referenced to the internal CPU clock.
2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9248-179.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).



### PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the **ICS9248-179**. It is used to turn off the PCICLK clocks for low power operation. PCI\_STOP# is synchronized by the **ICS9248-179** internally. The minimum that the PCICLK clocks are enabled (PCI\_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



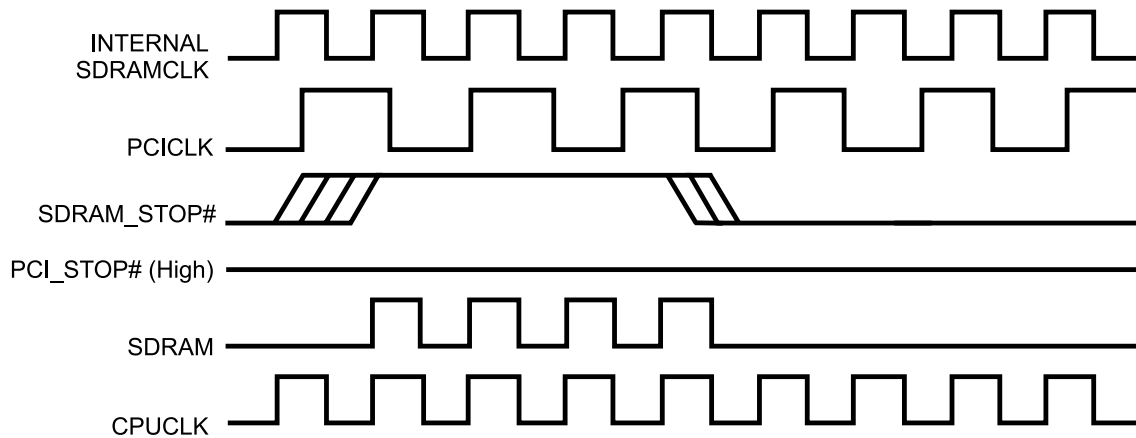
#### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-179 device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9248-179.
3. All other clocks continue to run undisturbed.
4. CPU\_STOP# is shown in a high (true) state.



### SDRAM\_STOP# Timing Diagram

SDRAM\_STOP# is an asynchronous input to the clock synthesizer. It is used to stop SDRAM clocks for low power operation. SDRAM\_STOP# is synchronized to complete its current cycle, by the **ICS9248-179**. All other clocks will continue to run while the SDRAM clocks are disabled. The SDRAM clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse.



**Notes:**

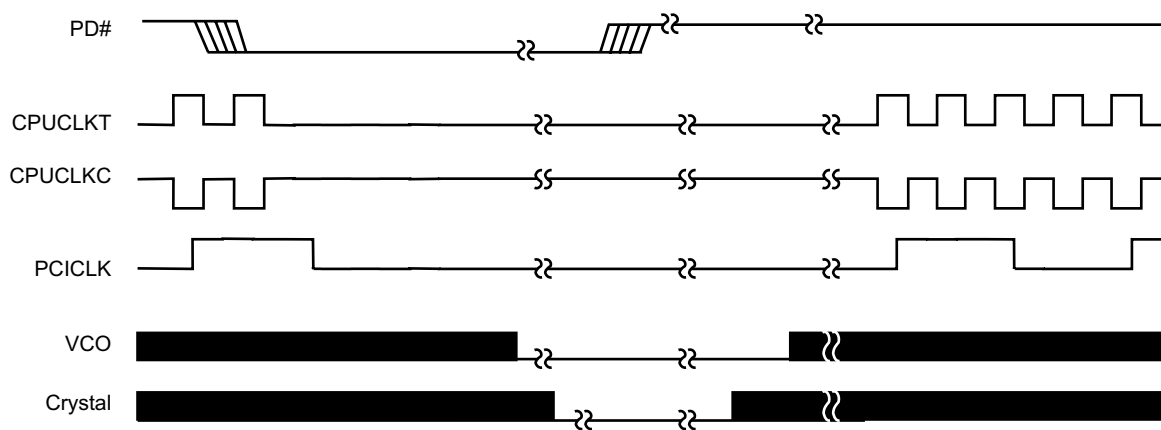
- 1. All timing is referenced to the internal CPU clock.
- 2. SDRAM is an asynchronous input and metastable conditions may exist. This signal is synchronized to the SDRAM clocks inside the ICS9248-179.
- 3. All other clocks continue to run undisturbed.



### PD# Timing Diagram

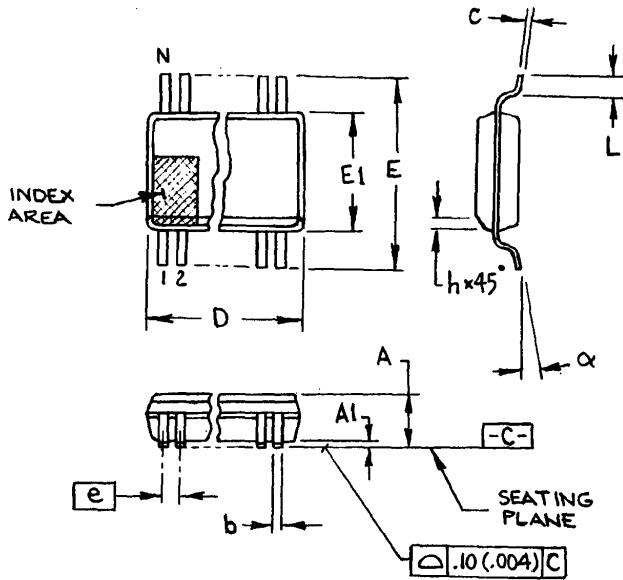
The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI\_STOP# and CPU\_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



#### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248-179 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



300 mil SSOP

| SYMBOL | In Millimeters<br>COMMON DIMENSIONS |        | In Inches<br>COMMON DIMENSIONS |       |
|--------|-------------------------------------|--------|--------------------------------|-------|
|        | MIN                                 | MAX    | MIN                            | MAX   |
| A      | 2.413                               | 2.794  | .095                           | .110  |
| A1     | 0.203                               | 0.406  | .008                           | .016  |
| b      | 0.203                               | 0.343  | .008                           | .0135 |
| c      | 0.127                               | 0.254  | .005                           | .010  |
| D      | SEE VARIATIONS                      |        | SEE VARIATIONS                 |       |
| E      | 10.033                              | 10.668 | .395                           | .420  |
| E1     | 7.391                               | 7.595  | .291                           | .299  |
| e      | 0.635 BASIC                         |        | 0.025 BASIC                    |       |
| h      | 0.381                               | 0.635  | .015                           | .025  |
| L      | 0.508                               | 1.016  | .020                           | .040  |
| N      | SEE VARIATIONS                      |        | SEE VARIATIONS                 |       |
| α      | 0°                                  | 8°     | 0°                             | 8°    |

VARIATIONS

| N  | D mm.  |        | D (inch) |      |
|----|--------|--------|----------|------|
|    | MIN    | MAX    | MIN      | MAX  |
| 48 | 15.748 | 16.002 | .620     | .630 |

JEDEC MO-118  
DOC# 10-0034  
6/1/00  
REV B

Ordering Information

ICS9248yF-179-T

Example:

ICS XXXX y F - PPP - T

