Integrated Circuit Systems, Inc.

ICS9248-134

Frequency Timing Generator for PENTIUM II/III Systems

Recommended Application:
For Intel Camino Style Chipsets

Output Features:

- 3 - CPUs @ 2.5V, up to 180MHz.
- 1 - CPU/2 @ 2.5V.
- 3 - IOAPIC @ 2.5V, PCI or PCI/2
- 3 - 3V66MHz @ 3.3V.
- 11 - PCIs @ 3.3V
- 1 - 48MHz, @ 3.3V fixed
- 1 - 24/48MHz, @ 3.3V

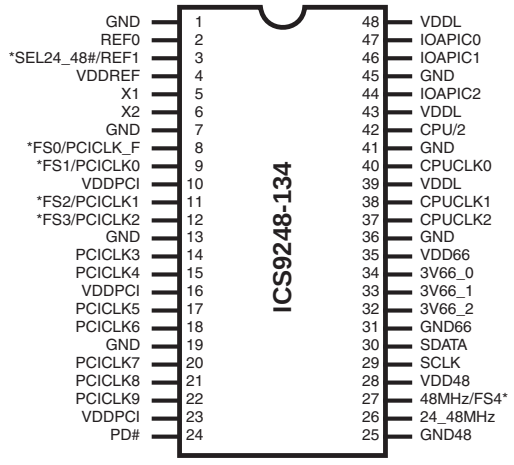
Features:

- Support power management: Power down Mode from I^2C programming.
- Spread spectrum for EMI control ± 0.25% center spread).
- Uses external 14.318MHz crystal

Key Specifications:

- CPU Output Jitter: <250ps
- IOAPIC Output Jitter: <500ps
- 48MHz, 3V66, PCI Output Jitter: <500ps)

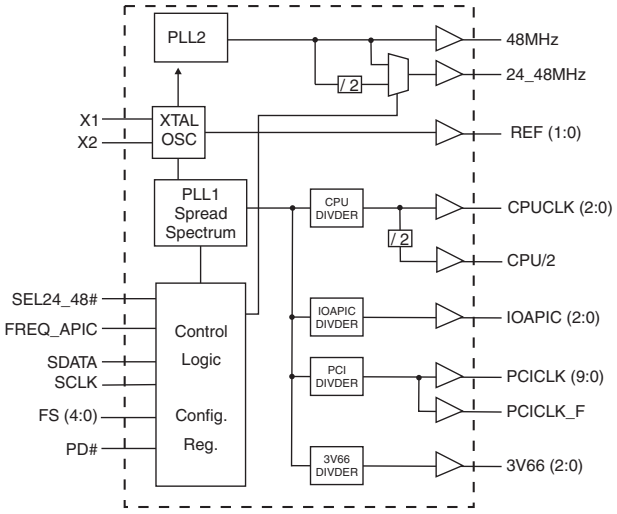
Pin Configuration



48-pin SSOP

*120K ohm pull-up to VDD on indicated inputs.

Block Diagram



Functionality

FS4	FS3	FS2	FS1	FS0	CPU	PCI	3V66	IOAPIC
0	0	0	0	0	103.00	34.33	68.67	17.17
0	0	0	0	1	105.00	35.00	70.00	17.50
0	0	0	1	0	100.45	33.483	66.967	16.742
0	0	0	1	1	100.90	33.63	67.27	16.82
0	0	1	0	0	107.10	35.700	71.400	17.850
0	0	1	0	1	109.00	36.33	72.67	18.17
0	0	1	1	0	112.00	37.34	74.67	18.67
0	0	1	1	1	114.00	28.50	57.00	14.25
0	1	0	0	0	116.00	29.00	58.00	14.50
0	1	0	0	1	118.00	29.50	59.00	14.75
0	1	0	1	0	133.30	33.33	66.65	16.66
0	1	0	1	1	120.00	30.00	60.00	15.00
0	1	1	0	0	122.00	30.50	61.00	15.25
0	1	1	0	1	125.00	31.25	62.50	15.63
0	1	1	1	0	128.21	32.05	64.105	16.026
0	1	1	1	1	130.00	32.50	65.00	16.25
1	0	0	0	0	132.00	33.00	66.00	16.50
1	0	0	0	1	133.90	33.48	66.95	16.74
1	0	0	1	0	138.00	34.50	69.00	17.25
1	0	0	1	1	142.00	35.50	71.00	17.75
1	0	1	0	0	146.00	36.50	73.00	18.25
1	0	1	0	1	150.00	37.50	75.00	18.75
1	0	1	1	0	153.00	38.25	76.50	19.13
1	0	1	1	1	156.00	39.00	78.00	19.50
1	1	0	0	0	159.00	39.75	79.50	19.88
1	1	0	0	1	162.00	40.50	81.00	20.25
1	1	0	1	0	165.00	41.25	82.50	20.63
1	1	0	1	1	168.00	42.00	84.00	21.00
1	1	1	0	0	171.00	42.75	85.50	21.38
1	1	1	0	1	174.00	43.50	87.00	21.75
1	1	1	1	0	177.00	44.25	88.50	22.13
1	1	1	1	1	180.00	45.00	90.00	22.50

General Description

The **ICS9248-134** is a main clock synthesizer chip for Pentium II based systems using Rambus Interface DRAMs. This chip provides all the clocks required for such a system when used with a Direct Rambus Clock Generator(DRCG) chip such as the ICS9212-01.

Spread Spectrum may be enabled by driving the SPREAD# pin active. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9248-134** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

The CPU/2 clocks are inputs to the DRCG.

Pin Descriptions

Pin number	Pin name	Type	Description
1, 7, 13, 19, 25, 31, 36, 41, 45	GND	PWR	Ground pins
2	REF0	OUT	14.318MHz reference clock outputs at 3.3V
3	REF1	OUT	14.318MHz reference clock outputs at 3.3V
	SEL24_48	IN	Logic input to select 24 or 48MHz for pin 26 output
4, 10, 16, 23, 28, 35	VDD	PWR	Power pins 3.3V
5	X1	IN	XTAL_IN 14.318MHz crystal input
6	X2	OUT	XTAL_OUT Crystal output
8	PCICLK_F	OUT	Free running PCI clock at 3.3V. Synchronous to CPU clocks. Not affected by the PCI_STOP# input.
	FS0	IN	Logic - input for frequency selection
9	PCICLK0	OUT	PCI clock output at 3.3V. Synchronous to CPU clocks.
	FS1	IN	Logic - input for frequency selection
11	PCICLK1	OUT	PCI clock output at 3.3V. Synchronous to CPU clocks.
	FS2	IN	Logic - input for frequency selection
12	PCICLK2	OUT	PCI clock output at 3.3V. Synchronous to CPU clocks.
	FS3	IN	Logic - input for frequency selection
14, 15, 17, 18, 20, 21, 22	PCICLK (9:3)	OUT	PCI clock outputs at 3.3V. Synchronous to CPU clocks.
24	PD#	IN	This asynchronous input powers down the chip when drive active(Low). The internal PLLs are disabled and all the output clocks are held at a Low state.
26	24_48MHz	OUT	24 or 48MHz output selectable by SEL24_48# (0=48MHz 1=24MHz)
27	48MHz	OUT	Fixed 48MHz clock output. 3.3V
	FS4	IN	Logic - input for frequency selection
29	SCLK	IN	Clock input of I^2C input
30	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
32, 33, 34	3V66 (2:0)	OUT	3.3V clock outputs. These outputs are stopped when CPU_STOP# is driven active..
37, 38, 40	CPUCLK (2:0)	OUT	Host bus clock output at 2.5V.
42	CPU/2	OUT	2.5V clock outputs at 1/2 CPU frequency.
39, 43, 48	VDDL	PWR	Power pins for the CPU, CPU/2 & IOAPIC clocks. 2.5V
44, 46, 47	IOAPIC (2:0)	OUT	IOAPIC clocks at 2.5V. Synchronous with CPUCLKs.

Serial Configuration Command Bitmap

Byte 0: Functionality and frequency select register (Default = 0)

Bit	Description										PWD
	Bit 2 FS4	**Bit 7 FS3**	**Bit 6 FS2**	**Bit 5 FS1**	**Bit 4 FS0**	**CPU**	**CPU/2**	**PCI**	**3V66**	**IOAPIC**	
Bit 2, 7:4	0	0	0	0	0	103.00	51.50	34.33	68.67	17.17	Reserved Note 1
	0	0	0	0	1	105.00	52.50	35.00	70.00	17.50	
	0	0	0	1	0	100.45	50.225	33.483	66.967	16.742	
	0	0	0	1	1	100.90	50.45	33.63	67.27	16.82	
	0	0	1	0	0	107.10	53.550	35.700	71.400	17.850	
	0	0	1	0	1	109.00	54.50	36.33	72.67	18.17	
	0	0	1	1	0	112.00	56.00	37.34	74.67	18.67	
	0	0	1	1	1	114.00	57.00	28.50	57.00	14.25	
	0	1	0	0	0	116.00	58.00	29.00	58.00	14.50	
	0	1	0	0	1	118.00	59.00	29.50	59.00	14.75	
	0	1	0	1	0	133.30	66.65	33.33	66.65	16.66	
	0	1	0	1	1	120.00	60.00	30.00	60.00	15.00	
	0	1	1	0	0	122.00	61.00	30.50	61.00	15.25	
	0	1	1	0	1	125.00	62.50	31.25	62.50	15.63	
	0	1	1	1	0	128.21	64.105	32.05	64.105	16.026	
	0	1	1	1	1	130.00	65.00	32.50	65.00	16.25	
	1	0	0	0	0	132.00	66.00	33.00	66.00	16.50	
	1	0	0	0	1	133.90	66.95	33.48	66.95	16.74	
	1	0	0	1	0	138.00	69.00	34.50	69.00	17.25	
	1	0	0	1	1	142.00	71.00	35.50	71.00	17.75	
	1	0	1	0	0	146.00	73.00	36.50	73.00	18.25	
	1	0	1	0	1	150.00	75.00	37.50	75.00	18.75	
	1	0	1	1	0	153.00	76.50	38.25	76.50	19.13	
	1	0	1	1	1	156.00	78.00	39.00	78.00	19.50	
	1	1	0	0	0	159.00	79.50	39.75	79.50	19.88	
	1	1	0	0	1	162.00	81.00	40.50	81.00	20.25	
	1	1	0	1	0	165.00	82.50	41.25	82.50	20.63	
	1	1	0	1	1	168.00	84.00	42.00	84.00	21.00	
	1	1	1	0	0	171.00	85.50	42.75	85.50	21.38	
	1	1	1	0	1	174.00	87.00	43.50	87.00	21.75	
	1	1	1	1	0	177.00	88.50	44.25	88.50	22.13	
	1	1	1	1	1	180.00	90.00	45.00	90.00	22.50	
Bit 3	0 - Frequency is selected by hardware select, latched inputs 1 - Frequency is selected by Bit 2, 7:4										0
Bit 1	0 - Spread Spectrum disabled 1 - Spread spectrum enabled										1
Bit 0	0 - Running 1 - Tristate all outputs										0

Note 1:

Default at power-up will be latched logic inputs to define frequency, as displayed by Bit 1.

Byte 1: CPU, Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	40	1	CPUCLK 0
Bit 6	38	1	CPUCLK 1
Bit 5	37	1	CPUCLK 2
Bit 4	42	1	CPU/2
Bit 3	47	1	IOAPIC0
Bit 2	46	1	IOAPIC1
Bit 1	44	1	IOAPIC2
Bit 0	-	X	(Reserved)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 2: PCI Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	18	1	PCICLK7
Bit 6	17	1	PCICLK6
Bit 5	15	1	PCICLK5
Bit 4	14	1	PCICLK4
Bit 3	12	1	PCICLK3
Bit 2	11	1	PCICLK2
Bit 1	9	1	PCICLK1
Bit 0	8	1	PCICLK_F

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 3: 3V66 Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	34	1	3V66_0
Bit 6	33	1	3V66_1
Bit 5	32	1	3V66_2
Bit 4	-	X	FS1#
Bit 3	3	1	REF1
Bit 2	2	1	REF0
Bit 1	-	X	FS3#
Bit 0	-	X	FS2#

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 4: PCI Active/Inactive Register
(1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	26	1	24_48MHz
Bit 6	27	1	48MHz
Bit 5	-	X	FS0#
Bit 4	-	1	(Reserved)
Bit 3	22	1	PCICLK10
Bit 2	21	1	PCICLK9
Bit 1	20	1	PCICLK8
Bit 0	-	X	FS4#

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte 5: Active/Inactive Register
(1= enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit7	-	1	Reserved (Note)
Bit6	-	1	Reserved (Note)
Bit5	-	1	Reserved (Note)
Bit4	-	1	Reserved (Note)
Bit3	-	1	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	1	Reserved (Note)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.

Byte6: Active/Inactive Register
(1= enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Absolute Maximum Ratings

Supply Voltage ..... 5.5 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C
Case Temperature ..... 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}		0.1	5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5	2.0		µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200	-100		µA
Operating Supply Current	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100 MHz		71	160	mA
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133 MHz		76	160	mA
Input frequency	F_i	V_{DD} = 3.3 V;	11	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.		5		ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	$I_{DD2.5OP100}$	C_L = 0 pF; Select @ 100 MHz		15	75	mA
	$I_{DD2.5OP133}$	C_L = 0 pF; Select @ 133 MHz		18	90	mA
Power Down Supply Current	$I_{DD2.5PD}$	C_L = 0 pF; PWRDWN# = 0		272	400	µA

[1]Guaranteed by design, not 100% tested in production.

Group Offset

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

GROUP	OFFSET	MEASUREMENT LOADS	MEASURE POINTS
CPU to 3V66	0.0-1.5 ns; CPU leads.	CPU @ 20pF, 3V66 @ 30pF	CPU @ 1.25V, 3V66 @ 1.5V
3V66 to PCI	0.5-4.0 ns; 3V66 leads.	3V66 @ 30pF, PCI @ 30pF	3V66 @ 1.5V, PCI @ 1.5V
CPU to IOAPIC	0.5-4.0 ns; CPU leads.	CPU @ 20pF, IOAPIC @ 20pF	CPU @ 1.25V, IOAPIC @ 1.25V
CPU to PCI	0.5-4.0 ns; CPU leads.	CPU @ 20pF, PCI @ 30pF	CPU @ 1.25V, PCI @ 1.5V

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$V_O = V_{DD}*(0.5)$	13.5	30	45	Ω
Output Impedance[1]	R_{DSN2B}	$V_O = V_{DD}*(0.5)$	13.5	32	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.24		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12.0 mA		0.31	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-31	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	25		mA
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.1	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.4	1.8	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V; CPU frequencies < 135 MHz	45	50	55	%
Skew[1]	t_{sk2B}	V_T = 1.25 V		53	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V; CPU frequencies <135 MHz		179	275	ps
		V_T = 1.25 V; CPU frequencies >=135 MHz		231	350	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU/2

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	$V_O = V_{DD}*(0.5)$	13.5	30	45	Ω
Output Impedance[1]	R_{DSN2B}	$V_O = V_{DD}*(0.5)$	13.5	31	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2	2.2		V
Output Low Voltage	V_{OL2B}	I_{OL} = 12.0 mA		0.31	0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V		-31	-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19	26		mA
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.1	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.1	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45	49	55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V; CPU frequencies <135 MHz		227	275	ps
		V_T = 1.25 V; CPU frequencies >=135 MHz		306	350	

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1}	$V_O = V_{DD}*(0.5)$	12	24	55	Ω
Output Impedance[1]	R_{DSN1}	$V_O = V_{DD}*(0.5)$	12	23	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.17	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-51	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	41		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.4	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.5	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		89	250	ps
Jitter, Cycle-to-cycle[1]	$T_{jcyc-cyc1}$	V_T = 1.5 V		173	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1}	$V_O = V_{DD}*(0.5)$	12	24	55	Ω
Output Impedance[1]	R_{DSN1}	$V_O = V_{DD}*(0.5)$	12	23	55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4	3.1		V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA		0.16	0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V		-50	-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16	42		mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.8	2.5	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.5	2.5	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	50	55	%
Skew Window[1]	t_{sk1}	V_T = 1.5 V, $PCICLK_{(F:7)}$		260	350	ps
		V_T = 1.5 V, $PCICLK_{(8:10)}$		211	250	
		V_T = 1.5 V, $PCICLK_{(F:10)}$		466	600	
Jitter, Cycle-to-cycle[1]	$T_{jcyc-cyc1}$	V_T = 1.5 V		280	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48 MHz, 24_48 MHz

T_A = 0 - 70ºC; V_{DD} = 3.3 V +/-5%; V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}*(0.5)$	20	47	60	Ω
Output Impedance[1]	R_{DSN5}	$V_O = V_{DD}*(0.5)$	20	44	60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4	2.62		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-27	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.1	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	51	55	%
Jitter, Cycle-to-cycle[1]	$T_{jcyc-cyc5}$	V_T = 1.5 V		375	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70ºC; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}*(0.5)$	20	48	60	Ω
Output Impedance[1]	R_{DSN5}	$V_O = V_{DD}*(0.5)$	20	44	60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4	2.6		V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA		0.3	0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V		-26	-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16	22		mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.1	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jitter, Cycle-to-cycle[1]	$T_{jcyc-cyc5}$	V_T = 1.5 V		839	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP4B}	$V_O = V_{DD}*(0.5)$	13.5	26	45	Ω
Output Impedance[1]	R_{DSN4B}	$V_O = V_{DD}*(0.5)$	13.5	31	45	Ω
Output High Voltage	V_{OH4B}	I_{OH} = -12.0 mA	2	2.24		V
Output Low Voltage	V_{OL4B}	I_{OL} = 12.0 mA		0.31	0.4	V
Output High Current	I_{OH4B}	V_{OH} = 1.7 V		-31	-19	mA
Output Low Current	I_{OL4B}	V_{OL} = 0.7 V	19	26		mA
Rise Time[1]	T_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V		1.6	2	ns
Fall Time[1]	T_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V		1.6	2	ns
Duty Cycle[1]	D_{t4B}	V_T = 1.25 V	45	49	55	%
Skew [1]	t_{sk4B}	V_T = 1.25 V		139	250	ps
Jitter, Cycle-to-cycle[1]	$T_{jcyc-cyc4B}$	V_T = 1.25 V		245	500	ps

[1]Guaranteed by design, not 100% tested in production.

Power Management Features:

PD#	CPUCLK	CPU/2	IOAPIC	3V66	PCI	PCI_F	REF. 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON	ON

Note:

1. LOW means outputs held static LOW as per latency requirement next page.
2. On means active.
3. PD# pulled Low, impacts all outputs including REF and 48 MHz outputs.

Power Management Requirements:

Signal	Signal State	Latency
		No. of rising edges of PCICLK
PD#	1 (normal operation)	3mS
	0 (power down)	2max.

Note:

1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/ high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high to when the first valid clocks are dirven from the device.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

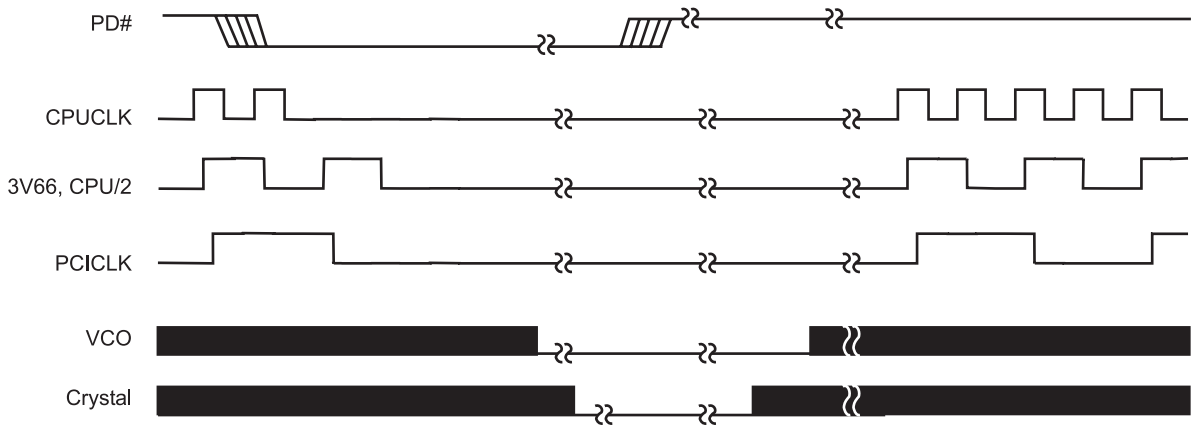
Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

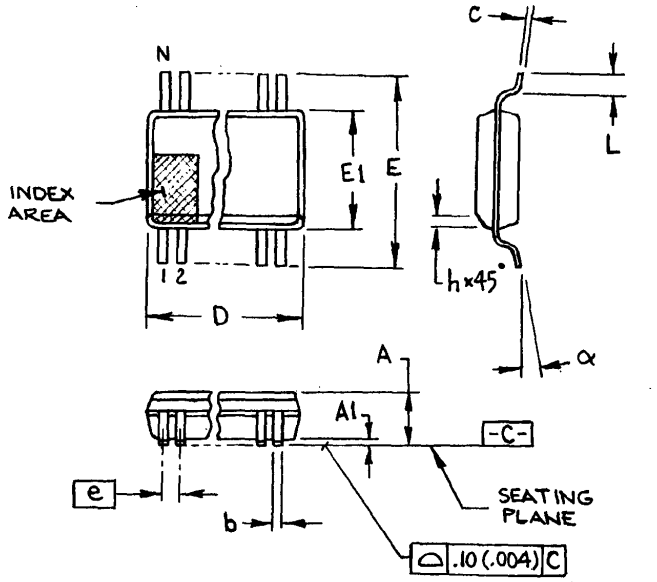
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.413	2.794	.095	.110
A1	0.203	0.406	.008	.016
b	0.203	0.343	.008	.0135
c	0.127	0.254	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.033	10.668	.395	.420
E1	7.391	7.595	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.381	0.635	.015	.025
L	0.508	1.016	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.398	9.652	.370	.380
34	11.303	11.557	.445	.455
48	15.748	16.002	.620	.630
56	18.288	18.542	.720	.730
64	20.828	21.082	.820	.830

JEDEC MO-118 6/1/00
DOC# 10-0034 REVB

Ordering Information

ICS9248yF-134-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device