Integrated Circuit Systems, Inc.

ICS9248-102

Frequency Generator & Integrated Buffers for Celeron & PII/III™ & K6

Recommended Application:

Motherboard Single chip clock solution for Pentium II/III and K6 processors, using SIS540/SIS630 style chipset

Output Features:

- 3- CPUs @ 2.5/3.3V, up to 166MHz.
- 14 - SDRAM @ 3.3V, up to166MHz.
- 7- PCI @3.3V,
- 1- 48MHz, @3.3V fixed.
- 1- 24/48MHz, @3.3V selectable by I^2C (Default is 24MHz).
- 2- REF @3.3V, 14.318MHz.

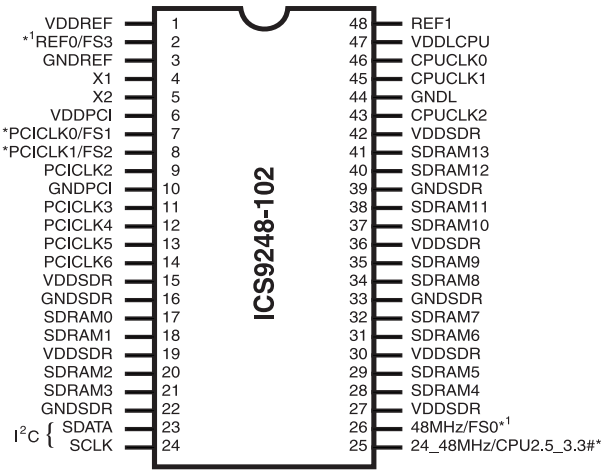
Features:

- Up to 166MHz frequency support
- Support FS0-FS3 trapping status bit for I^2C read back.
- Support power management: CPU, PCI, SDRAM stop and Power down Mode from I^2C programming.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%).
- FS0, FS1, FS3 must have a internal 120K pull-Down to GND.
- Uses external 14.318MHz crystal

Skew Specifications:

- CPU - CPU: < 175ps
- SDRAM - SDRAM < 250ps
- PCI - PCI: < 500ps
- CPU - SDRAM: < 500ps
- CPU (early) - PCI: 1-4ns (typ. 2ns)

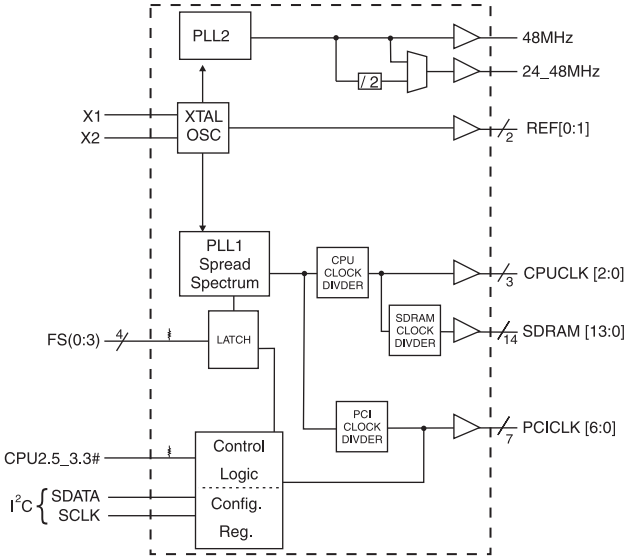
Pin Configuration



48-Pin 300mil SSOP

* These inputs have a 120K pull down to GND.
1 These are double strength.

Block Diagram



Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	SDRAM (MHz)	PCICLK (MHz)	REF (MHz)
0	0	0	0	66.82	100.20	33.41	14.318
0	0	0	1	100.23	100.00	33.41	14.318
0	0	1	0	150.34	100.00	37.59	14.318
0	0	1	1	133.64	100.00	33.41	14.318
0	1	0	0	66.82	133.00	33.41	14.318
0	1	0	1	100.23	133.33	33.41	14.318
0	1	1	0	100.23	150.00	37.59	14.318
0	1	1	1	133.64	133.10	33.41	14.318
1	0	0	0	66.82	66.75	33.41	14.318
1	0	0	1	83.33	83.30	27.78	14.318
1	0	1	0	90.00	90.00	30.00	14.318
1	0	1	1	95.00	95.00	31.67	14.318
1	1	0	0	95.00	126.67	31.67	14.318
1	1	0	1	112.01	112.00	37.34	14.318
1	1	1	0	166.00	111.00	27.67	14.318
1	1	1	1	166.00	166.50	27.67	14.318

General Description

The **ICS9248-102** is the single chip clock solution for Desktop/Notebook designs using the SIS 540/630 style chipset. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9248-102
employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Power Groups

VDDREF = REF [1:0], X1, X2
VDDPCI = PCICLK_F, PCICLK [9:0]
VDDSDR = SDRAM [11:0], supply for PLL core,
VDD48 = 48MHz, 24MHz
VDDLIOAPIC = IOAPIC_F
VDDLCPU = CPUCLK_F [2:1]

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 6, 15, 19, 27, 30, 36, 42	VDD	PWR	3.3V Power supply for SDRAM output buffers, PCI output buffers, reference output buffers and 48MHz output
2	REF0	OUT	14.318 MHz reference clock.
	FS3	IN	Frequency select pin.
3, 10, 16, 22, 33, 39, 44	GND	PWR	Ground pin for 3V outputs.
4	X1	IN	Crystal input,nominally 14.318MHz.
5	X2	OUT	Crystal output, nominally 14.318MHz.
7	FS1	IN	Frequency select pin.
	PCICLK0	OUT	PCI clock outputs.
8	FS2	IN	Frequency select pin.
	PCICLK1	OUT	PCI clock outputs.
9, 11, 12, 13, 14	PCICLK [2:6]	OUT	PCI clock outputs.
41, 40, 38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17	SDRAM	OUT	SDRAM clock outputs
23	SDATA	IN	Data input for I2C serial input, 5V tolerant input
24	SCLK	IN	Clock input of I2C input, 5V tolerant input
25	CPU2.5_3.3#	IN	Voltage select 2.5V when high - 3.3V when low
	24_48MHz	OUT	Clock output for super I/O/USB default is 24MHz
26	FS0	IN	Frequency select pin.
	48MHz	OUT	48MHz output clock
46, 45, 43	CPUCLK [0:2]	OUT	CPU clock outputs.
47	VDDLCPU	PWR	Power pin for the CPUCLKs. 2.5V
48	REF0	OUT	14.318 MHz reference clock.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description									PWD
	Bit7	Bit2	Bit6	Bit5	Bit4	CPU	SDRAM	PCI	SS%	
Bit 7, 2, Bit 6:4	0	0	0	0	0	66.82	100.20	33.41	±0.25%	00001 Note1
	0	0	0	0	1	100.23	100.00	33.41	±0.25%	
	0	0	0	1	0	150.34	100.00	37.59	±0.25%	
	0	0	0	1	1	133.64	100.00	33.41	±0.25%	
	0	0	1	0	0	66.82	133.00	33.41	±0.25%	
	0	0	1	0	1	100.23	133.33	33.41	±0.25%	
	0	0	1	1	0	100.23	150.00	37.59	±0.25%	
	0	0	1	1	1	133.64	133.10	33.41	±0.25%	
	0	1	0	0	0	66.82	66.75	33.41	±0.25%	
	0	1	0	0	1	83.33	83.30	27.78	±0.25%	
	0	1	0	1	0	90.00	90.00	30.00	±0.25%	
	0	1	0	1	1	95.00	95.00	31.67	±0.25%	
	0	1	1	0	0	95.00	126.67	31.67	±0.25%	
	0	1	1	0	1	112.01	112.00	37.34	±0.25%	
	0	1	1	1	0	166.00	111.00	27.67	±0.25%	
	0	1	1	1	1	166.00	166.50	27.67	±0.25%	
	1	0	0	0	0	66.66	100.00	35.33	0 to-0.5%	
	1	0	0	0	1	100.00	100.00	33.33	0 to-0.5%	
	1	0	0	1	0	96.25	96.25	32.08	±0.25%	
	1	0	0	1	1	133.33	100.00	33.33	0 to-0.5%	
	1	0	1	0	0	75.00	100.00	37.50	±0.25%	
	1	0	1	0	1	83.34	125.01	31.25	±0.25%	
	1	0	1	1	0	105.00	140.00	35.00	±0.25%	
	1	0	1	1	1	133.33	133.33	33.3	±0.25%	
	1	1	0	0	0	110.25	147.00	36.75	±0.25%	
	1	1	0	0	1	115.02	153.36	38.34	±0.25%	
	1	1	0	1	0	120.00	120.00	30.00	±0.25%	
	1	1	0	1	1	138.01	138.01	34.50	±0.25%	
	1	1	1	0	0	140.00	140.00	35.00	±0.25%	
	1	1	1	0	1	145.05	145.05	36.26	±0.25%	
	1	1	1	1	0	147.59	147.59	36.90	±0.25%	
	1	1	1	1	1	160.01	160.01	26.67	±0.25%	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 7, 2, 6:4									0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled									1
Bit 0	0 - Running 1- Tristate all outputs									0

Note1:
Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.
The I^2C readback for Bits 7, 2, 6:4 indicate the revision code.

Note: PWD = Power-Up Default

I^2C is a trademark of Philips Corporation

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	SEL24_48# (48MHz when set to 0) (24MHz when set to 1)
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	43	1	CPUCLK2 (Act/Inact)
Bit 2	45	1	CPUCLK1 (Act/Inact)
Bit 1	46	1	CPUCLK0 (Act/Inact)
Bit 0	-	1	Reserved

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(CPU2.5_3.3#)
Bit 6	14	1	PCICLK6 (Act/Inact)
Bit 5	13	1	PCICLK5 (Act/Inact)
Bit 4	12	1	PCICLK4 (Act/Inact)
Bit 3	11	1	PCICLK3 (Act/Inact)
Bit 2	9	1	PCICLK2 (Act/Inact)
Bit 1	8	1	PCICLK1 (Act/Inact)
Bit 0	7	1	PCICLK0 (Act/Inact)

Byte 3: SDRAM, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	32	1	SDRAM 7 (Act/Inact)
Bit 6	31	1	SDRAM 6 (Act/Inact)
Bit 5	29	1	SDRAM 5 (Act/Inact)
Bit 4	28	1	SDRAM 4 (Act/Inact)
Bit 3	21	1	SDRAM 3 (Act/Inact)
Bit 2	20	1	SDRAM 2 (Act/Inact)
Bit 1	18	1	SDRAM 1 (Act/Inact)
Bit 0	17	1	SDRAM 0 (Act/Inact)

Byte 4: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	25	1	24_48MHz
Bit 6	26	1	48MHz
Bit 5	41	1	SDRAM13
Bit 4	40	1	SDRAM12
Bit 3	38	1	SDRAM11
Bit 2	37	1	SDRAM10
Bit 1	35	1	SDRAM9
Bit 0	34	1	SDRAM8

Byte 5: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	FS3#
Bit 4	-	1	FS2#
Bit 3	-	1	FS1#
Bit 2	-	1	FS0#
Bit 1	48	1	REF1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inferted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-102 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

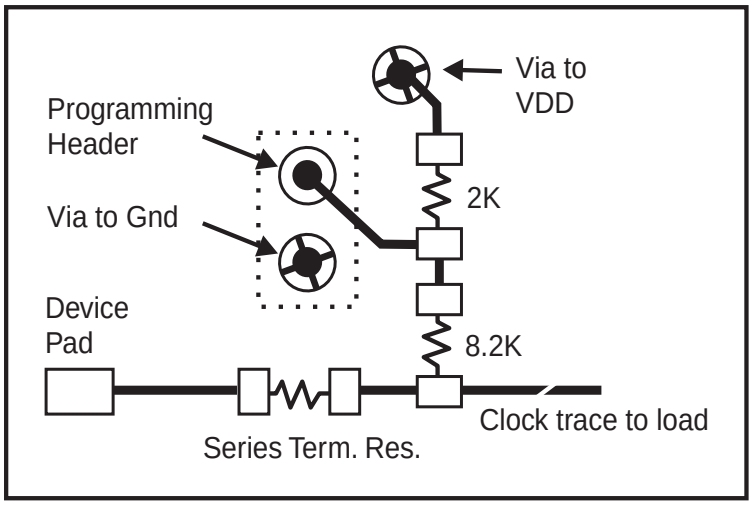


Fig. 1

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Supply Current	I_{DD}				180	mA
	I_{DDL}	CL = 0 pF; Select @ 66M			30	mA
Input frequency	F_i	V_{DD} = 3.3 V;				MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	ps
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.				ms
Clk Stabilization[1]	T_{STAB}	From = 3.3 V to 1% target Freq			3	ms
Skew1	TCPU-PCI	VT = 1.5 V;	1	2.58	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; V_{DD} = 3.3V +/-5%; C_L= 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}	$V_O = V_{DD}*(0.5)$ Output P	10		20	Ω
Output Impedance	R_{DSN2A}	$V_O = V_{DD}*(0.5)$ Output P	10		20	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	tr_{2A}	V_{OL} =0.4 V, V_{OH} = 2.4 V	0.4	1.17	2	ns
Fall Time	t_{f2A}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	1.515	2	ns
Duty Cycle	d_{t2A}	V_T = 1.25 V	45	51.15	55	%
$Skew_{(Window)}$	t_{sk2A}	V_T = 1.25 V		69.5	175	ps
Jitter	jitter			190	250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24M, 48M, REF 1

T_A = 0 - 70C; V_{DD} = V_{DDL} = 3.3 V +/- 5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP5}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance	R_{DSN5}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -14 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 6.0 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-20	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	10			mA
Rise Time	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		2.25	4	ns
Fall Time	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		2.19	4	ns
Duty Cycle	d_{t5}	V_T = 1.5 V	45	50.3	55	%
Jitter (cyc to cyc)	t_{j1s5}	V_T = 1.5 V			250	ps
Jitter abs	t_{jabs5}	V_T = 1.5 V		715	800	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output Impedance	R_{DSN1}	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25			mA
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.925	2	ns
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.66	2	ns
Duty Cycle	d_{t1}	V_T = 1.5 V	45	49.4	55	%
Skew Window	t_{sk1}	V_T = 1.5 V		74.5	250	ps
Jitter	t_{j1s1}	V_T = 1.5 V			150	ps
	t_{jabs1}	V_T = 1.5 V		150	500	ps

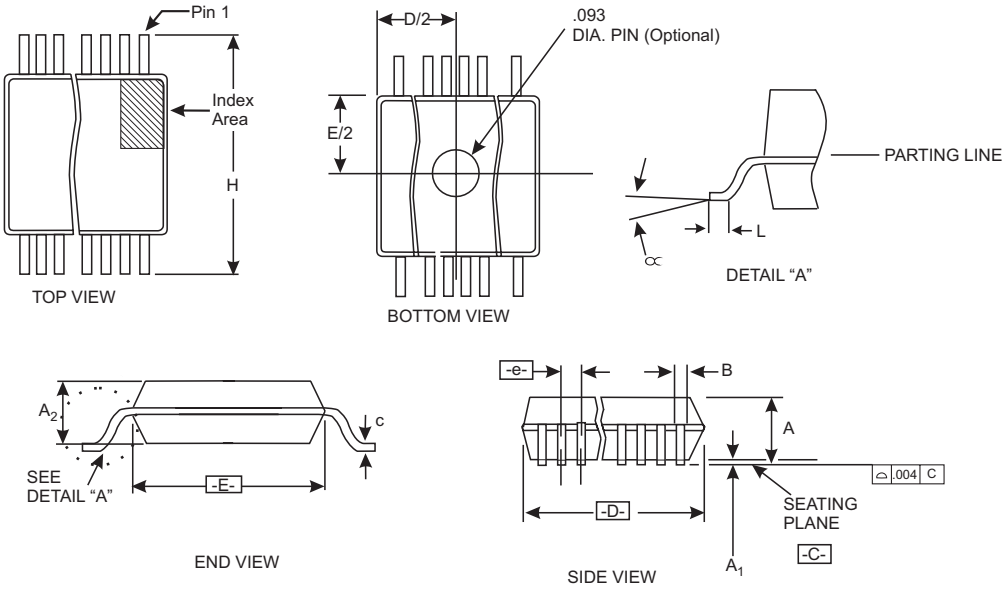
[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2A}	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output Impedance	R_{DSN2A}	$V_O = V_{DD}*(0.5)$	10		20	Ω
Output High Voltage	V_{OH2A}	I_{OH} = -28 mA	2.4			V
Output Low Voltage	V_{OL2A}	I_{OL} = 19 mA			0.4	V
Output High Current	I_{OH2A}	V_{OH} = 2.0 V			-42	mA
Output Low Current	I_{OL2A}	V_{OL} = 0.8 V	33			mA
Rise Time	t_{r2A}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.08	2	ns
Fall Time	t_{f2A}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.26	2	ns
Duty Cycle	d_{t2A}	V_T = 1.5 V	45	49.85	55	%
Skew Window	tsk2A	VT = 1.5 V		203	250	ps

[1]Guarenteed by design, not 100% tested in production.



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.102	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.087	.090	.094					
B	.008	-	.0135					
c	.005	-	.010					
D	See Variations							
E	.291	.295	.299					
e	0.025 BSC							
H	.395	-	.420					
h	.010	.013	.016					
L	.020	-	.040					
N	See Variations							
∝	0°	-	8°					

"For current dimensional specifications, see JEDEC 95."

Dimensions in inches

48 Pin 300 mil SSOP Package

Ordering Information

ICS9248yF-102-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device