



# Frequency Generator & Integrated Buffers for Mother Boards

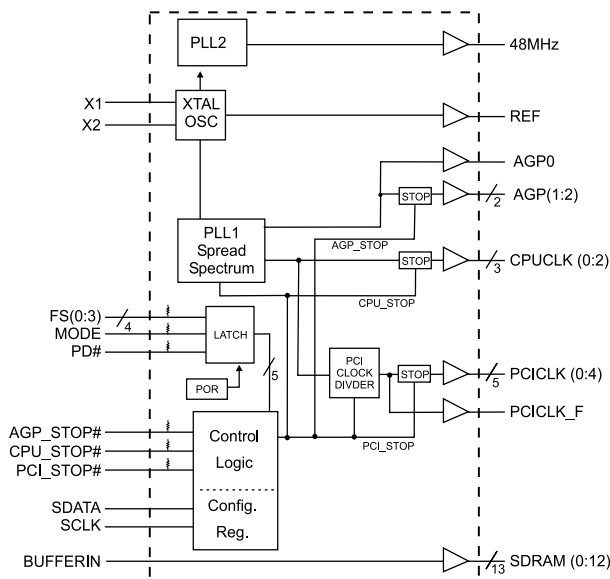
## General Description

The **ICS9148-75** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro™, AMD™ or Cyrix™. Sixteen different reference frequency multiplying factors are externally selectable with smooth frequency transitions.

Spread spectrum may be enabled through I<sup>2</sup>C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The **ICS9148-75** employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I<sup>2</sup>C interface allows changing functions, stop clock programming and frequency selection. The SDRAM12 output may be used as a feed back into an off chip PLL.

## Block Diagram



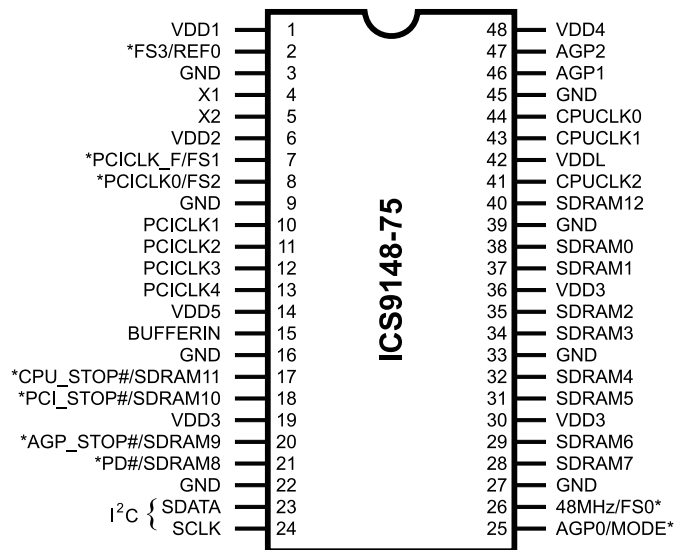
## Power Groups

- VDD1 = REF (0:1), X1, X2
- VDD2 = PCICLK\_F, PCICLK(0:5)
- VDD3 = SDRAM (0:11), supply for PLL core
- VDD4 = AGP (1:2)
- VDD5 = Fixed PLL, 48MHz, AGP0
- VDDL = CPUCLK (0:3)

## Features

- Generates the following system clocks:
  - 3 CPU(2.5V/3.3V) up to 100MHz.
  - 6 PCI(3.3V) @ 33.3MHz (including one free running PCICLK)
  - 3AGP(3.3V) @ 2x PCI
  - 13 SDRAMs(3.3V) up to 100MHz
  - 1 REF (3.3V) @ 14.318MHz
  - 1 - 48MHz (3.3V) fixed
- Skew characteristics:
  - CPU – CPU ≤ 250ps
  - CPU(early) – PCI: 1-4ns
  - AGP – PCI: 250ps
  - PCI – PCI < 500ps
- Supports Spread Spectrum modulation & I<sup>2</sup>C programming for Power Management, Frequency Select
- Efficient Power management scheme through power down PCI, AGP and CPU\_STOP clocks.
- Uses external 14.318MHz crystal
- 48 pin 300mil SSOP.

## Pin Configuration



## 48-Pin SSOP

\* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs

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I<sup>2</sup>C is a trademark of Philips Corporation



### Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDD1	PWR	Ref (0:2), XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 MHz reference clock.
	FS3	IN	Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.
3,9,16,22,27,33,39,45	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (33pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (33pF)
6	VDD2	PWR	Supply for PCICLK_F and PCICLK (0:5), nominal 3.3V
7	PCICLK_F	OUT	Free running PCI clock output. Synchronous with CPUCLKs with 1-4ns skew (CPU early) This is not affected by PCI_STOP#
	FS1 <sup>1,2</sup>	IN	Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.
8	PCICLK0	OUT	PCI clock outputs. Synchronous CPUCLKs with 1-4ns skew (CPU early)
	FS2 <sup>1,2</sup>	IN	Frequency select pin. Latched Input
10, 11, 12, 13	PCICLK(1:4)	OUT	PCI clock outputs. Synchronous CPUCLKs with 1-4ns skew (CPU early)
14	VDD5	PWR	Supply for fixed PLL, 48MHz, AGP0
15	BUFFERIN	IN	Input pin for SDRAM buffers.
17	CPU_STOP#	IN	Halts CPUCLK (0:3) clocks at logic 0 level, when input low (in Mobile Mode, MODE=0)
	SDRAM 11	OUT	SDRAM clock output
18	PCI_STOP# <sup>1</sup>	IN	Halts PCICLK(0:5) clocks at logic 0 level, when input low (In mobile mode, MODE=0)
	SDRAM 10	OUT	SDRAM clock output
28, 29, 31, 32, 34, 35,37,38	SDRAM (0:9)	OUT	SDRAM clock outputs.
20	AGP_STOP# <sup>1</sup>	IN	This asynchronous input halts AGP(1:2) clocks at logic "0" level when input low (in Mobile Mode, MODE=0) Does not affect AGP0
	SDRAM9	OUT	SDRAM clock output
21	PD# <sup>1</sup>	IN	This asynchronous Power Down input Stops the VCO, crystal & internal clocks when active, Low. (In Mobile Mode, MODE=0)
	SDRAM8	OUT	SDRAM clock output
19,30,36	VDD3	PWR	Supply for SDRAM (0:11), CPU Core, 48MHz clocks, nominal 3.3V.
23	SDATA	IN	Data input for I <sup>2</sup> C serial input.
24	SCLK	IN	Clock input of I <sup>2</sup> C input
25	AGP0	OUT	Advanced Graphic Port output, powered by VDD4. Not affected by AGP_STOP#
	MODE <sup>1,2</sup>	IN	Pin 17, 18, 20 & 21 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.
26	48MHz	OUT	48MHz output clock for USB timing.
	FS0 <sup>1,2</sup>	IN	Frequency select pin. Latched Input. Along with other FS pins determines the CPU, SDRAM, PCI & AGP frequencies.
41, 43, 44	CPUCLK(0:3)	OUT	CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low
40	SDRAM12	OUT	Feedback SDRAM clock output.
42	VDDL	PWR	Supply for CPU (0:3), either 2.5V or 3.3V nominal
46, 47	AGP (1:2)	OUT	Advanced Graphic Port output powered by VDD4.
48	VDD4	PWR	Supply for AGP (0:2)

#### Notes:

- 1: Internal Pull-up Resistor of 240K to 3.3V on indicated inputs
- 2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



### Mode Pin - Power Management Input Control

MODE, Pin 25 (Latched Input)	Pin 17	Pin 18	Pin 20	Pin 21
0	CPU_STOP# (INPUT)	PCI_STOP# (INPUT)	AGP_STOP# (INPUT)	PD# (INPUT)
1	SDRAM 11 (OUTPUT)	SDRAM 10 (OUTPUT)	SDRAM 9 (OUTPUT)	SDRAM 8 (OUTPUT)

### Power Management Functionality

AGP_STOP#	CPU_STOP#	PCI_STOP#	CPUCLK Outputs	PCICLK (0:5)	PCICLK_F, REF, 48MHz and SDRAM	Crystal OSC	VCO	AGP(1:2)
1	0	1	Stopped Low	Running	Running	Running	Running	Running
1	1	1	Running	Running	Running	Running	Running	Running
1	1	0	Running	Stopped Low	Running	Running	Running	Running
0	1	1	Running	Running	Running	Running	Running	Stopped Low

### CPU 3.3#\_2.5V Buffer selector for CPUCLK drivers.

CPU3.3#_2.5 Input level (Latched Data)	Buffer Selected for operation at:
1	2.5V VDD
0	3.3V VDD

# ICS9148-75

## Preliminary Product Preview



### Functionality

$V_{DD1,2,3,4} = 3.3V \pm 5\%$ ,  $T_A = 0$  to  $70^\circ C$   
Crystal (X1, X2) = 14.31818MHz

FS3	FS2	FS1	FS0	CPU,SDRAM (MHZ)	PCI (MHZ)	AGP (MHZ)	REF, IOAPIC (MHZ)
1	1	1	1	105	35	70	14.318
1	1	1	0	110	36.67	73.34	14.318
1	1	0	1	115	38.33	76.66	14.318
1	1	0	0	120	40	80	14.318
1	0	1	1	125	41.66	83.32	14.318
1	0	1	0	130	43.33	86.66	14.318
1	0	0	1	135	45	90	14.318
1	0	0	0	140	46.67	93.44	14.318
0	1	1	1	100	33.3	66.6	14.318
0	1	1	0	95.25	31.75	63.5	14.318
0	1	0	1	83.3	33.3	66.6	14.318
0	1	0	0	75	30	60	14.318
0	0	1	1	75	37.5	75	14.318
0	0	1	0	68.5	34.25	68.5	14.318
0	0	0	1	66.8	33.4	66.8	14.318
0	0	0	0	60	30	60	14.318



## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming. For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends a dummy command code
- ICS clock will **acknowledge**
- Controller (host) sends a dummy byte count
- ICS clock will **acknowledge**
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will **acknowledge** each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Byte 6	
	<b>ACK</b>
Stop Bit	

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the **byte count**
- Controller (host) acknowledges
- ICS clock sends first byte (**Byte 0**) through **byte 6**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
	<b>Byte 6</b>
ACK	
Stop Bit	

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



### Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description				PWD
Bit 7	0 - $\pm 0.25\%$ Spread Spectrum Modulation				0
	1 - $\pm 0.6\%$ Spread Spectrum Modulation				
Bit (2, 6:4)	Bit (2, 6:4)	CPU CLKs	PCI CLKs	AGP CLKs	Note1
	1111	105	35	70	
	1110	110	36.67	73.34	
	1101	115	38.33	76.66	
	1100	120	40	80	
	1011	125	41.66	83.32	
	1010	130	43.33	86.66	
	1001	135	45	90	
	1000	140	46.67	93.44	
	0111	100	33.3	66.6	
	0110	95.25	31.75	63.5	
	0101	83.3	33.3	66.6	
	0100	75	30	60	
	0011	75	37.5	75	
	0010	68.5	34.25	68.5	
	0001	66.8	33.4	66.8	
0000	60	30	60		
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 6:4 (above)				0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled (center spread)				0
Bit 0	0 - Running 1 - Tristate all outputs				0

**Note 1:** Default at power-up will be for latched logic inputs to define frequency;  
Bits 2, 6:4 are default to 000

**Note:** PWD = Power-Up Default



### Byte 1: CPU, Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	40	1	CPUCLK3 (Act/Inact)
Bit 2	41	1	CPUCLK2 (Act/Inact)
Bit 1	43	1	CPUCLK1 (Act/Inact)
Bit 0	44	1	CPUCLK0 (Act/Inact)

#### Notes:

- Inactive means outputs are held LOW and are disabled from switching.

### Byte 3: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	28	1	SDRAM7 (Act/Inact)
Bit 6	29	1	SDRAM6 (Act/Inact)
Bit 5	31	1	SDRAM5 (Act/Inact)
Bit 4	32	1	SDRAM4 (Act/Inact)
Bit 3	34	1	SDRAM3 (Act/Inact)
Bit 2	35	1	SDRAM2 (Act/Inact)
Bit 1	37	1	SDRAM1 (Act/Inact)
Bit 0	38	1	SDRAM0 (Act/Inact)

#### Notes:

- Inactive means outputs are held LOW and are disabled from switching.

### Byte 5: Peripheral Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	8	-	FS2#
Bit 5	7	-	FS1#
Bit 4	47	1	AGP2 (Act/Inact)
Bit 3	-	1	(Reserved)
Bit 2	2	-	FS3#
Bit 1	46	1	AGP1 (Act/Inact)
Bit 0	2	1	REF0 (Act/Inact)

#### Notes:

- Inactive means outputs are held LOW and are disabled from switching.

### Byte 2: PCI Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	7	1	PCICLK_F (Act/Inact)
Bit 5	15	1	PCICLK5 (Act/Inact)
Bit 4	13	1	PCICLK4 (Act/Inact)
Bit 3	12	1	PCICLK3 (Act/Inact)
Bit 2	11	1	PCICLK2 (Act/Inact)
Bit 1	10	1	PCICLK1 (Act/Inact)
Bit 0	8	1	PCICLK0 (Act/Inact)

#### Notes:

- Inactive means outputs are held LOW and are disabled from switching.

### Byte 4: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	Pin #	PWD	Description
Bit 7	25	1	AGP0 (Active/Inactive)
Bit 6	-	1	(Reserved)
Bit 5	26	-	FS0#
Bit 4	-	1	(Reserved)
Bit 3	17	1	SDRAM11 (Act/Inact) (Desktop Mode Only)
Bit 2	18	1	SDRAM10 (Act/Inact) (Desktop Mode Only)
Bit 1	20	1	SDRAM9 (Act/Inact)
Bit 0	21	1	SDRAM8 (Act/Inact)

#### Notes:

- Inactive means outputs are held LOW and are disabled from switching.

### Byte 6: Optional Register for Possible Future Requirements

Bit	Pin #	PWD	Description
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	-	1	(Reserved)
Bit 0	-	1	(Reserved)

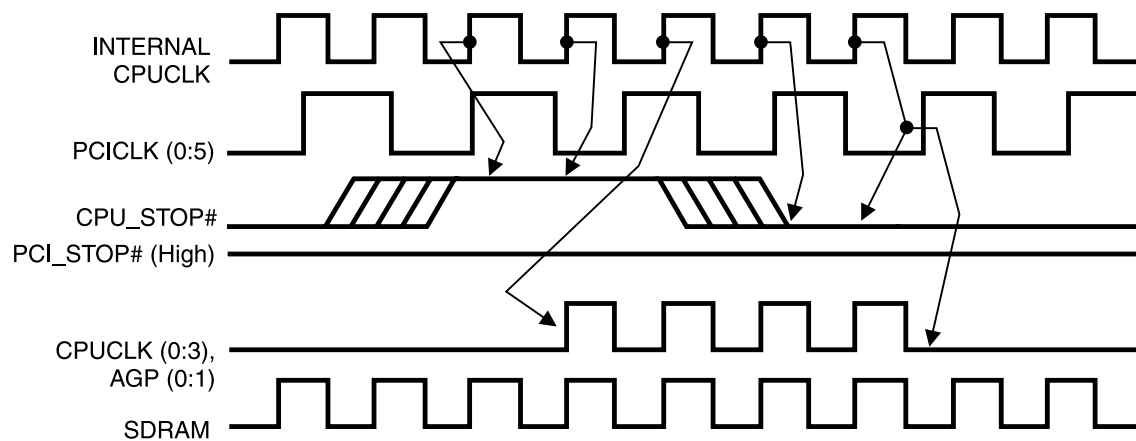
#### Notes:

- Byte 6 is reserved by Integrated Circuit Systems for future applications.



### CPU\_STOP# Timing Diagram

CPU\_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU\_STOP# is synchronized by the ICS9148-75. The minimum that the CPU clock is enabled (CPU\_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.



#### Notes:

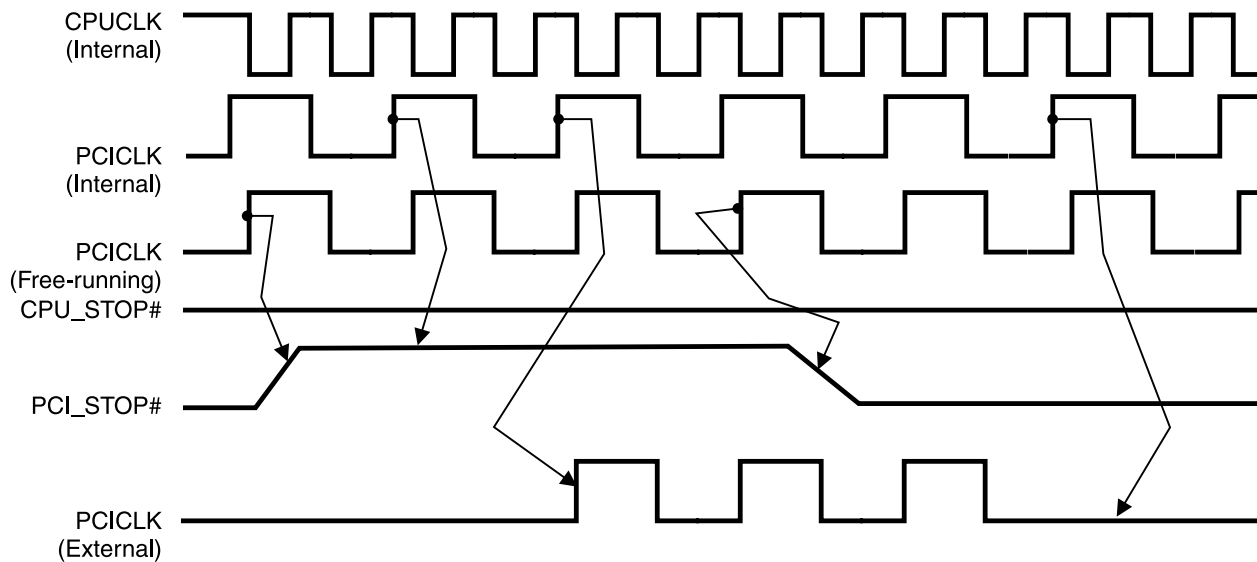
1. All timing is referenced to the internal CPU clock.
2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS9148-75.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).





### PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the ICS9148-75. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI\_STOP# is synchronized by the ICS9148-75 internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI\_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



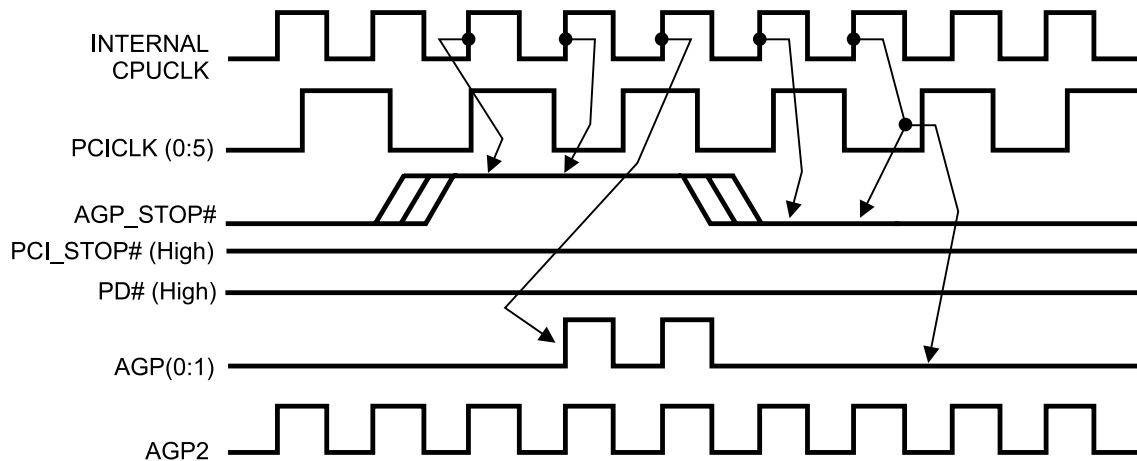
#### Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. CPU\_STOP# is shown in a high (true) state.



### AGP\_STOP# Timing Diagram

AGP\_STOP# is an asynchronous input to the clock synthesizer. It is used to turn off the AGP (0:1) clocks. for low power operation. AGP\_STOP# is synchronized by the **ICS9148-75**. The AGP2 clock is free-running and is not affected by AGP\_STOP#. All other clocks will continue to run while the AGPCLKs are disabled. The AGPCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. AGPCLK on latency is less than AGPCLK and AGPCLK off latency is less than 4 AGPCLKs. This function is available only with MODE pin latched low.



#### Notes:

1. All timing is referenced to the internal CPUCLK.
2. AGP\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9148-75**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI\_STOP# are shown in a high (true) state.
5. Only applies if MODE pin latched 0 at power up.



### Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9148-75 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

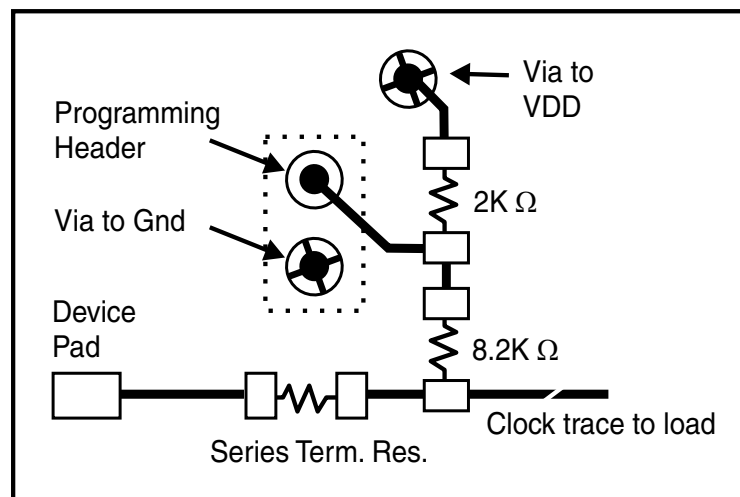


Fig. 1



### Absolute Maximum Ratings

Supply Voltage	7.0 V
Logic Inputs	GND-0.5 V to V <sub>DD</sub> +0.5 V
Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = V<sub>DDL</sub> = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V <sub>IH</sub>		2		V <sub>DD</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>		V <sub>SS</sub> -0.3		0.8	V
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>		0.1	5	mA
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5	2.0		mA
Input Low Current	I <sub>IL2</sub>	V <sub>IN</sub> = 0 V; Inputs with pull-up resistors	-200	-100		mA
Operating Supply Current	I <sub>DD3.3OP</sub>	C <sub>L</sub> = 0 pF; 66.8 MHz		100	160	mA
Input frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V;		14.318		MHz
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	Logic Inputs			5	pF
	C <sub>INX</sub>	X1 & X2 pins	27	36	45	pF
Transition Time <sup>1</sup>	T <sub>trans</sub>	To 1st crossing of target Freq.			2	ms
Settling Time <sup>1</sup>	T <sub>s</sub>	From 1st crossing to 1% target Freq.				ms
Clk Stabilization <sup>1</sup>	T <sub>STAB</sub>	From V <sub>DD</sub> = 3.3 V to 1% target Freq.			2	ms
Skew <sup>1</sup>	T <sub>CPU-SDRAM1</sub>	V <sub>T</sub> = 1.5 V; SDRAM Leads	-500	200	500	ps
	T <sub>CPU-PCI1</sub>	V <sub>T</sub> = 1.5 V; CPU Leads	2	5	6	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current	I <sub>DD2.5OP</sub>	C <sub>L</sub> = 0 pF; 66.8 MHz		10	20	mA
Skew <sup>1</sup>	T <sub>CPU-SDRAM2</sub>	V <sub>T</sub> = 1.5 V; V <sub>TL</sub> = 1.25 V; SDRAM Leads	-500	200	500	ps
	T <sub>CPU-PCI2</sub>	V <sub>T</sub> = 1.5 V; V <sub>TL</sub> = 1.25 V; CPU Leads	2	5	6	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**Electrical Characteristics - CPU**

T<sub>A</sub> = 0 - 70C; V<sub>DD</sub> = V<sub>DDL</sub> = 3.3 V +/-10%; C<sub>L</sub> = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH2A</sub>	I <sub>OH</sub> = -28 mA	2.5	2.6		V
Output Low Voltage	V <sub>OL2A</sub>	I <sub>OL</sub> = 27 mA		0.35	0.4	V
Output High Current	I <sub>OH2A</sub>	V <sub>OH</sub> = 2.0 V		-29	-23	mA
Output Low Current	I <sub>OL2A</sub>	V <sub>OL</sub> = 0.8 V	33	37		mA
Rise Time	t <sub>r2A</sub> <sup>1</sup>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V		1.75	2	ns
Fall Time	t <sub>f2A</sub> <sup>1</sup>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V		1.1	2	ns
Duty Cycle	d <sub>l2A</sub> <sup>1</sup>	V <sub>T</sub> = 1.5 V	45	50	55	%
Skew	t <sub>sk2A</sub> <sup>1</sup>	V <sub>T</sub> = 1.5 V		50	250	ps
Jitter, One Sigma	t <sub>j1s2A</sub> <sup>1</sup>	V <sub>T</sub> = 1.5 V		65	150	ps
Jitter, Absolute	t <sub>jabs2A</sub> <sup>1</sup>	V <sub>T</sub> = 1.5 V	-250	165	250	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - PCI**

T<sub>A</sub> = 0 - 70C; V<sub>DD</sub> = V<sub>DDL</sub> = 3.3 V +/-10%; C<sub>L</sub> = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -28 mA	2.4	3		V
Output Low Voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 23 mA		0.2	0.4	V
Output High Current	I <sub>OH1</sub>	V <sub>OH</sub> = 2.0 V		-60	-40	mA
Output Low Current	I <sub>OL1</sub>	V <sub>OL</sub> = 0.8 V	41	50		mA
Rise Time	t <sub>r1</sub> <sup>1</sup>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V		1.8	2	ns
Fall Time	t <sub>f1</sub> <sup>1</sup>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V		1.6	2	ns
Duty Cycle	d <sub>t1</sub> <sup>1</sup>	V <sub>T</sub> = 1.5 V	45	50	55	%
Skew	t <sub>sk1</sub> <sup>1</sup>	V <sub>T</sub> = 1.5 V		130	250	ps
Jitter, One Sigma <sup>1</sup>	t <sub>j1s1a</sub>	V <sub>T</sub> = 1.5 V, synchronous		40	150	ps
	t <sub>j1s1b</sub>	V <sub>T</sub> = 1.5 V, asynchronous		200	250	ps
Jitter, Absolute <sup>1</sup>	t <sub>jabs1a</sub>	V <sub>T</sub> = 1.5 V, synchronous	-250	135	250	ps
	t <sub>jabs1b</sub>	V <sub>T</sub> = 1.5 V, asynchronous	-650	500	650	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.



### Electrical Characteristics - SDRAM

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 5\%$ ;  $C_L = 30 \text{ pF}$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH1}$	$I_{OH} = -28 \text{ mA}$	2.4	3		V
Output Low Voltage	$V_{OL1}$	$I_{OL} = 23 \text{ mA}$		0.2	0.4	V
Output High Current	$I_{OH1}$	$V_{OH} = 2.0 \text{ V}$		-60	-40	mA
Output Low Current	$I_{OL1}$	$V_{OL} = 0.8 \text{ V}$	41	50		mA
Rise Time <sup>1</sup>	$T_{r1}$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$		1.75	2	ns
Fall Time <sup>1</sup>	$T_{f1}$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$		1.5	2	ns
Duty Cycle <sup>1</sup>	$D_{t1}$	$V_T = 1.5 \text{ V}$	45	50	55	%
Skew <sup>1</sup>	$T_{sk1}$	$V_T = 1.5 \text{ V}$		200	500	ps
Jitter, One Sigma <sup>1</sup>	$T_{j1s1}$	$V_T = 1.5 \text{ V}$		50	150	ps
Jitter, Absolute <sup>1</sup>	$T_{jabs1}$	$V_T = 1.5 \text{ V}$ (with synchronous PCI)	-250		+250	ps
Jitter, Absolute <sup>1</sup>	$T_{jabs1}$	$V_T = 1.5 \text{ V}$ (with asynchronous PCI)	-400		400	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - AGP

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 10\%$ ;  $C_L = 30 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH1}$	$I_{OH} = -28 \text{ mA}$	2.4	3		V
Output Low Voltage	$V_{OL1}$	$I_{OL} = 23 \text{ mA}$		0.2	0.4	V
Output High Current	$I_{OH1}$	$V_{OH} = 2.0 \text{ V}$		-60	-40	mA
Output Low Current	$I_{OL1}$	$V_{OL} = 0.8 \text{ V}$	41	50		mA
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$		1.1	2	ns
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$		1	2	ns
Duty Cycle	$d_{t1}^1$	$V_T = 1.4 \text{ V}$	45	50	55	%
Skew	$t_{sk1}^1$	$V_T = 1.5 \text{ V}$		130	250	ps
Jitter, One Sigma <sup>1</sup>	$t_{j1s1}$	$V_T = 1.5 \text{ V}$		2	3	%
Jitter, Absolute <sup>1</sup>	$t_{jabs1a}$	$V_T = 1.5 \text{ V}$ , synchronous	-5	2.5	5	%
	$t_{jabs1b}$	$V_T = 1.5 \text{ V}$ , asynchronous	-6	4.5	6	%

<sup>1</sup>Guaranteed by design, not 100% tested in production.

**Electrical Characteristics - 24MHz, 48MHz, REF** $T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 10\%$ ;  $C_L = 10 - 20 \text{ pF}$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH5}$	$I_{OH} = -16 \text{ mA}$	2.4	2.6		V
Output Low Voltage	$V_{OL5}$	$I_{OL} = 9 \text{ mA}$		0.3	0.4	V
Output High Current	$I_{OH5}$	$V_{OH} = 2.0 \text{ V}$		-32	-22	mA
Output Low Current	$I_{OL5}$	$V_{OL} = 0.8 \text{ V}$	16	25		mA
Rise Time	$t_{r5}^1$	$V_{OL} = 0.4 \text{ V}, V_{OH} = 2.4 \text{ V}$		2	4	ns
Fall Time	$t_{f5}^1$	$V_{OH} = 2.4 \text{ V}, V_{OL} = 0.4 \text{ V}$		1.9	4	ns
Duty Cycle	$d_{t5}^1$	$V_T = 1.5 \text{ V}$	45	50	55	%
Jitter, One Sigma	$t_{j1s5}^1$	$V_T = 1.5 \text{ V}$		1	3	%
Jitter, Absolute	$t_{jabs5}^1$	$V_T = 1.5 \text{ V}$	-5	-	5	%

<sup>1</sup>Guaranteed by design, not 100% tested in production.

# ICS9148-75

## Preliminary Product Preview

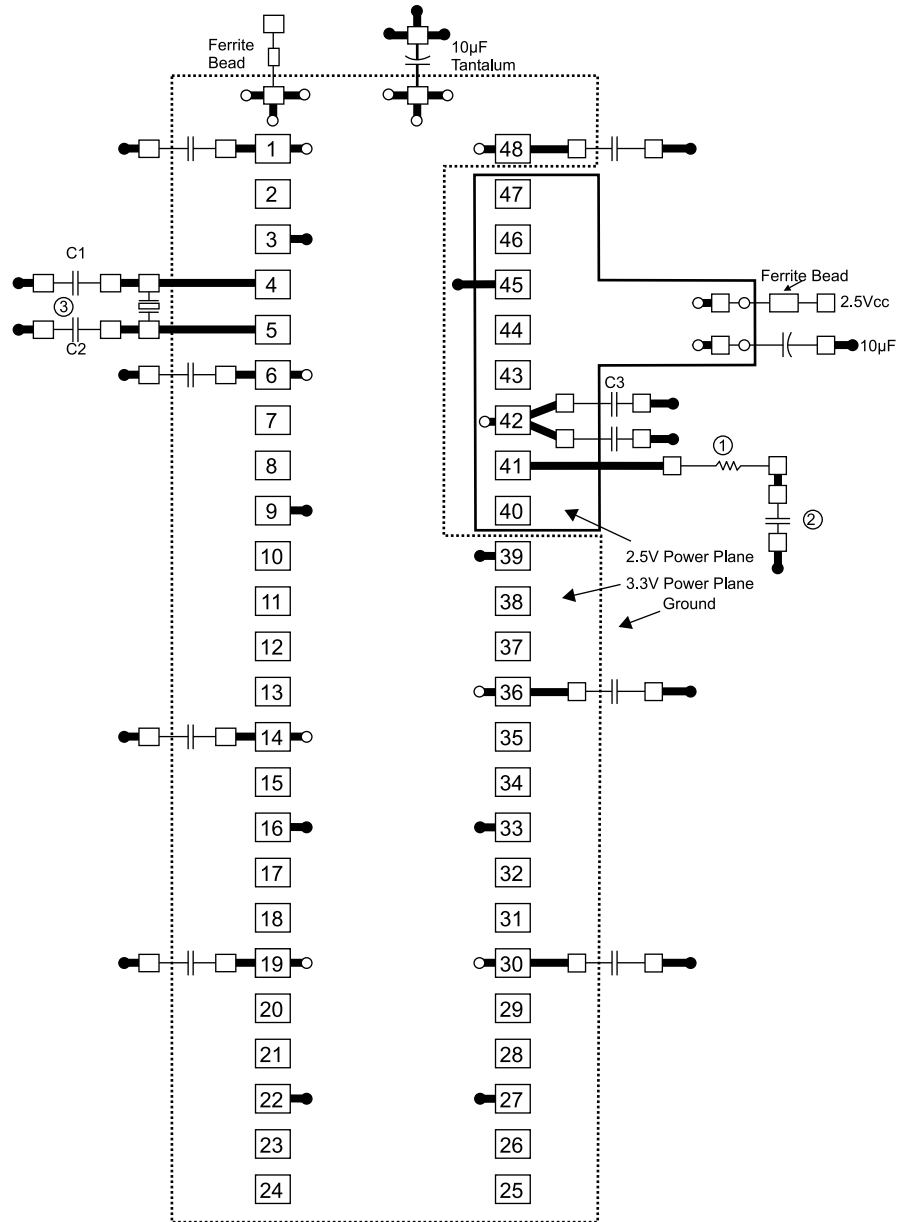


### General Layout Precautions:

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and vias as wide as possible to lower inductance.

### Notes:

- 1 All clock outputs should have series terminating resistor. Not shown in all places to improve readability of diagram
- 2 Optional EMI capacitor should be used on all CPU, SDRAM, and PCI outputs.
- 3 Optional crystal load capacitors are recommended.



- = Ground Plane Connection
- = Power Plane Connection
- = Solder Pads

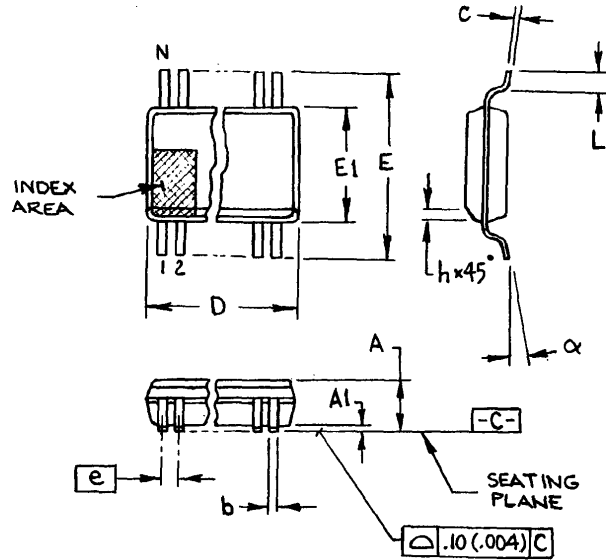
### Capacitor Values:

C1, C2 : Crystal load values determined by user

C3 : 100pF ceramic

All unmarked capacitors are 0.01 µF ceramic





300 mil SSOP

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.40	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.00	10.70	.395	.420
E1	7.40	7.60	.291	.299
e	0.065 BASIC		0.025 BASIC	
h	0.40	0.65	.015	.025
L	0.50	1.00	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.40	9.65	.370	.380
34	11.30	11.55	.445	.455
48	15.75	16.00	.620	.630
56	18.30	18.55	.720	.730
64	20.80	21.05	.820	.830

Ordering Information

ICS9148yF-75-T

Example:

ICS XXXX y F - PPP - T

