

### GENERAL DESCRIPTION

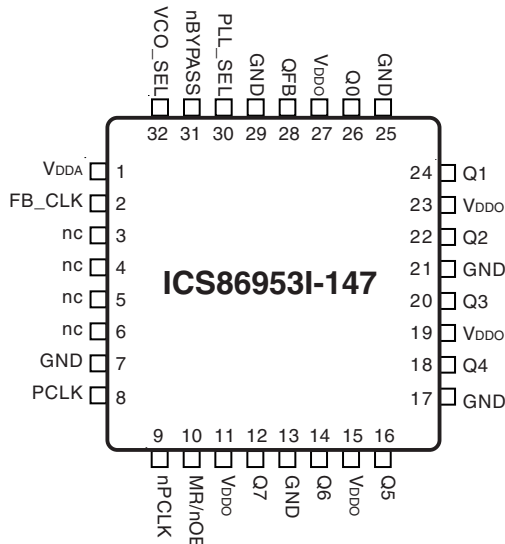


The ICS86953I-147 is a low voltage, low skew 1-to-9 Differential-to-LVCMOS/LVTTTL Clock Generator. The PCLK, nPCLK pair can accept most standard differential input levels. With output frequencies up to 175MHz, the ICS86953I-147 is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS86953I-147 contains frequency configurable outputs and an external feedback input for regenerating clocks with “zero delay”.

### FEATURES

- Nine single ended LVCMOS/LVTTTL outputs; (8) clocks, (1) feedback
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Maximum output frequency: PLL Mode, 175MHz
- VCO range: 250MHz to 700MHz
- Output skew: 75ps (maximum)
- Cycle-to-cycle jitter: 50ps (maximum)
- Static phase offset: 90ps ± 110ps
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

### PIN ASSIGNMENT



**32-Lead LQFP**

7mm x 7mm x 1.4mm package body

**Y package**

Top View

### BLOCK DIAGRAM

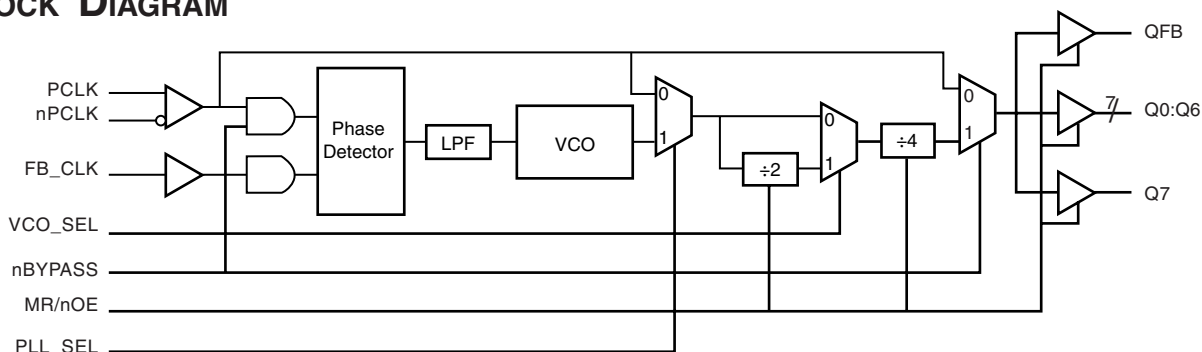


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V <sub>DDA</sub>	Power		Analog supply pin.
2	FB_CLK	Input	Pullup	Feedback clock input. LVCMOS / LVTTTL interface levels.
3, 4, 5, 6	nc	Unused		No connect.
7, 13, 17, 21, 25, 29	GND	Power		Power supply ground.
8	PCLK	Input	Pullup	Non-inverting LVPECL differential clock input.
9	nPCLK	Input	Pullup/ Pulldown	Inverting LVPECL differential clock input. Internally biased to V <sub>DDO</sub> /2.
10	MR/nOE	Input	Pulldown	Active HIGH Master Reset. Active LOW output enable. When logic High, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
11, 15, 19, 23, 27	V <sub>DDO</sub>	Power		Output supply pins.
12, 14, 16, 18, 20, 22, 24, 26	Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. LVCMOS / LVTTTL interface levels. 14Ω typical output impedance.
28	QFB	Output		Feedback clock output. LVCMOS / LVTTTL interface levels. 14Ω typical output impedance.
30	PLL_SEL	Input	Pullup	Selects VCO when HIGH. When LOW, selects PCLK, nPCLK. LVCMOS / LVTTTL interface levels.
31	nBYPASS	Input	Pullup	Selects PLL when HIGH. When LOW, in Bypass mode.
32	VCO_SEL	Input	Pullup	Selects VCO ÷2 when HIGH. Selects VCO ÷1 when LOW. LVCMOS / LVTTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DDA</sub> , V <sub>DDO</sub> = 3.465V	5	7	12	pF
R <sub>OUT</sub>	Output Impedance			14		Ω

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Input	Outputs
MR/nOE	QFB, Q0:Q7
1	HiZ
0	Enabled

TABLE 3B. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE

Inputs			Operation	Outputs
Bypass	PLL_SEL	VCO_SEL		QFB, Q0:Q7
0	X	X	Test Mode: PLL and divider bypass	CLK
1	0	0	Test Mode: PLL bypass	CLK/4
1	0	1	Test Mode: PLL bypass	CLK/8
1	1	0	PLL Mode	VCO/4
1	1	1	PLL Mode	VCO/8

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_i$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_o$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DDA}$	Analog Supply Current				20	mA
$I_{DDO}$	Output Supply Current				75	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	VCO_SEL, nBYPASS, PLL_SEL, MR/nOE	2		$V_{DD} + 0.3$	V
		FB_CLK	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	VCO_SEL, nBYPASS, PLL_SEL, MR/nOE	-0.3		0.8	V
		FB_CLK	-0.3		1.3	V
$I_{IN}$	Input Current				$\pm 120$	$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OH} = -20\text{mA}$	$V_{DD} - 0.6$			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 20\text{mA}$			0.6	V

**TABLE 4C. LVPECL DC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IN}$	Input Current				$\pm 120$	$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

**TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{REF}$	Input Reference Frequency				175	MHz

**TABLE 6. AC CHARACTERISTICS,  $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{MAX}$	Output Frequency	PLL Mode	VCO_SEL = 1	31.25		87.5	MHz
		PLL Mode	VCO_SEL = 0	62.50		175	MHz
		Bypass Mode				200	MHz
$t_{PD}$	Propagation Delay; NOTE 1	PCLK, nPCLK	2.5		4	ns	
$t_{sk(o)}$	Output Skew; NOTE 2, 4	Measured on rising edge at $V_{DD}/2$			75	ps	
$f_{jitter(cc)}$	Cycle-to-Cycle Jitter; NOTE 5				50	ps	
$t(\emptyset)$	Static Phase Offset; NOTE 3, 5		-20	90	200	ps	
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		700	ps	
odc	Output Duty Cycle		47	50	53	%	
$t_{LOCK}$	PLL Lock Time				10	ms	
$t_{EN}$	Output Enable Time; NOTE 4				6	ns	
$t_{DIS}$	Output Disable Time; NOTE 4				7	ns	

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Termination of  $50\Omega$  to  $V_{DDO}/2$ .

NOTE 1: Measured from the differential input crossing point to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

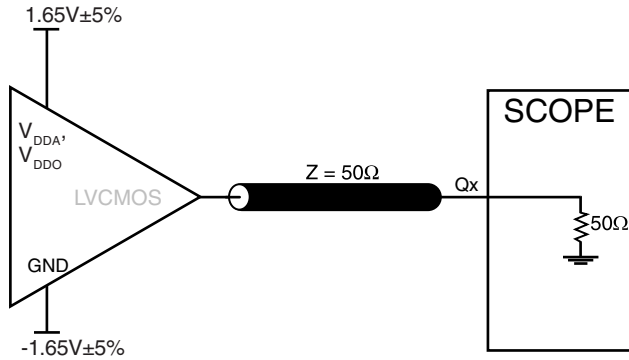
Measured at  $V_{DDO}/2$ .

NOTE 3: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

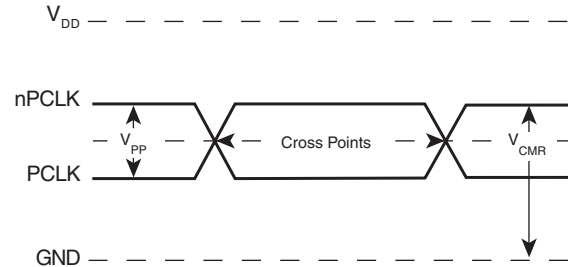
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

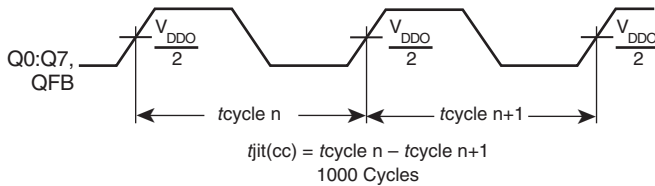
# PARAMETER MEASUREMENT INFORMATION



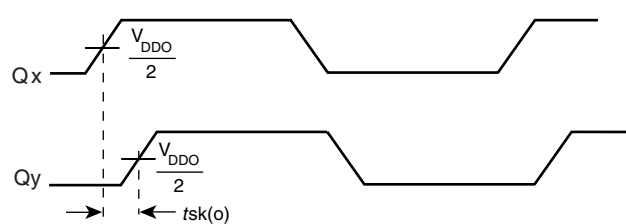
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



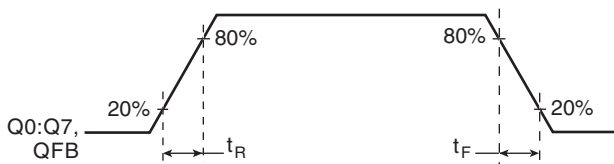
**DIFFERENTIAL INPUT LEVEL**



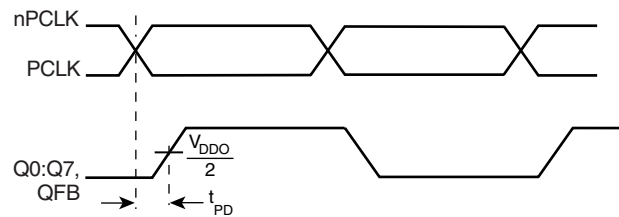
**CYCLE-TO-CYCLE JITTER**



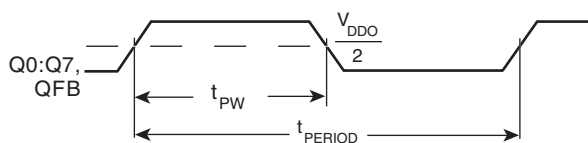
**OUTPUT SKEW**



**OUTPUT RISE/FALL TIME**

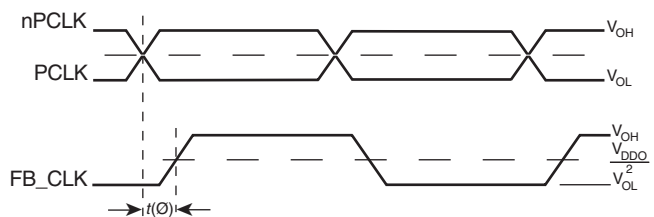


**PROPAGATION DELAY**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



$$t_{jit}(\emptyset) = |t(\emptyset) - t(\emptyset)_{mean}| = \text{Phase Jitter}$$

(where  $t(\emptyset)$  is any random sample, and  $t(\emptyset)_{mean}$  is the average of the sampled cycles measured on controlled edges)

**PHASE JITTER & STATIC PHASE OFFSET**

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS86953I-147 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.

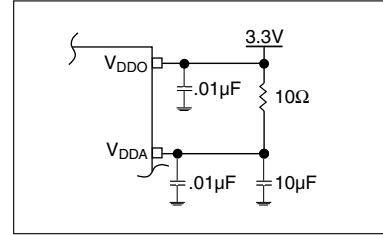


FIGURE 1. POWER SUPPLY FILTERING

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors  $R1$  and  $R2$ . The bypass capacitor ( $C1$ ) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ ,  $R1$  and  $R2$  value should be adjusted to set  $V_{REF}$  at  $1.25\text{V}$ . The values below are for when both the single-ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R3$  and  $R4$  in parallel should equal the transmission line

impedance. For most 50 applications,  $R3$  and  $R4$  can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than  $-0.3\text{V}$  and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3\text{V}$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

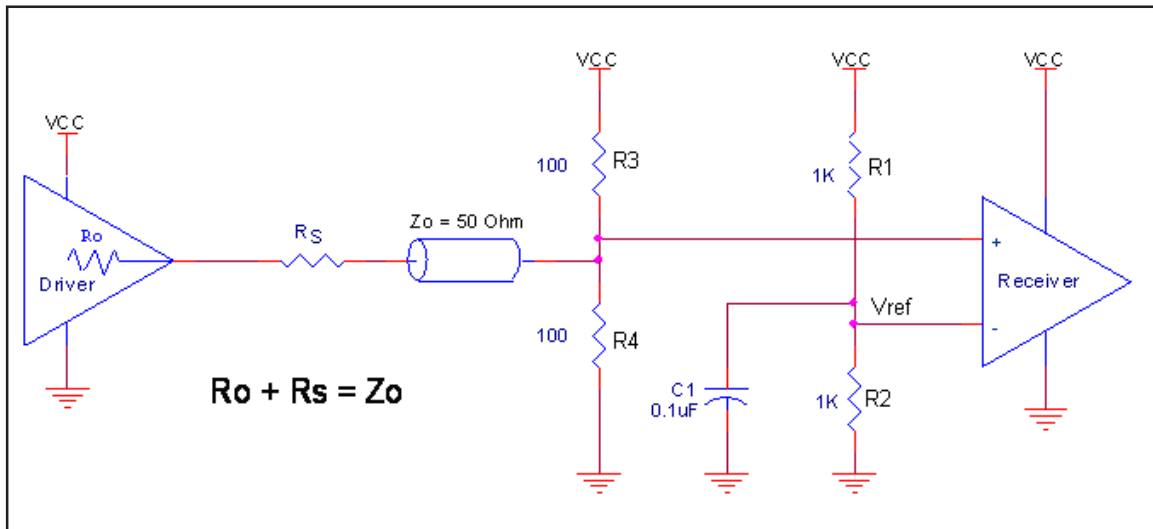
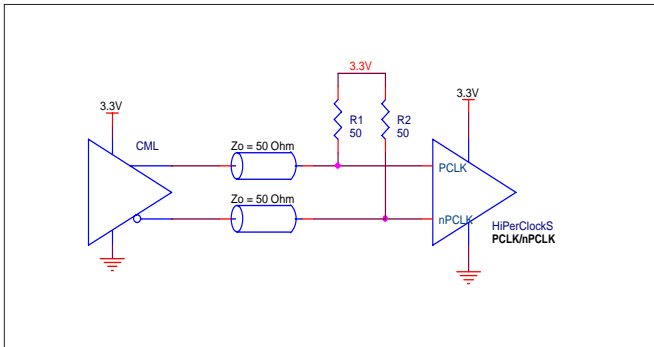


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

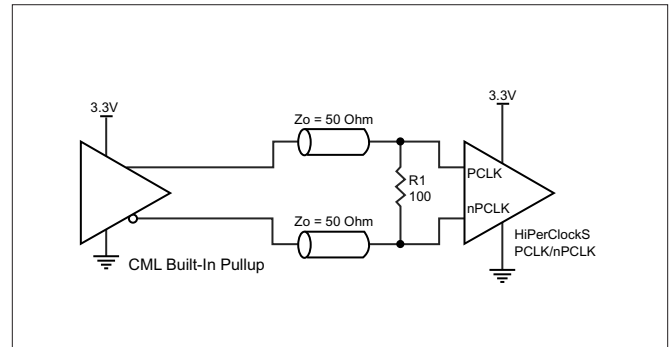
### LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both differential inputs must meet the  $V_{pp}$  and  $V_{CMR}$  input requirements. Figures 3A to 3E show interface examples for the PCLK/nPCLK input driven by the most common

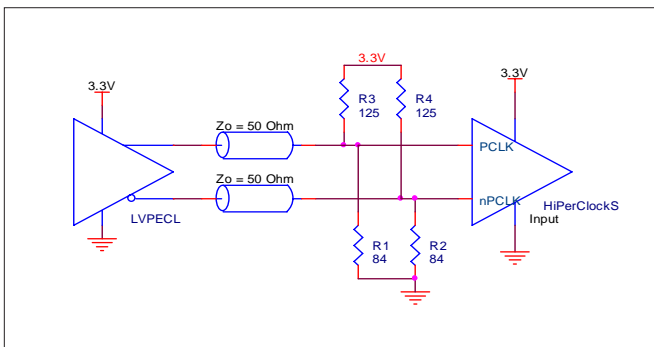
driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



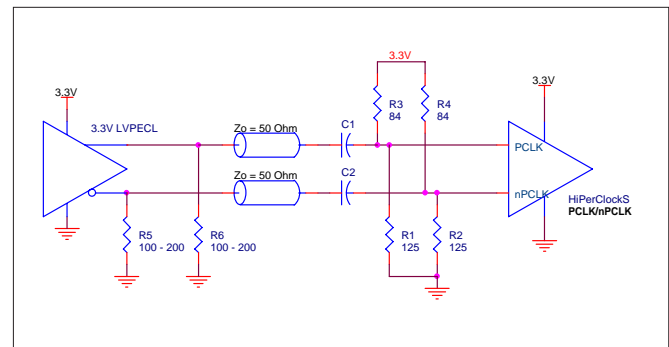
**FIGURE 3A. PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER**



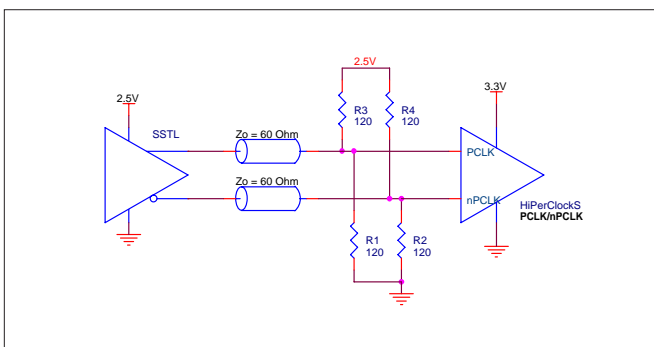
**FIGURE 3B. PCLK/nPCLK INPUT DRIVEN BY A BUILT-IN PULLUP CML DRIVER**



**FIGURE 3C. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 3D. PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**



**FIGURE 3E. PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER**

### LAYOUT GUIDELINE

The schematic of the ICS86953I-147 layout example is shown in *Figure 4A*. The ICS86953I-147 recommended PCB board layout for this example is shown in *Figure 4B*. This layout example is used as a general guideline. The layout in the actual system will depend

on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

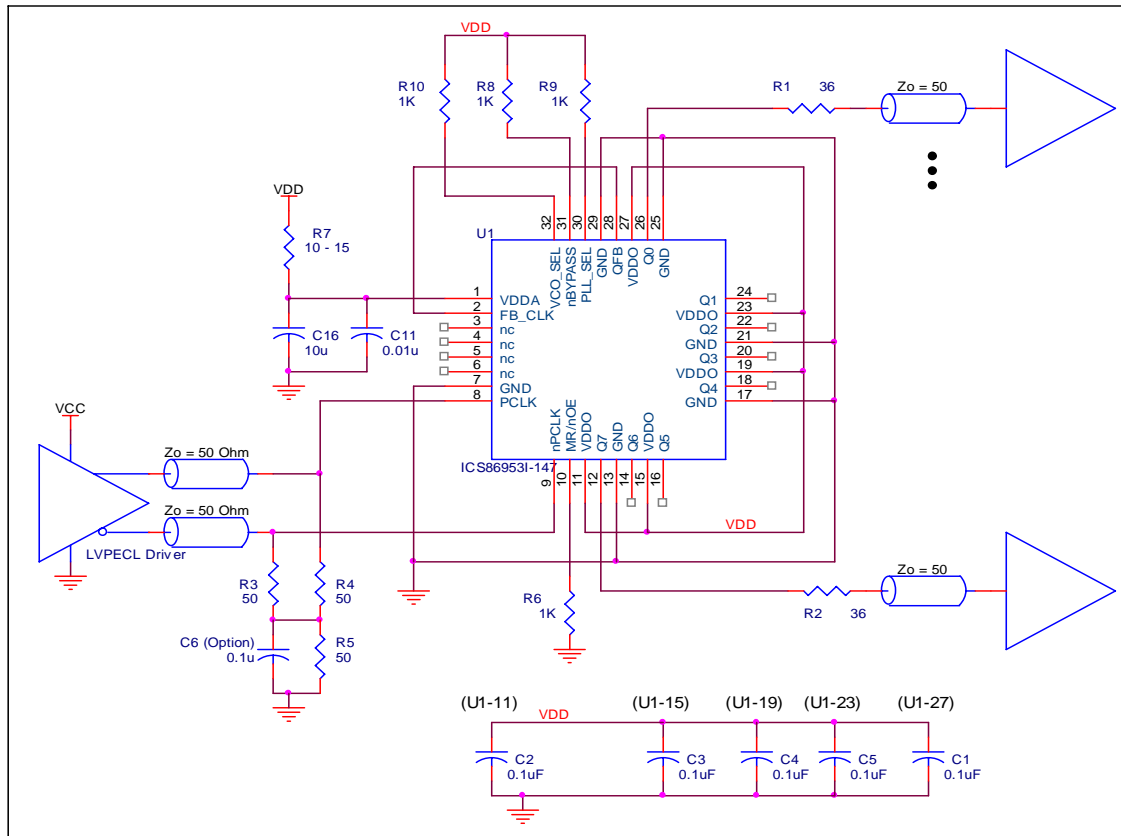


FIGURE 4A. ICS86953I-147 LVCMOS ZERO DELAY BUFFER SCHEMATIC EXAMPLE



The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

### POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the  $V_{DDA}$  pin as possible.

### CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay

might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The series termination resistors should be located as close to the driver pins as possible.

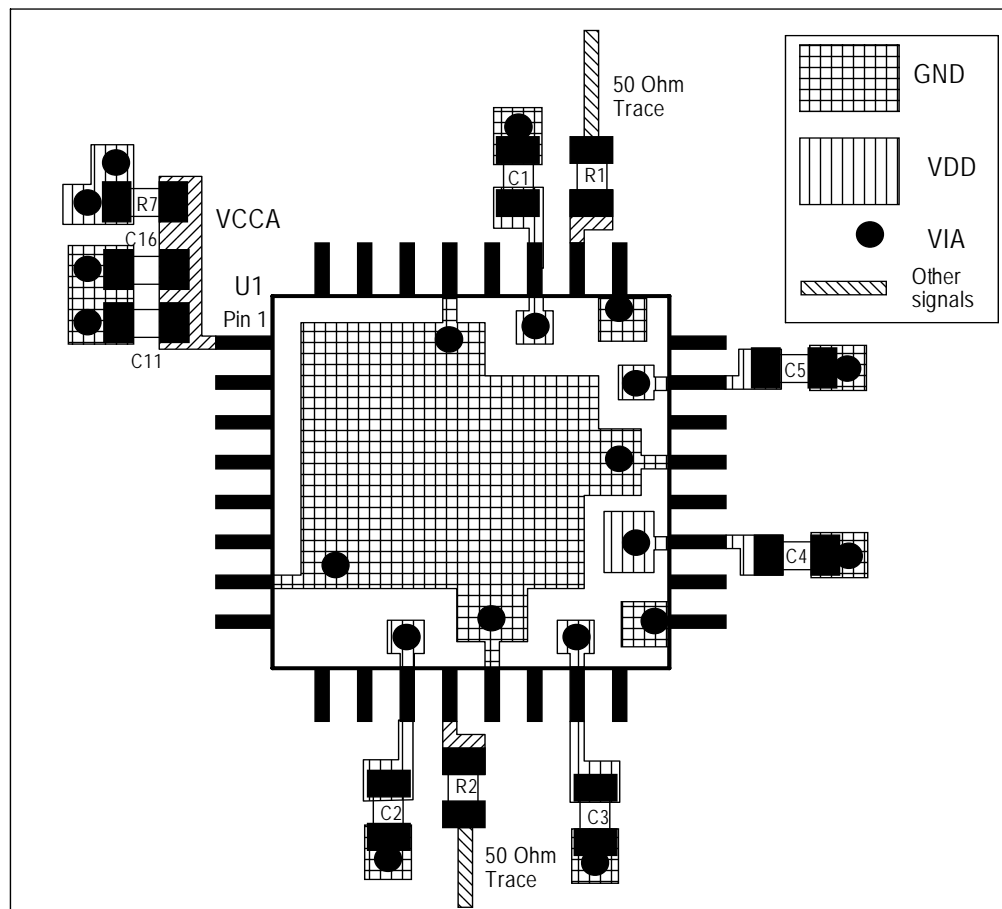


FIGURE 4B. PCB BOARD LAYOUT FOR ICS86953I-147

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 32 LEAD LQFP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS86953I-147 is: 1758

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

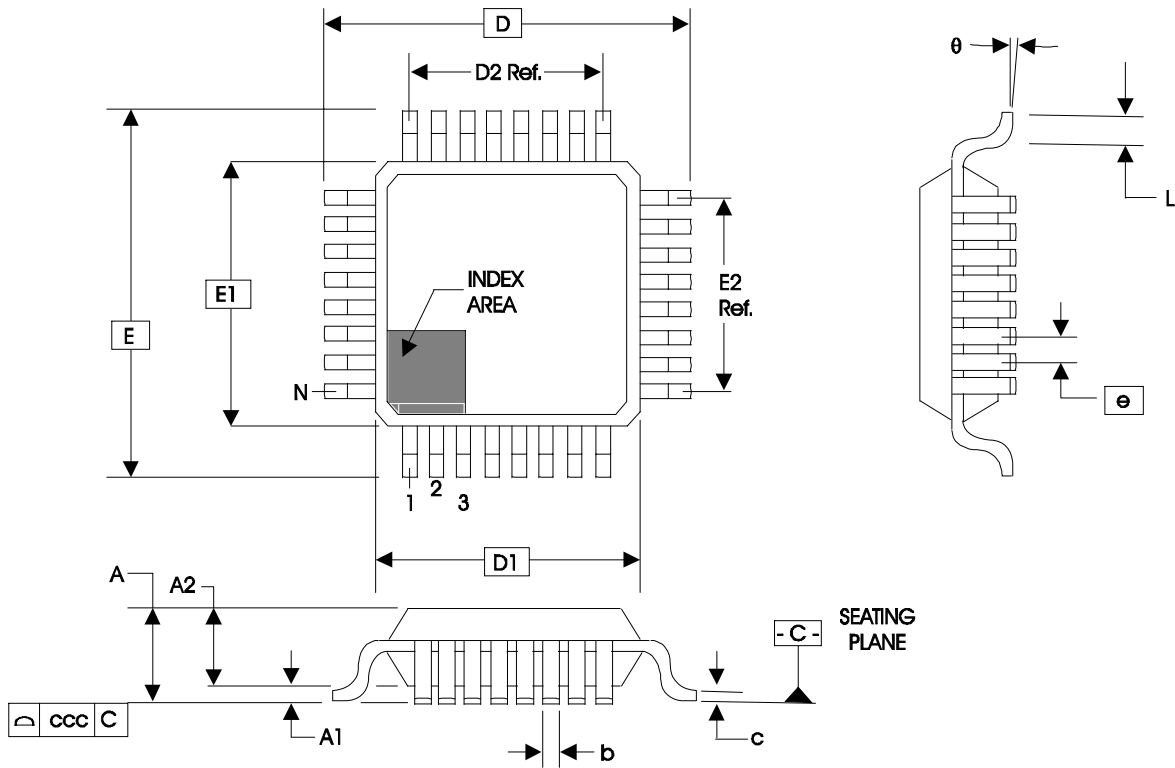


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
theta	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

**TABLE 9. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Packaging</b>	<b>Temperature</b>
86953BYI-147	ICS86953BI147	32 Lead LQFP	Tray	-40°C to 85°C
86953BYI-147T	ICS86953BI147	32 Lead LQFP	1000 Tae & Reel	-40°C to 85°C
86953BYI-147LF	ICS6953BI147L	Lead-Free, 32 Lead LQFP	Tray	-40°C to 85°C
86953BYI-147LFT	ICS6953BI147L	Lead-Free, 32 Lead LQFP	1000 Tae & Reel	-40°C to 85°C

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T1	2	Added Pullup/Pulldown to Pin 9.	10/28/03
	T2	2	Pin Characteristics table - changed $C_{IN}$ limit from 4pF max. to 4pF typical. Added 5pF min. and 7pF typical to $C_{PD}$ .	
		7	Updated Figure 3C and 3D.	
		8 & 9	Added Layout Guideline and PCB Board layout.	
B	T2	2	Pin Characteristics Table - added $R_{OUT}$ row.	4/23/04
B	T6	4	AC Characteristics Table - added thermal note.	2/26/10
		6	Updated Wiring the Differential input to Accept Single Ended Levels section.	
		7	Updated LVPECL Clock Input Interface section.	
	T9	12	Ordering Info Table - removed the ICS prefix from the Part/Order Number column. Added lead-free marking. Updated header/footer of datasheet.	



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