1:1 DIFFERENTIAL-TO-LVDS ZERO DELAY CLOCK GENERATOR

ICS8745B-21

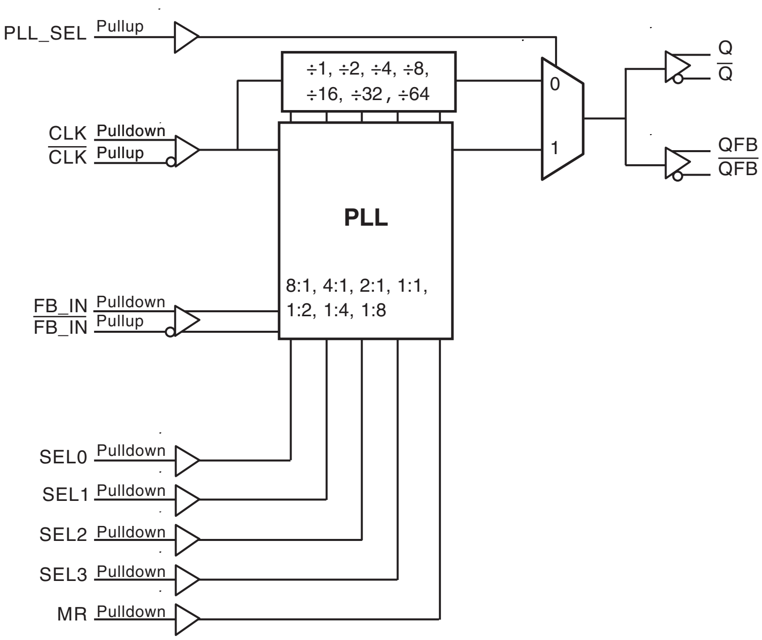
Description

The ICS8745B-21 is a highly versatile 1:1 LVDS Clock Generator and a member of the HiPerClockS™ f family of High Performance Clock Solutions from IDT. The ICS8745B-21 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The Reference Divider, Feedback Divider and Output Divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve "zero delay" between the input clock and the output clock. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

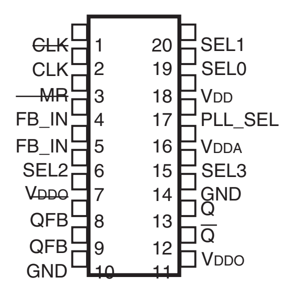
Features

- One differential LVDS output designed to meet or exceed the requirements of ANSI TIA/EIA-644 One differential feedback output pair
- Differential CLK, CLK input pair
- CLKx, CLKx pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 30ps (maximum)
- Output skew: 35ps (maximum)
- Static phase offset: 25ps ± 125ps
- Full 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8745B-21

20-Lead SOIC
7.5mm x 12.8mm x 2.3mm package body
M Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	$\overline{CLK}$	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output $\overline{Q}$ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
4	$\overline{FBIN}$	Input	Pullup	Inverting differential feedback input to phase detector for regenerating clocks with "Zero Delay."
5	FBIN	Input	Pulldown	Non-inverted differential feedback input to phase detector for regenerating clocks with "Zero Delay."
6, 15, 19, 20	SEL2, SEL3, SEL0 SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
7, 11	V_{DDO}	Power		Output supply pins.
8, 9	$\overline{QFB}$/QFB	Output		Differential feedback output pair. LVDS interface levels.
10, 14	GND	Power		Power supply ground.
12, 13	$\overline{Q}$/Q	Output		Differential output pair. LVDS interface levels.
16	V_{DDA}	Power		Analog supply pin.
17	PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. LVCMOS/LVTTL interface levels.
18	V_{DD}	Power		Core supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kZ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kZ

Function Tables

Table 3A. Control Input Function Table

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	$Q/\overline{Q}$
0z	0	0	0	250 - 700	÷1
0	0	0	1	125 - 350	÷1
0	0	1	0	62.5 - 175	÷1
0	0	1	1	31.25 - 87.5	÷1
0	1	0	0	250 - 700	÷2
0	1	0	1	125 - 350	÷2
0	1	1	0	62.5 - 175	÷2
0	1	1	1	250 - 700	÷4
1	0	0	0	125 - 350	÷4
1	0	0	1	250 - 700	÷8
1	0	1	0	125 - 350	x2
1	0	1	1	62.5 - 175	x2
1	1	0	0	31.25 - 87.5	x2
1	1	0	1	62.5 - 175	x4
1	1	1	0	31.25 - 87.5	x4
1	1	1	1	31.25 - 87.5	x8

*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

Table 3B. PLL Bypass Function Table

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	$Q/\overline{Q}$
0z	0	0	0	÷4
0	0	0	1	÷4
0	0	1	0	÷4
0	0	1	1	÷8
0	1	0	0	÷8
0	1	0	1	÷8
0	1	1	0	÷16
0	1	1	1	÷16
1	0	0	0	÷32
1	0	0	1	÷64
1	0	1	0	÷2
1	0	1	1	÷2
1	1	0	0	÷4
1	1	0	1	÷1
1	1	1	0	÷2
1	1	1	1	÷1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, t_{JA}	46.2·C/W (0 lfpm)
Storage Temperature, T_{STG}	-65·C to 150·C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				125	mA
I_{DDA}	Analog Supply Current				17	mA
I_{DDO}	Output Supply Current				59	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SEL[0:3], MR	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		PLL_SEL	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	SEL[0:3], MR	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		PLL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, FB_IN	$V_{DD} = V_{IN} = 3.465V$			150	µA
		$\overline{\text{CLK}}$, $\overline{\text{FB\_IN}}$	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK, FB_IN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		$\overline{\text{CLK}}$, $\overline{\text{FB\_IN}}$	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for CLK, $\overline{\text{CLK}}$ is $V_{DD} + 0.3V$.

Table 4D. LVDS DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		320	440	550	mV
GV_{OD}	V_{OD} Magnitude Change			0	50	mV
V_{OS}	Offset Voltage		1.05	1.2	1.35	V
GV_{OS}	V_{OS} Magnitude Change				25	mV

Table 5. Input Frequency Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{IN}	Input Frequency	CLK, $\overline{\text{CLK}}$	PLL_SEL = 1	31.25		700	µA
			PLL_SEL = 0			700	V

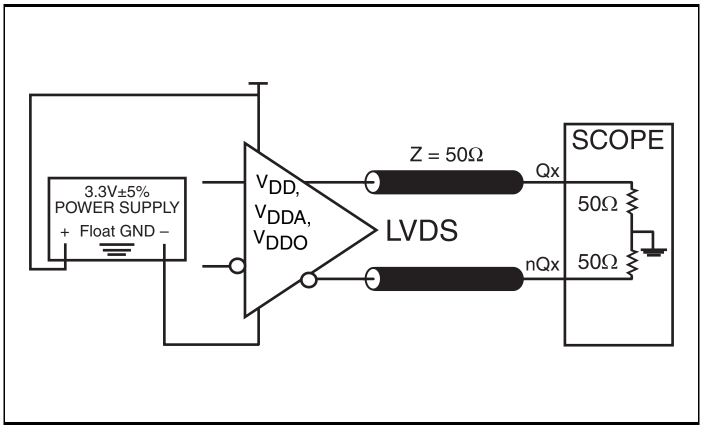
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

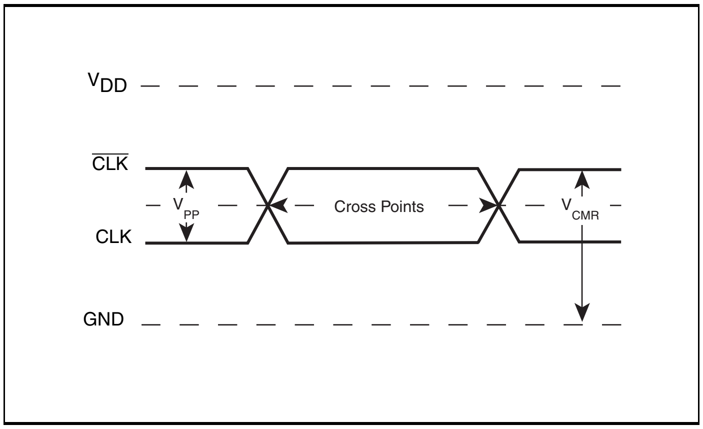
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V, f ƒ 700MHz	3.1	3.4	4.0	ns
*t*sk(Ø)	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-100	25	150	ps
*t*sk(o)	Output Skew; NOTE 3, 5				35	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 5, 6				30	ps
*t*jit(t)	Phase Jitter; NOTE 4, 5, 6				±52	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time; NOTE 7	20% to 80%	200		700	ps
odc	Output Duty Cycle		46	50	54	%

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 6: Characterized at VCO frequency of 622MHz.
NOTE 7: Measured from the 20% to 80% points. Guaranteed by characterization. Not production tested.

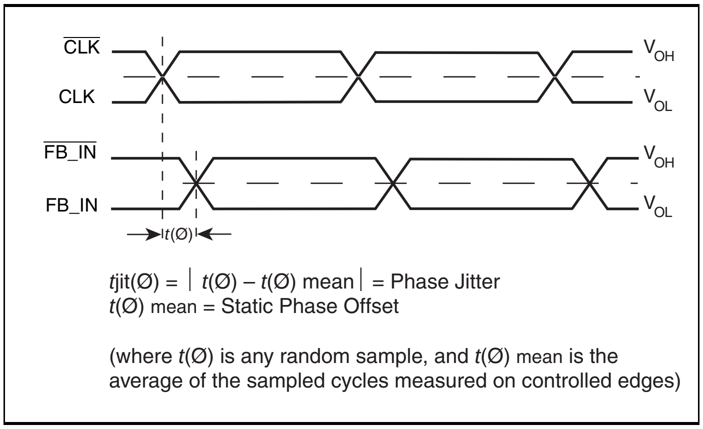
Parameter Measurement Information



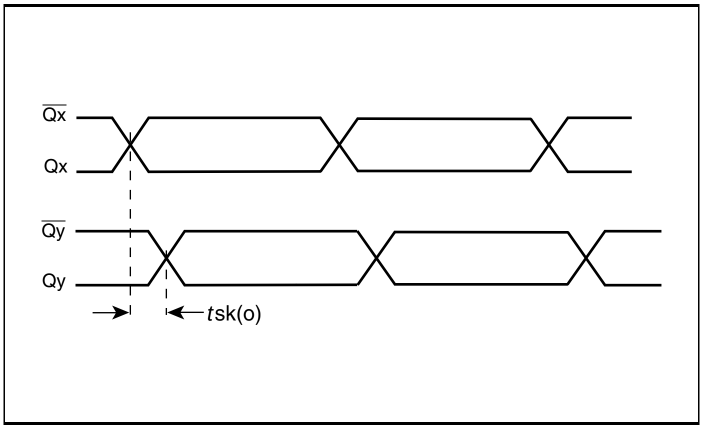
3.3V LVDS Output Load AC Test Circuit



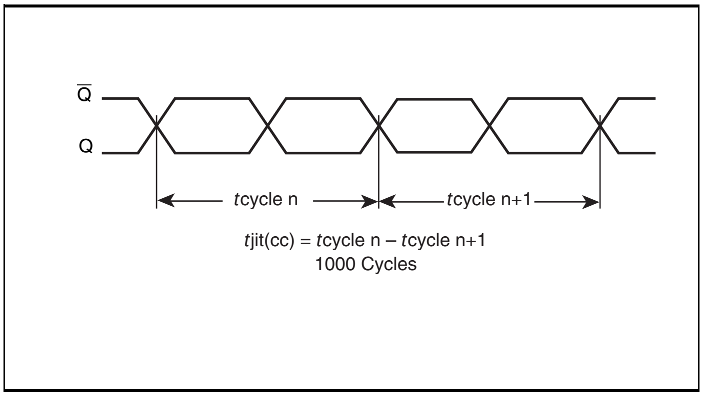
Differential Input Level



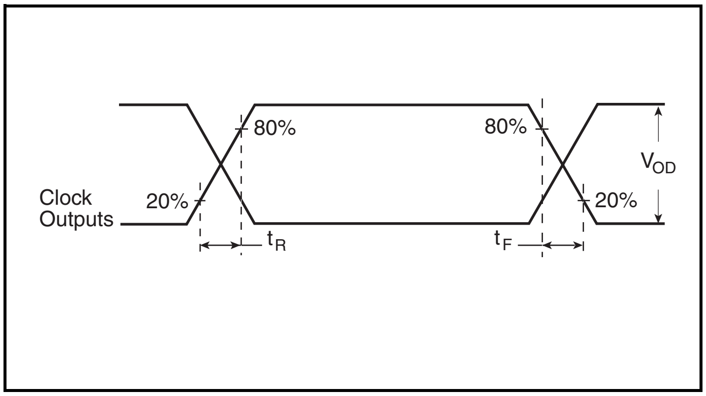
Phase Jitter and Static Phase Offset



Output Skew

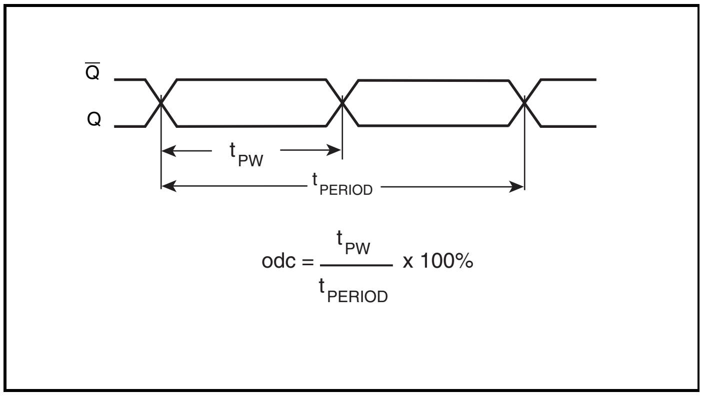


Cycle-to-Cycle Jitter

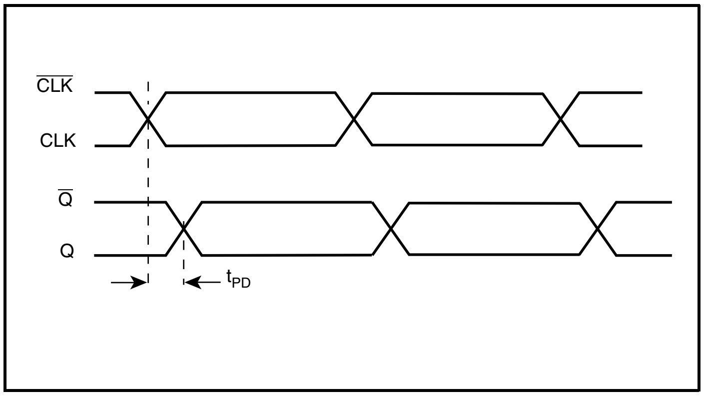


Output Rise/Fall Time

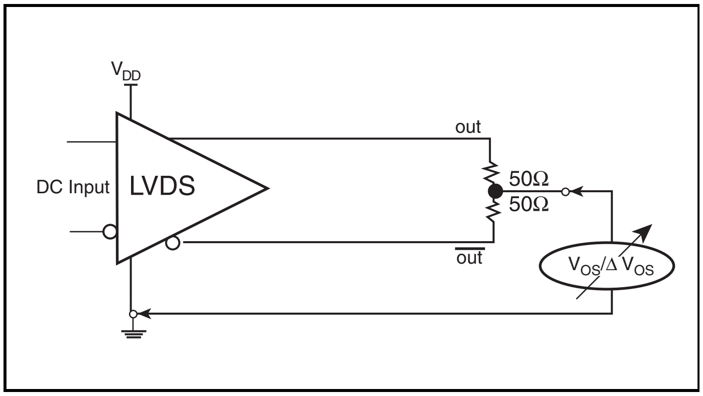
Parameter Measurement Information, continued



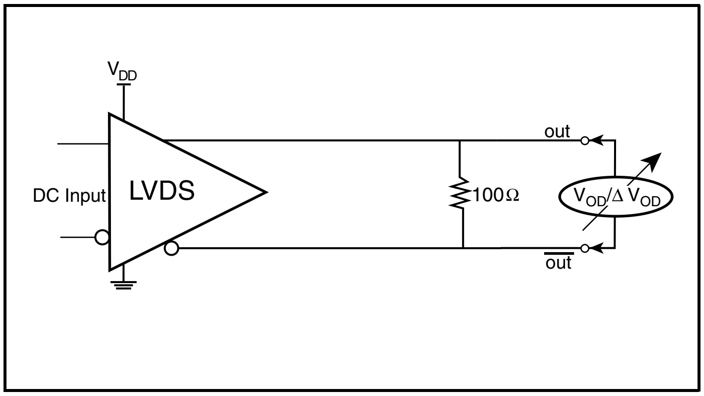
Output Duty Cycle



Propagation Delay



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8745B-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Z resistor along with a 10pF and a .01pF bypass capacitor should be connected to each V_{DDA} pin. The 10Z resistor can also be replaced by a ferrite bead.

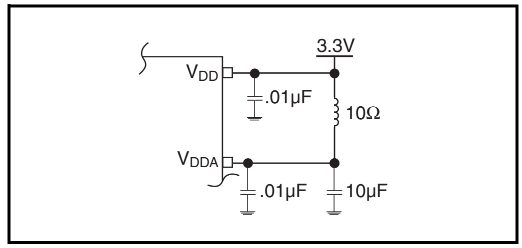


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

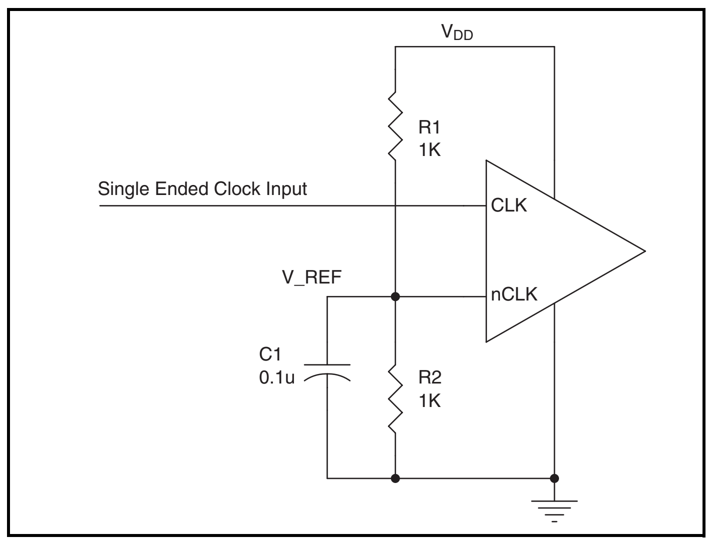


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /$\overline{\text{CLK}}$ accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the HiPerClockS CLK/$\overline{\text{CLK}}$ input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

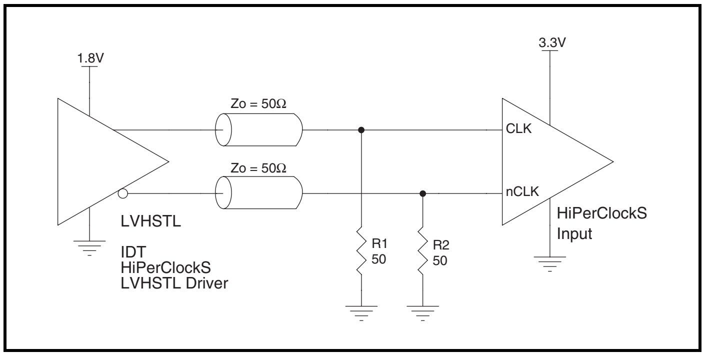


Figure 3A. HiPerClockS CLK/$\overline{\text{CLK}}$ Input Driven by an IDT HiPerClockS LVHSTLDriver

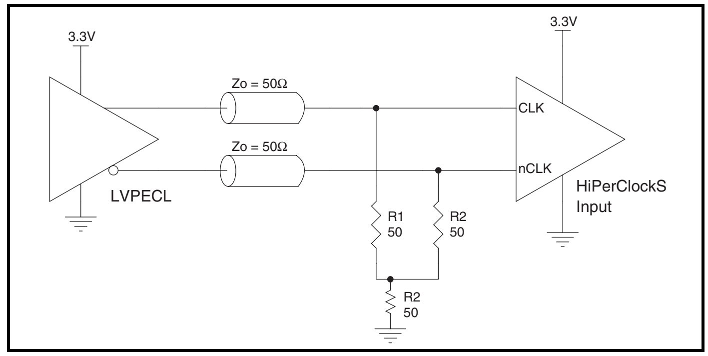


Figure 3B. HiPerClockS CLK/$\overline{\text{CLK}}$ Input Driven by a 3.3V LVPECL Driver

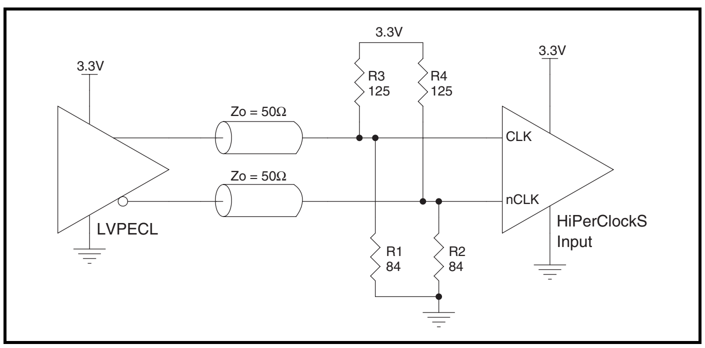


Figure 3C. HiPerClockS CLK/$\overline{\text{CLK}}$ Input Driven by a 3.3V LVPECL Driver

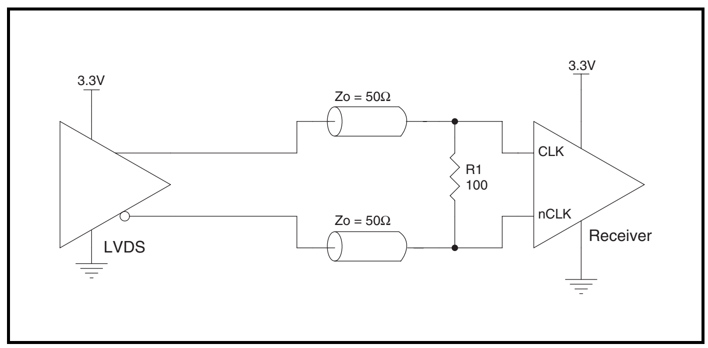


Figure 3D. HiPerClockS CLK/$\overline{\text{CLK}}$ Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/$\overline{\text{CLK}}$ INPUT:

For applications not requiring the use of the differential input, both CLK and $\overline{\text{CLK}}$ can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVDS Output

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

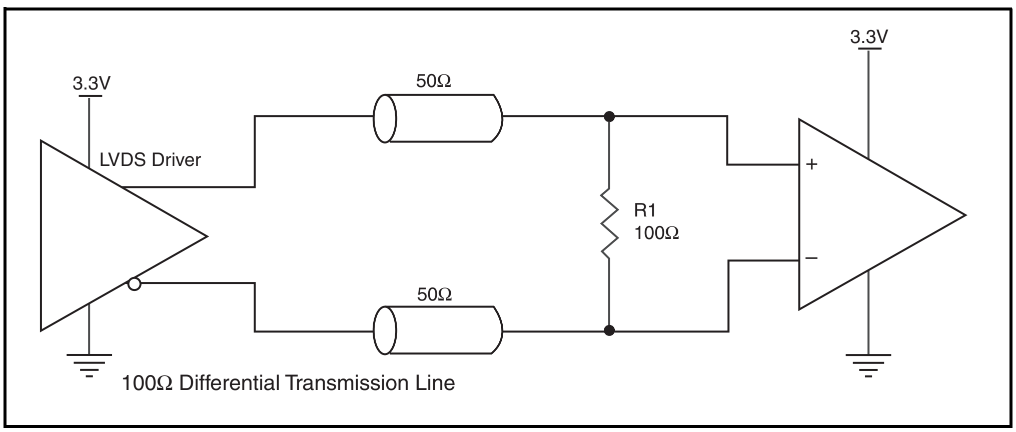


Figure 4. Typical LVDS Driver Termination

Schematic Example

The schematic of the ICS8745B-21 layout example is shown in *Figure 5A.* The ICS8745B-21 recommended PCB board layout for this example is shown in *Figure 5B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

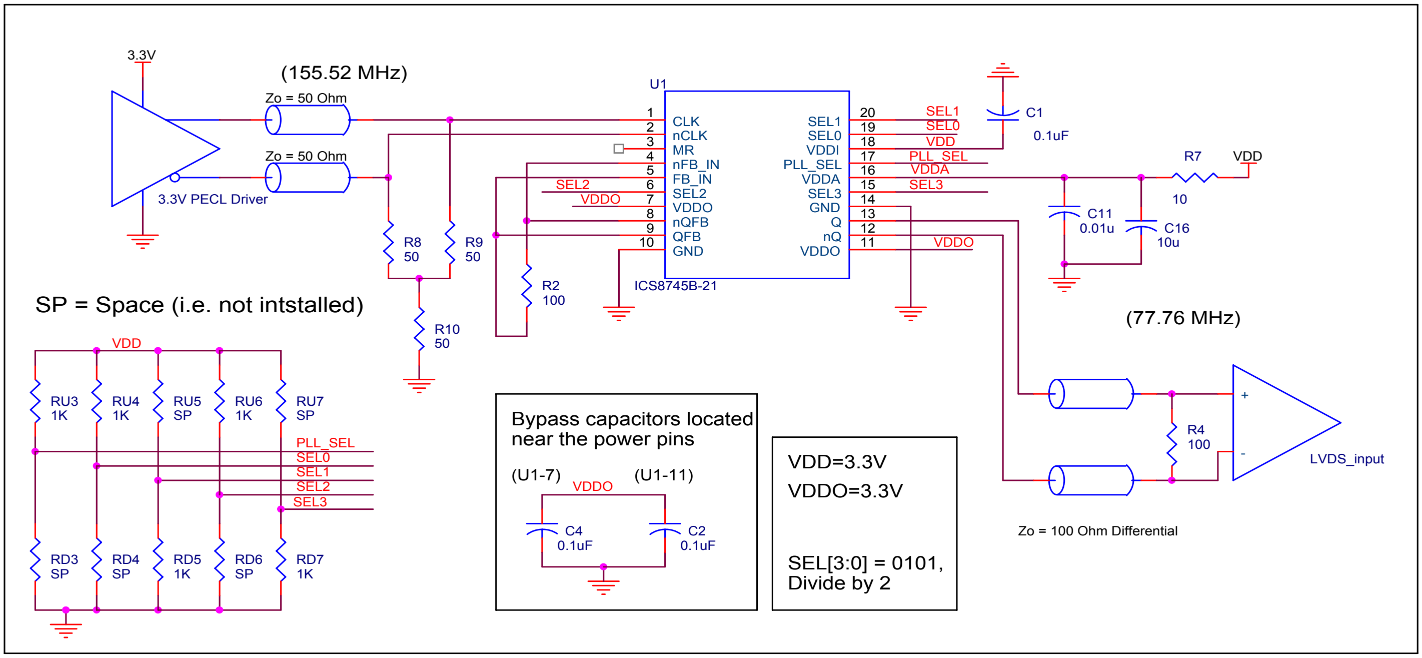


Figure 5A. ICS8745B-21 LVDS Zero Delay Buffer Schematic Example

The following component footprints are used in this layout example.

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have the same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

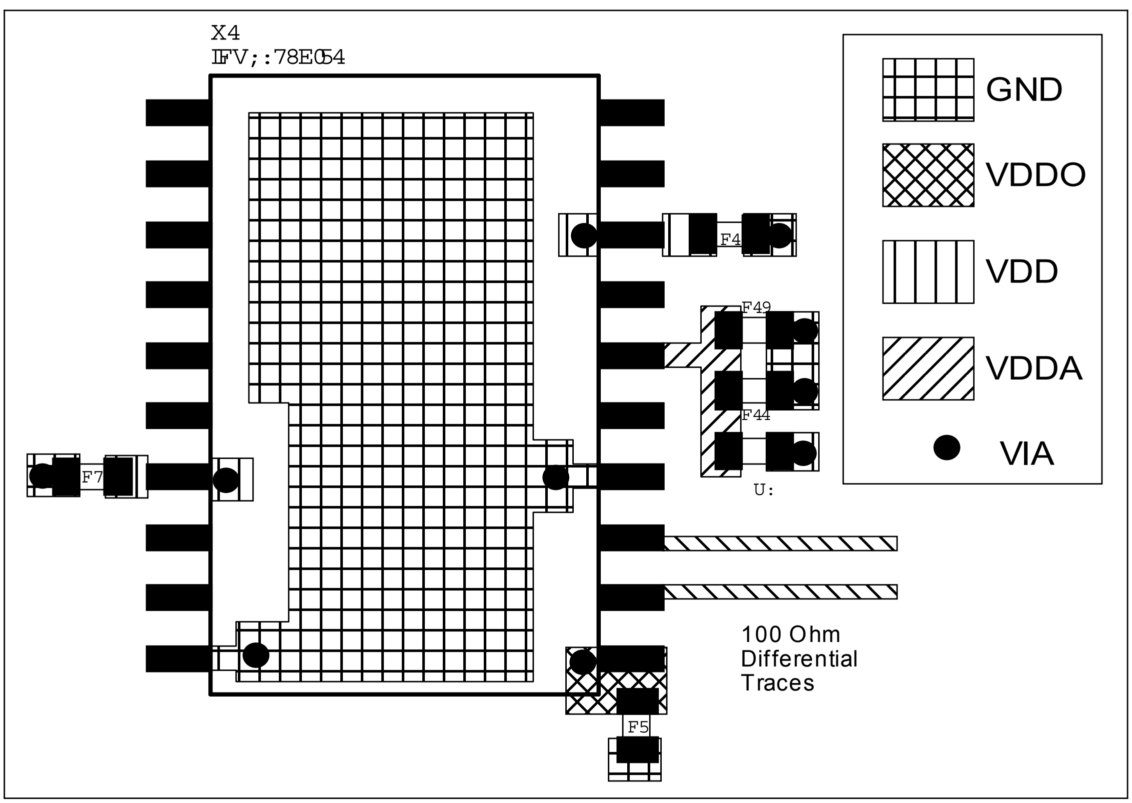


Figure 5B. PCB Board Layout for ICS8745B-21

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8745B-21.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8745B-21 is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (125mA + 17mA) = **492mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 59mA = **204mW**

Total Power$_{\_MAX}$ = 492mW + 204mW = **696mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = t_{JA} * Pd_total + T_A

Tj = Junction Temperature

t_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance t_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 7below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.696W * 39.7°C/W = 97.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 7. Thermal Resitance t_{JA} for 20 Lead TSSOP, Forced Convection

t_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Reliability Information

Table 8. t_{JA} vs. Air Flow Table for a 20 Lead TSSOP

t_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

Transistor Count

The transistor count for ICS8745B-21 is: 2772

Package Outline and Package Dimension

Package Outline - M Suffix for 20 Lead SOIC

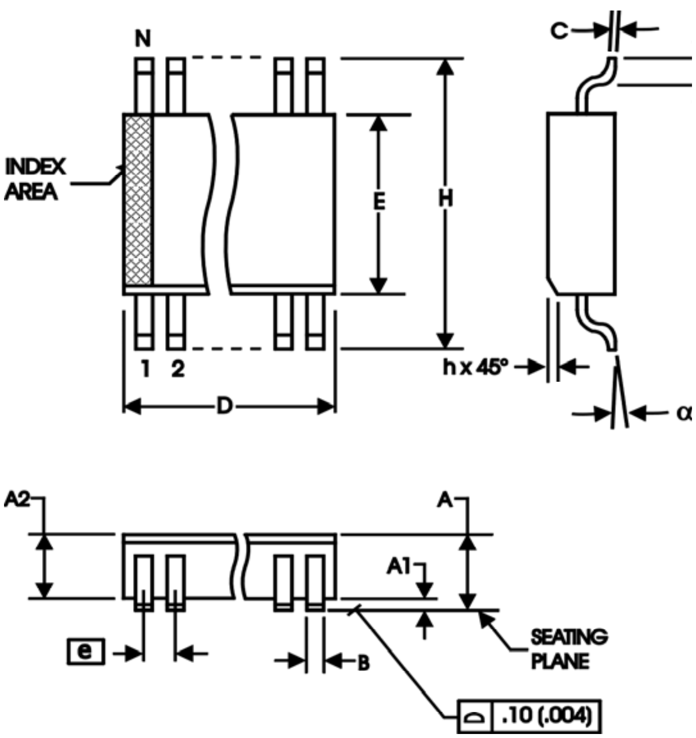


Table 9. Package Dimensions for 20 Lead SOIC

300 Millimeters All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		2.65
A1	0.10	
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 Basic	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
d	0°	7°

Reference Document: JEDEC Publication 95, MS-013, MS-119

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8745BM-21	ICS8745BM-21	20 Lead SOIC	Tube	0·C to 70·C
8745BM-21T	ICS8745BM-21	20 Lead SOIC	1000 Tape & Reel	0·C to 70·C
8745BM-21LF	TBD	"Lead-Free" 20 Lead SOIC	Tube	0·C to 70·C
8745BM-21LFT	TBD	"Lead-Free" 20 Lead SOIC	1000 Tape & Reel	0·C to 70·C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4D	5	LVDS DC Characteristics Table - modified VOS 0.90V min. to 1.05V min, 1.15V typical to 1.2V typical, and 1.4V max. to 1.35V max.	3/17/04
B	 T9	1 14	Added Lead-Free bullet. Ordering Information Table - added Lead-Free part and note.	12/2/04
C	T6	7 12 15	AC Characteristics Table - changed t_{PD} max limit from 3.7ns to 4.0ns. Added Recommendations for Unused Input & Output Pins. Added Power Considerations section. Updated format throughout the datasheet.	4/17/07

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