Integrated Circuit Systems, Inc.

ICS87952I-147

LOW SKEW, 1-TO-11 LVCMOS / LVTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER

GENERAL DESCRIPTION

The ICS87952I-147 is a low voltage, low skew LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. With output frequencies up to 180MHz, the ICS87952I-147 is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS87952I-147 contains frequency configurable outputs and an external feedback input for regenerating clocks with "zero delay".

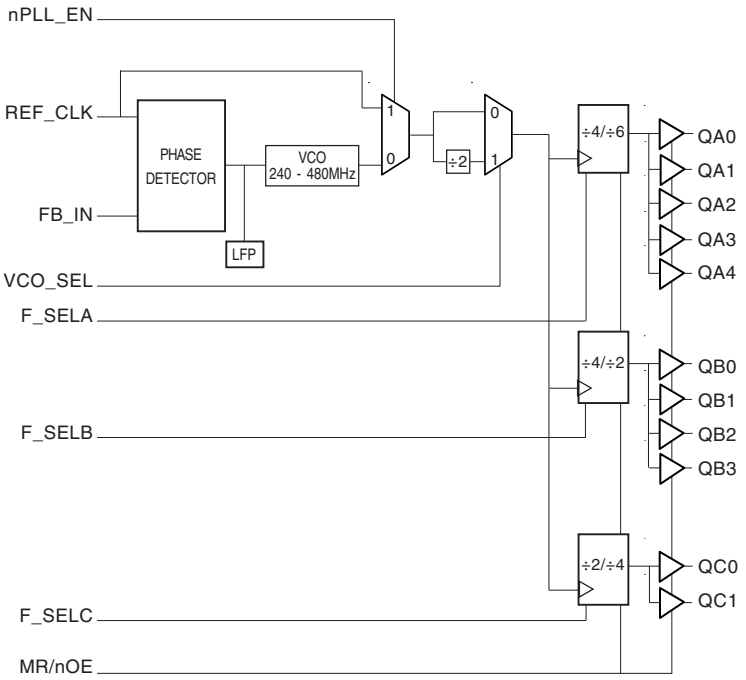
For test and system debug purposes, the nPLL_EN input allows the PLL to be bypassed. When HIGH, the MR/nOE input resets the internal dividers and forces the outputs to the high impedance state.

The low impedance LVCMOS/LVTTL outputs of the ICS87952I-147 are designed to drive terminated transmission lines. The effective fanout of each output can be doubled by utilizing the ability of each output to drive two series terminated transmission lines.

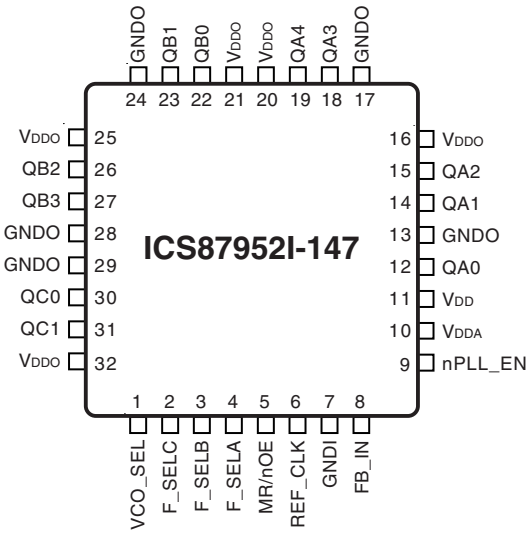
FEATURES

- Fully integrated PLL
- Eleven LVCMOS / LVTTL outputs, 7Ω typical output impedance
- LVCMOS / LVTTL REF_CLK input
- Output frequency range up to 180MHz at V_{DD} = 3.3V ± 5%
- VCO range: 240MHz - 480MHz
- External feedback for "zero delay" clock regeneration
- Cycle-to-cycle jitter: 100ps (maximum)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	VCO_SEL	Input	Pulldown	VCO select input. LVCMOS / LVTTL interface levels.
2	F_SELC	Input	Pulldown	Determines output divider values for Bank C as described in Table 3A. LVCMOS / LVTTL interface levels.
3	F_SELB	Input	Pulldown	Determines output divider values for Bank B as described in Table 3A. LVCMOS / LVTTL interface levels.
4	F_SELA	Input	Pulldown	Determines output divider values for Bank A as described in Table 3A. LVCMOS / LVTTL interface levels.
5	MR/nOE	Input	Pulldown	Active High Master Reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in Hi-Z. When logic LOW, the internal dividers and the outputs are enabled. Reset not required on power-up. LVCMOS / LVTTL interface levels.
6	REF_CLK	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.
7	GNDI	Power		Internal power supply ground.
8	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTL interface levels.
9	nPLL_EN	Input	Pulldown	PLL select input. Selects between REF_CLK and the PLL. When HIGH, selects REF_CLK. When LOW, selects PLL. LVCMOS / LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12, 14, 15, 18, 19	QA0, QA1, QA2, QA3, QA4	Output		Bank A clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
13, 17, 24, 28, 29	GNDO	Power		Output power supply ground.
16, 20, 21, 25, 32	V_{DDO}	Power		Output supply pins.
22, 23, 26, 27	QB0, QB1, QB2, QB3	Output		Bank B clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.
30, 31	QC0, QC1	Output		Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDA}, V_{DDO} = 3.465V		25		pF
R_{OUT}	Output Impedance			7		Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Input	Output	Input	Output	Input	Output
F_SELA	QA0:QA4	F_SELB	QB0:QB3	F_SELC	QC0:QC1
0	÷4	0	÷4	0	÷2
1	÷6	1	÷2	1	÷4

TABLE 3B. CONTROL SELECT FUNCTION TABLE

Control Input	Logic 0	Logic 1
VCO_SEL	fVCO	fVCO/2
MR/nOE	Output Enable	HiZ
nPLL_EN	Enable PLL	Disable PLL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				160	mA
I_{DDA}	Analog Supply Current			15	20	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, MR/nOE, FB_IN, VCO_SEL, F_SELA:F_SELC, nPLL_EN	$V_{DD} = V_{IN} = 3.465V$			120	µA
I_{IL}	Input Low Current	REF_CLK, MR/nOE, FB_IN, VCO_SEL, F_SELA:F_SELC, nPLL_EN	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-120			µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -20mA	2.4			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 20mA			0.5	V

NOTE 1: Outputs terminaed with 50Ω to V_{DDO}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit" diagram.

TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

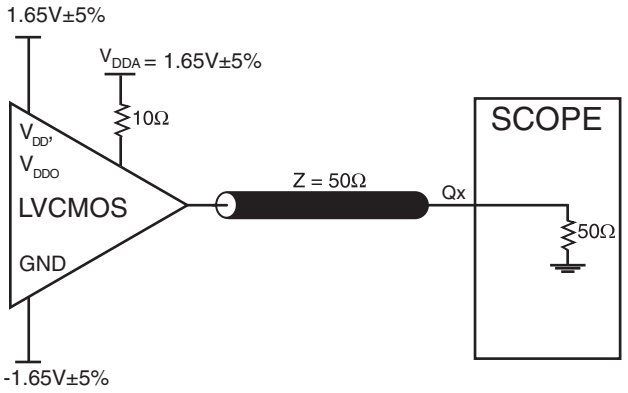
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency NOTE: Input reference frequency is limited by the divider selection and the VCO lock range.				100	MHz

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

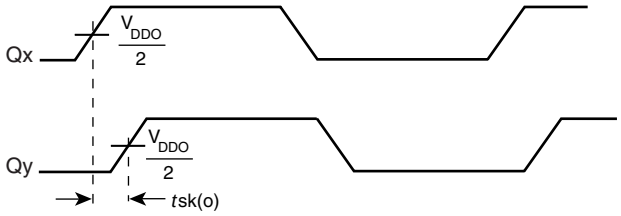
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency (PLL Mode)	QC, QB (÷2)		180			MHz
		QA, QB, QC (÷4)		120			MHz
		QA (÷6)		80			MHz
t_{PD}	Propagation Delay, REF_CLK to FB_IN Delay, (Static Phase Offset); NOTE 1		REF_CLK = 50MHz	-100		200	ps
f_{VCO}	PLL VCO Lock Range			240		480	MHz
*t*sk(o)	Output Skew; NOTE 2, 3	All Outputs	Any Frequency			150	ps
		Within QA Bank				100	ps
		Within QB Bank				100	ps
		Within QC Bank				50	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 3		Output Frequencies Mixed			400	ps
		All Outputs	Same Frequency			100	ps
*t*jit(per)	Period Jitter		Output Frequencies Mixed			450	ps
		All Outputs	Same Frequency			100	ps
t_L	PLL Lock Time					10	ms
t_R / t_F	Output Rise/Fall Time		0.8V to 2.0V	0.10		1.0	ns
t_{PLZ}, t_{PHZ}	Output Disable Time			1.5		8	ns
t_{PZL}	Output Enable Time			2		10	ns
odc	Output Duty Cycle			47	50	53	%

All parameters measured at f_{MAX} unless noted otherwise.
All outputs loaded at 50Ω to $V_{DDO}/2$.
NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

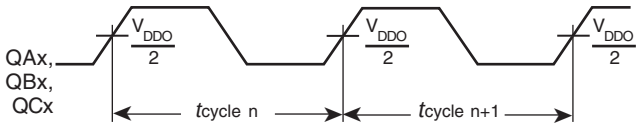
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT

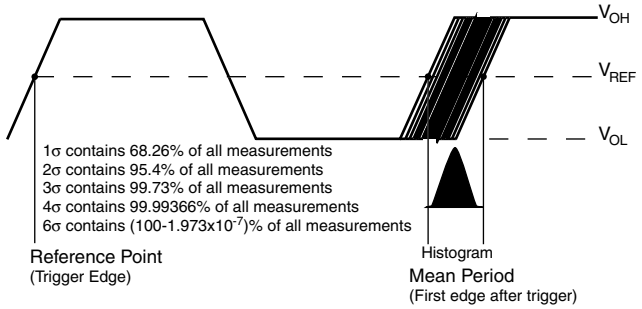


OUTPUT SKEW

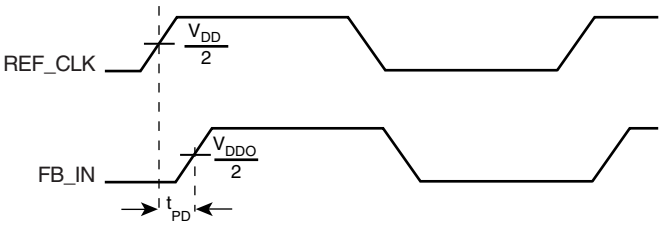


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

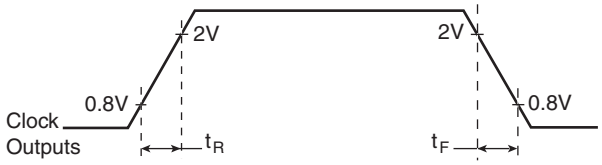
CYCLE-TO-CYCLE JITTER



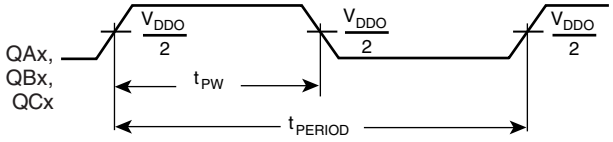
PERIOD JITTER



REF_CLK TO FB_IN DELAY



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS87952I-147 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10mF and a .01mF bypass capacitor should be connected to each V_{DDA} pin.

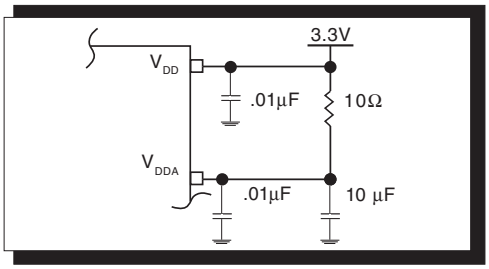


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS:
All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:
All unused LVCMOS output can be left floating. There should be no trace attached.

LAYOUT GUIDELINE

The schematic of the ICS87952I-147 layout example is shown in *Figure 2A.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

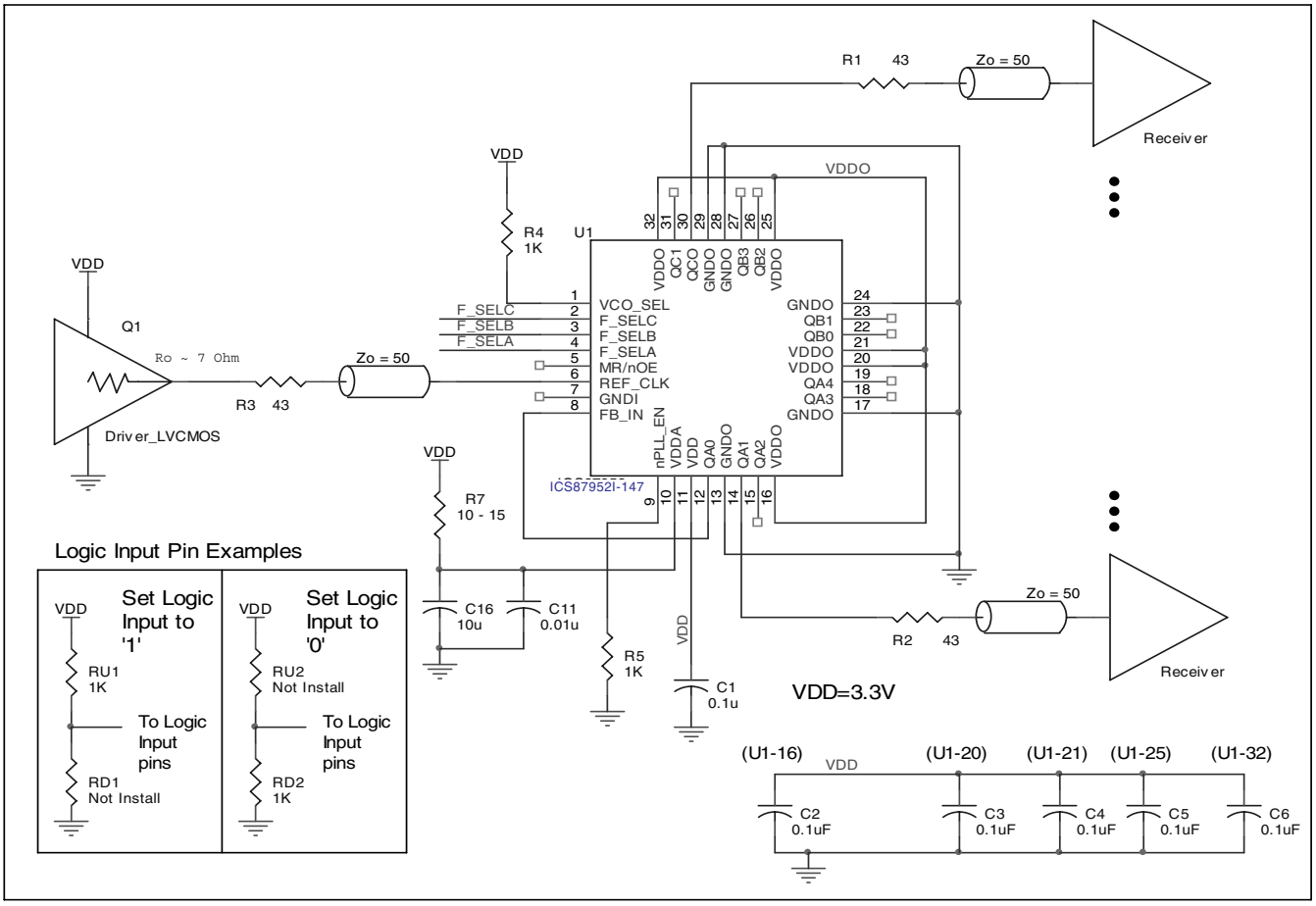


FIGURE 2A. ICS87952I-147 LVCMOS/LVTTL CLOCK MULTIPLIER/ZERO DELAY BUFFER SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- The series termination resistors should be located as close to the driver pins as possible.

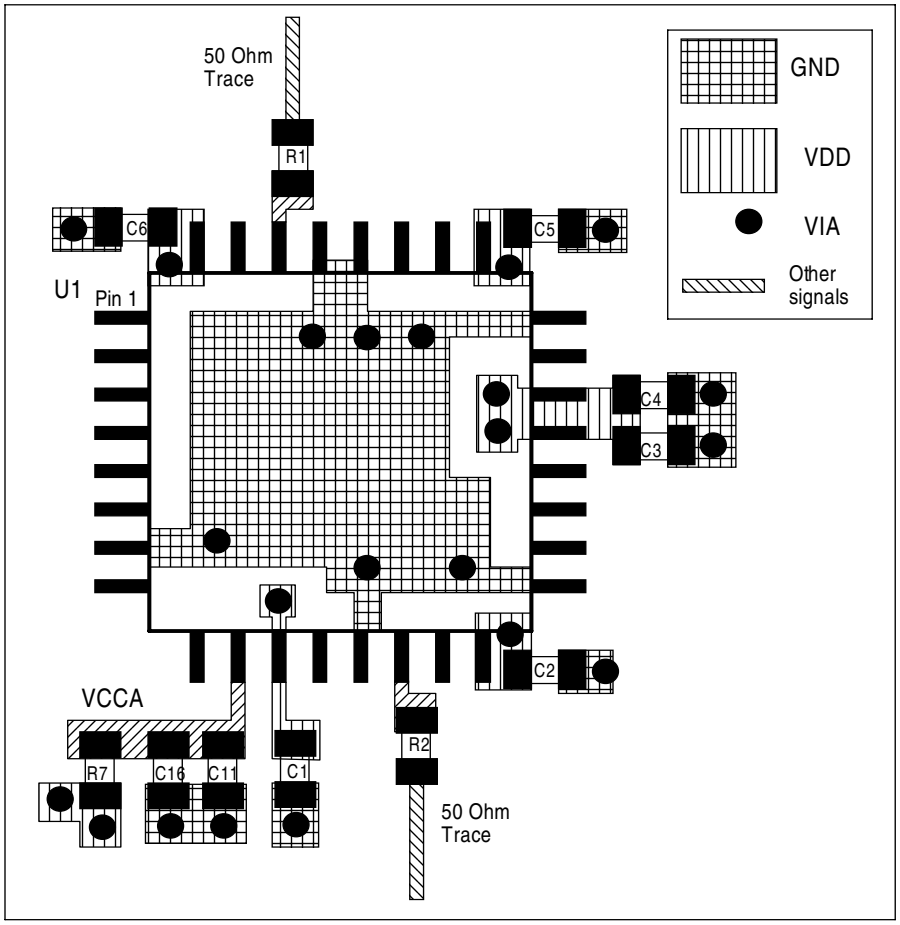


FIGURE 2B. PCB BOARD LAYOUT FOR ICS87952I-147

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87952I-147 is: 2882

Compatible with MPC952, MPC9352, MPC93R52

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

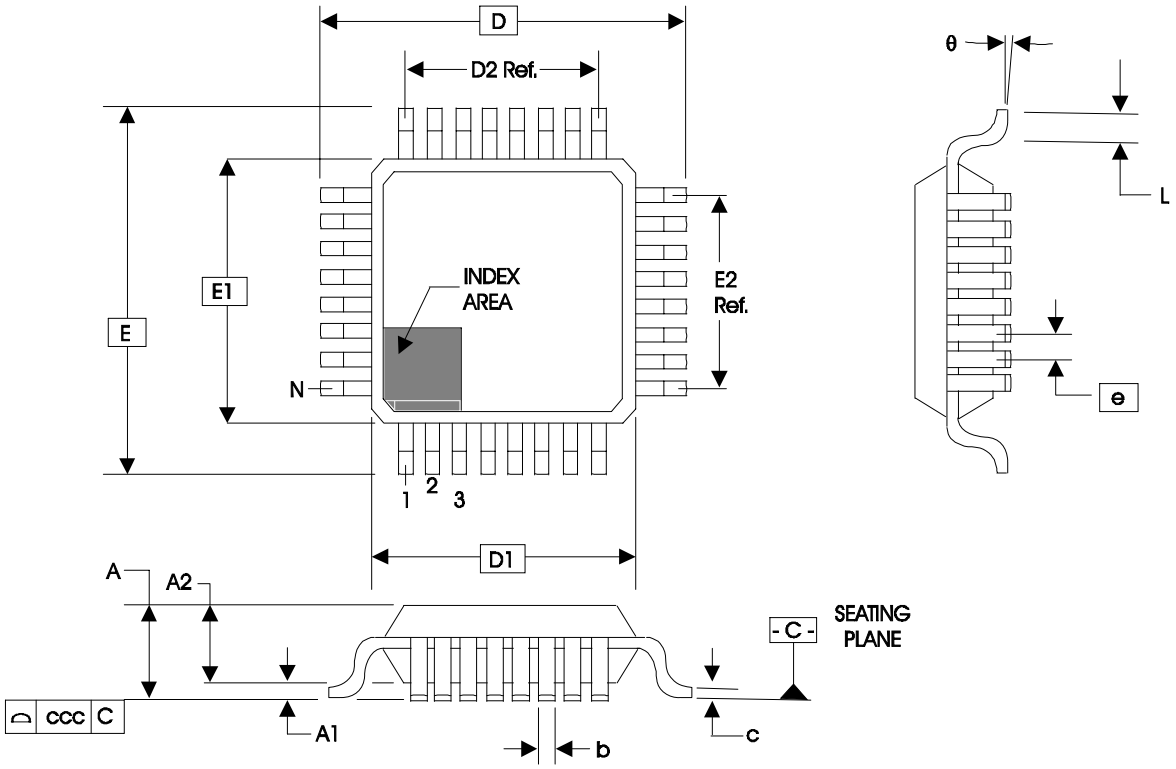


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87952AYI-147	ICS87952AI147	32 Lead LQFP	tray	-40°C to 85°C
ICS87952AYI-147T	ICS87952AI147	32 Lead LQFP	1000 tape & reel	-40°C to 85°C
ICS87952AYI-147LF	ICS7952AI147L	32 Lead "Lead-Free" LQFP	tray	-40°C to 85°C
ICS87952AYI-147LFT	ICS7952AI147L	32 Lead "Lead-Free" LQFP	1000 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T6	4	AC Characteristics Table - t_{PD}, deleted 0ps typical and deleted t_{PW} row.	4/10/06