PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8536-02

LOW SKEW, 1-TO-6, DUAL CRYSTAL OR LVCMOS INPUT -TO-3.3V, 2.5V LVPECL FANOUT BUFFER

GENERAL DESCRIPTION

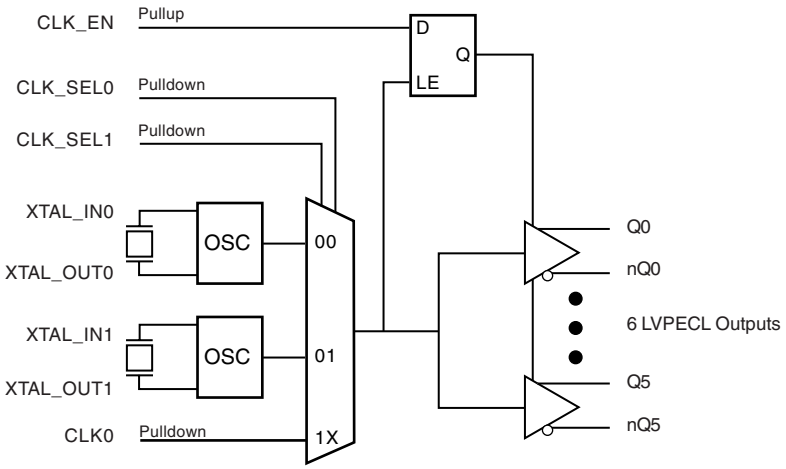
The ICS8536-02 is a low skew, high performance 1-to-6, Dual Crystal or LVCMOS Input-to-3.3V, 2.5V LVPECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8536-02 has selectable crystal or single ended clock input. The single ended clock input accepts LVCMOS or LVTTL input levels and translates them to LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8536-02 ideal for those applications demanding well defined performance and repeatability.

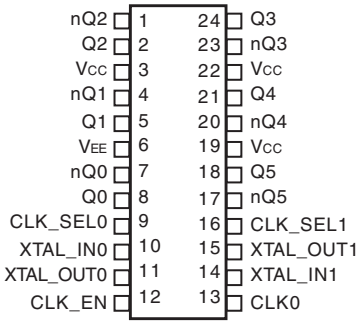
FEATURES

- Six 3.3V, 2.5V LVPECL outputs
- Selectable crystal oscillator or LVCMOS/LVTTL clock input
- Maximum output frequency: 266MHz
- Crystal frequency range: 14MHz - 40MHz
- Output skew: TBD
- Part-to-part skew: TBD
- Additive phase jitter, RMS: TBD
- Propagation delay: 1.69ns (typical)
- Full 3.3V or 2.5V supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS8536-02
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Νυμ βερ	Ναμ ε	Τψπε		Δεσχριπτιον
1, 2	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
3, 19, 22	V_{CC}	Power		Power supply pins.
4, 5	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
6	V_{EE}	Power		Negative supply pins.
7, 8	nQ0, Q0	Ouput		Differential output pair. LVPECL interface levels.
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select pins. LVCMOS/LVTTL interface levels. See Table 3B.
10, 11	XTAL_IN0, XTAL_OUT0	Input		Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.
12	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, the outputs are disabled. LVCMOS / LVTTL interface levels. See Table 3A.
13	CLK0	Input	Pulldown	LVCMOS/LVTTL clock input.
14, 15	XTAL_IN1, XTAL_OUT1	Input		Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.
17, 18	nQ5, Q5	Output		Differential output pair. LVPECL interface levels.
20, 21	nQ4, Q4	Output		Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs	
CLK_EN	**CLK_SEL1**	**CLK_SEL0**	**Selected Source**	**Q0:Q5**	**nQ0:nQ5**
0	0	0	XTAL0	Disabled	Disabled
0	0	1	XTAL1	Disabled	Disabled
0	1	X	CLK0	Disabled	Disabled
1	0	0	XTAL0	Enabled	Enabled
1	0	1	XTAL1	Enabled	Enabled
1	1	X	CLK0	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show in *Figure 1.*
In the active mode, the state of the outputs are a function of the selected clock input as described in Table 3B.

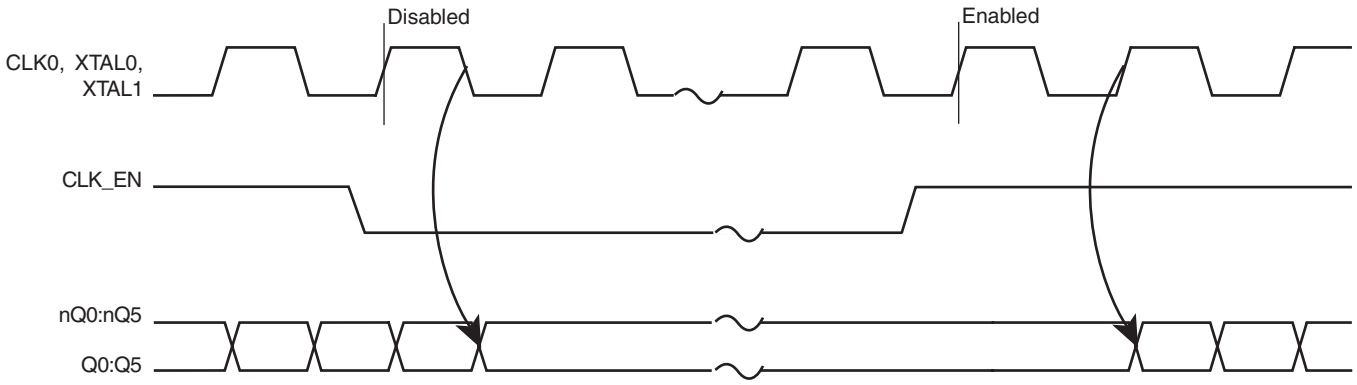


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Input	Outputs		Input to Output Mode	Polarity
CLK0	**Q0:Q5**	**nQ0:nQ5**		
0	LOW	HIGH	Single Ended to Differential	Non Inverting
1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section ""Wiring the Differential Input to Accept Single Ended Levels"".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			70		mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current			65		mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK_SEL0:1	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
		CLK_EN	V_{CC} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	CLK0, CLK_SEL0:1	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		CLK_EN	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5% OR 2.5V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		14		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay, NOTE 1			1.69		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2			TBD		ps
*t*sk(o)	Output Skew; NOTE 3, 4			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		TBD		ps
odc	Output Duty Cycle			50		%
$MUX_{-ISOLATION}$	MUX Isolation; NOTE 6	*f* = 150MHz		-76		dB
		f = 250MHz		-74		dB

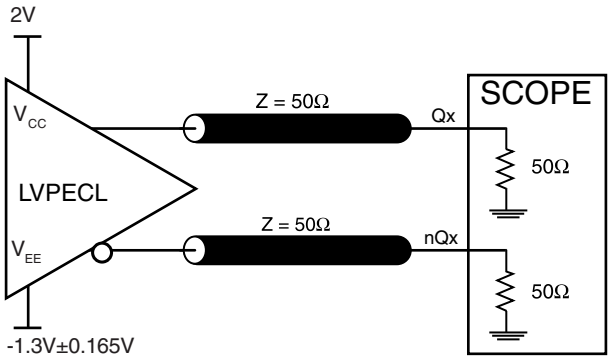
All parameters measured at f_{MAX} unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Driving only one input clock.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 6: XTAL's sensitivity measured while single-ended CLK0 driving data at 150MHz and 250MHz.

TABLE 6B. AC CHARACTERISTICS, V_{CC} = 2.5V±5%, TA = 0°C TO 70°C

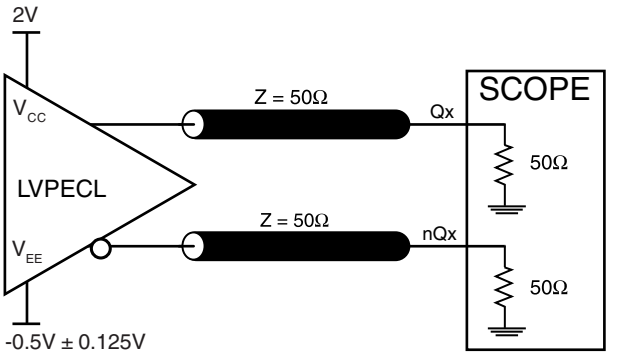
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				266	MHz
t_{PD}	Propagation Delay, NOTE 1			1.69		ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2			TBD		ps
*t*sk(o)	Output Skew; NOTE 3, 4			TBD		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 5			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		TBD		ps
odc	Output Duty Cycle			50		%
$MUX_{-ISOLATION}$	MUX Isolation; NOTE 6	*f* = 150MHz		-38		dB
		f = 250MHz		-27		dB

See notes in Table 6A above.

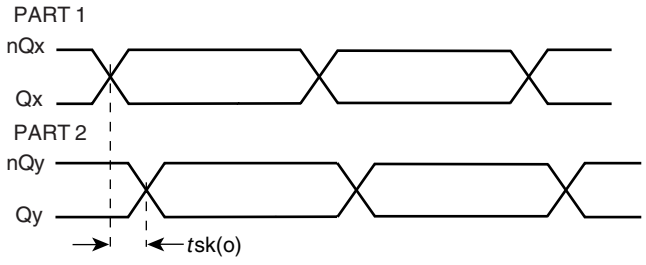
PARAMETER MEASUREMENT INFORMATION



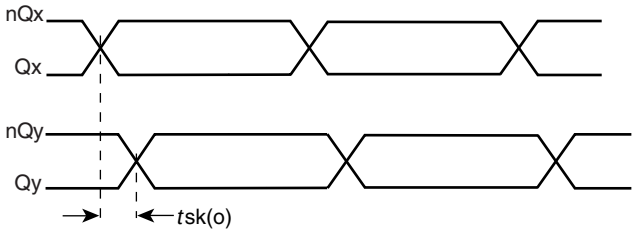
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



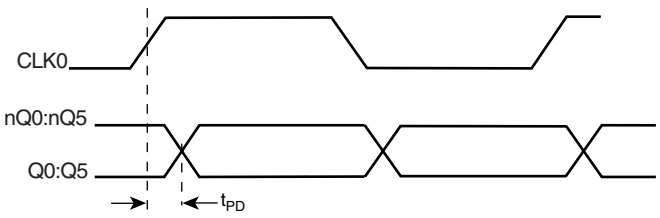
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



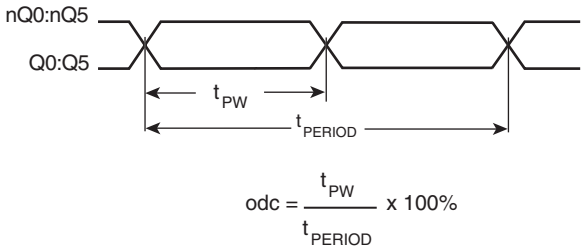
PART-TO-PART SKEW



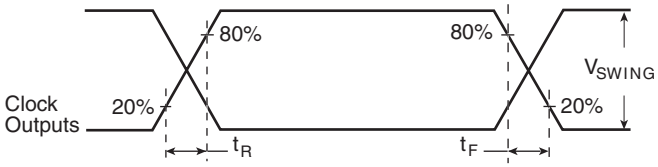
OUTPUT SKEW



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

The ICS8536-02 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

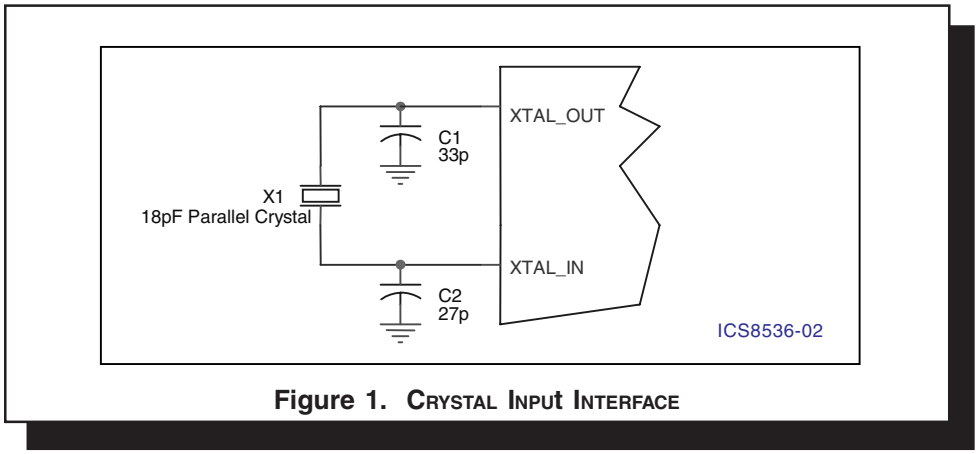


Figure 1. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK INPUT:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

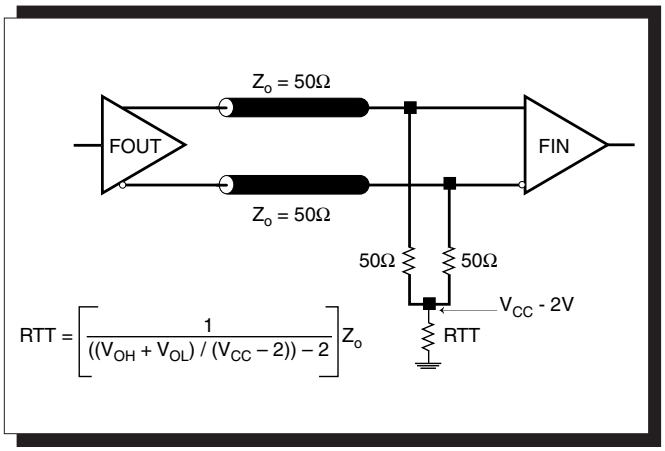


FIGURE 2A. LVPECL OUTPUT TERMINATION

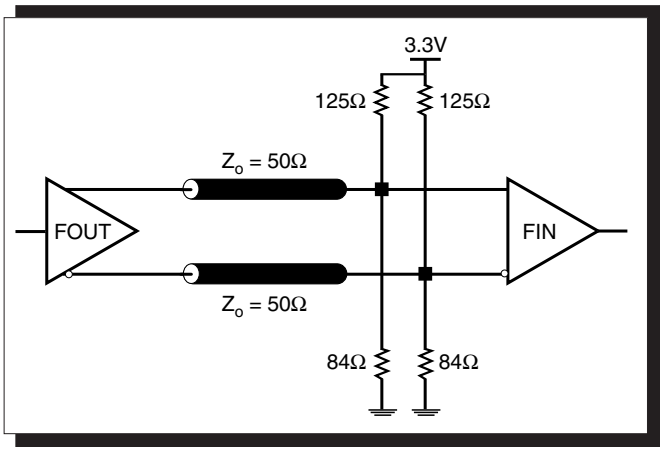


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 3A and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

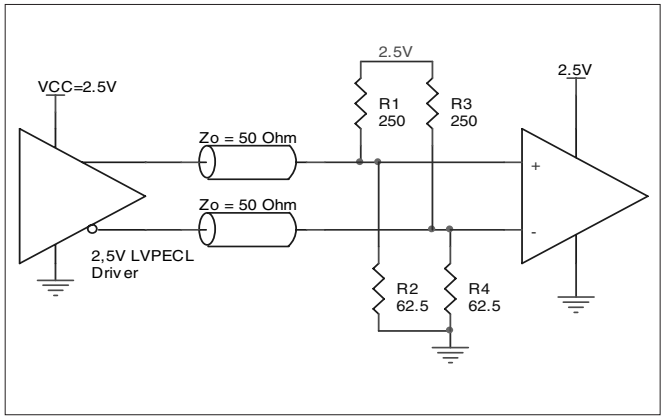


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

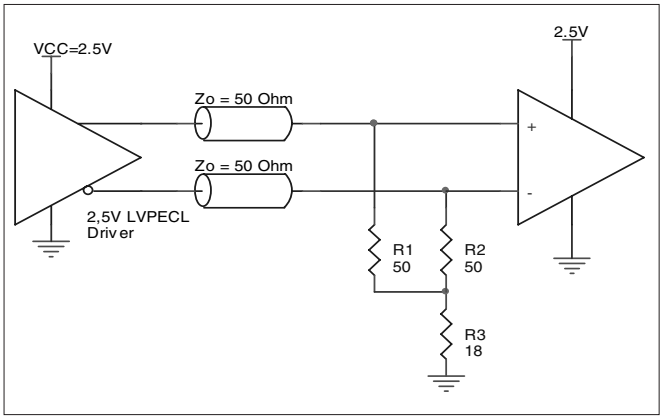


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

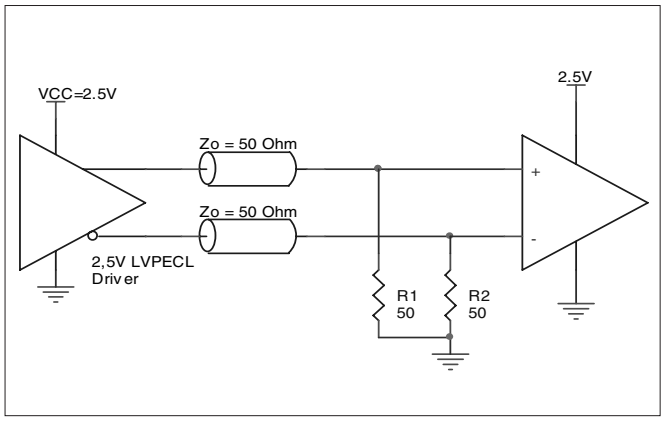


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8536-02. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8536-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 70mA = **242.55mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6* 30mW = **180mW**

Total Power $_{MAX}$ (3.465V, with all outputs switching) = 242.55mW + 180mW = 422.6**mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.423W * 65°C/W = 97.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 4.*

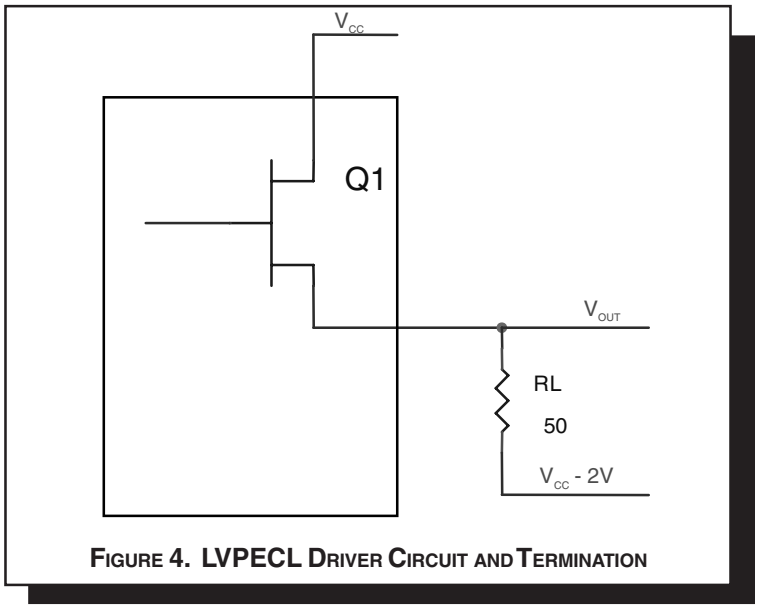


FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS8536-02 is: 467

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

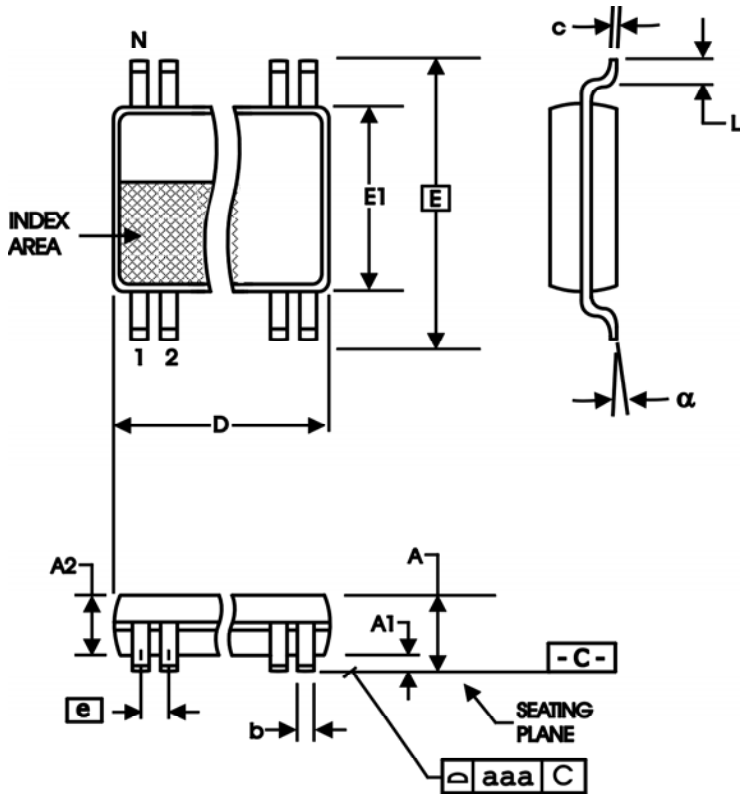


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8536AG-02	ICS8536AG-02	24 Lead TSSOP	tube	0°C to 70°C
ICS8536AG-02T	ICS8536AG-02	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS8536AG-02LF	TBD	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS8536AG-02LFT	TBD	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.