Data Sheet

S6D0144

Preliminary

128-RGB X 160-DOT SINGLE CHIP DRIVER IC
WITH INTERNAL GRAM FOR 262,144 Colors TFT-LCD

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Ver. 0.7

Prepared by	Checked by	Approved by
Hak-Seong. Lee hakseong.lee@samsung.com	Byoung-Ha, Kim bhkim21@samsung.com	Yhong-Deug, Ma yd.ma@samsung.com

System LSI Division
Device Solution Network
SAMSUNG ELECTRONICS CO., LTD.

CONTENTS

INTRODUCTION

S6D0144 is a single chip solution for TFT-LCD panel: source driver with built-in memory, gate driver and power circuits are integrated on this LSI. It can display to the maximum of 128-RGB x 160-dot graphics on 260k-color TFT-LCD panel.

S6D0144 supports 18-/16-/9-/8-bits high-speed parallel bus interfaces and Serial Peripheral Interface (SPI). In addition, the LSI has 18-/16-/6-bit RGB interface for motion picture display.

The motion picture area can be specified by Window Addressing Function. The specified window area can be updated selectively in order for motion picture to be able to be displayed independently of and simultaneously with still picture display.

S6D0144 has various functions for reducing the power consumption of TFT-LCD system: The LSI operates at low voltage and has internal GRAMs to store 128-RGB x 160-dot 260k-color image data. Additionally, it has an internal booster that generates the TFT-LCD driving voltage, breeder resistance and the voltage follower circuit for TFT-LCD driver.

S6D0144 is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDAs.

FEATURES

Overalls
- 128-RGB x 160-dot Resolution, 384ch Source Driver / 160ch Gate Driver

Various color-display control functions
- 262,144 colors can be displayed at the same time (including gamma adjust)
- 65,536 colors, 8 colors can be displayed

Various Interfaces
- 18-/16-/9-/8-bit high-speed parallel bus interfaces including MDT(Multiple Data Transfer) mode.
- serial peripheral interface
- 18-/16-/6-bit RGB interfaces for motion picture display

Various Graphic Operations
- Window-Addressing Function to display motion picture independently of still image display
- Image Rotation / Mirroring Function

Internal RAM capacity: 128 x 18 x 160 = 368,640 bits

Alternating functions for TFT-LCD counter-electrode power

Low-power operation supports
- Power-save functions (standby mode, sleep mode, deep-standby mode)
- Partial display (up to two separated screens) in any position
- Maximum 6-times step-up circuit for generating driving voltage
- Equalizing function for the switching performance of step-up circuits and operational amplifiers

Internal oscillation and external hardware reset
- The S6D0144 can provide R-C oscillation without external resistor.

Internal power supply circuit
- Step-up circuit: four to six times, positive-polarity inversion

Applying voltage
- VDD3 to VSS = 1.65V to 3.3V (I/O operating voltage range)
- VCI to VSS = 2.5V to 3.3V (internal reference power-supply voltage range)
- VDD to VSS = 1.4V to 1.6V (internal regulator only) (internal core operating voltage range)

Generated voltage
- For the source driver : AVDD to VSS = 3.5V to 5.5V (power supply for driving circuits)
  GVDD to VSS = 3.0V to 5.0V (reference power supply for grayscale voltages)
- For the gate driver : VGH to VGL = 14.0V to 30.0V
  VGH to VSS = 7.0V to 16.5V
  VGL to VSS = -13.5V to -7.0V
- For the TFT-LCD counter electrode : Vcom amplitude(max) = 6.0V
  VcomH to VSS (max) = GVDD
  VomL to VSS (max) =1.0V to -VCI1 + 0.5V
- The S6D0144 has various VCOM amplitude adjusting methods. User can select external resistor setting or internal electronic volume setting or MTP programmed setting.

BLOCK DIAGRAM

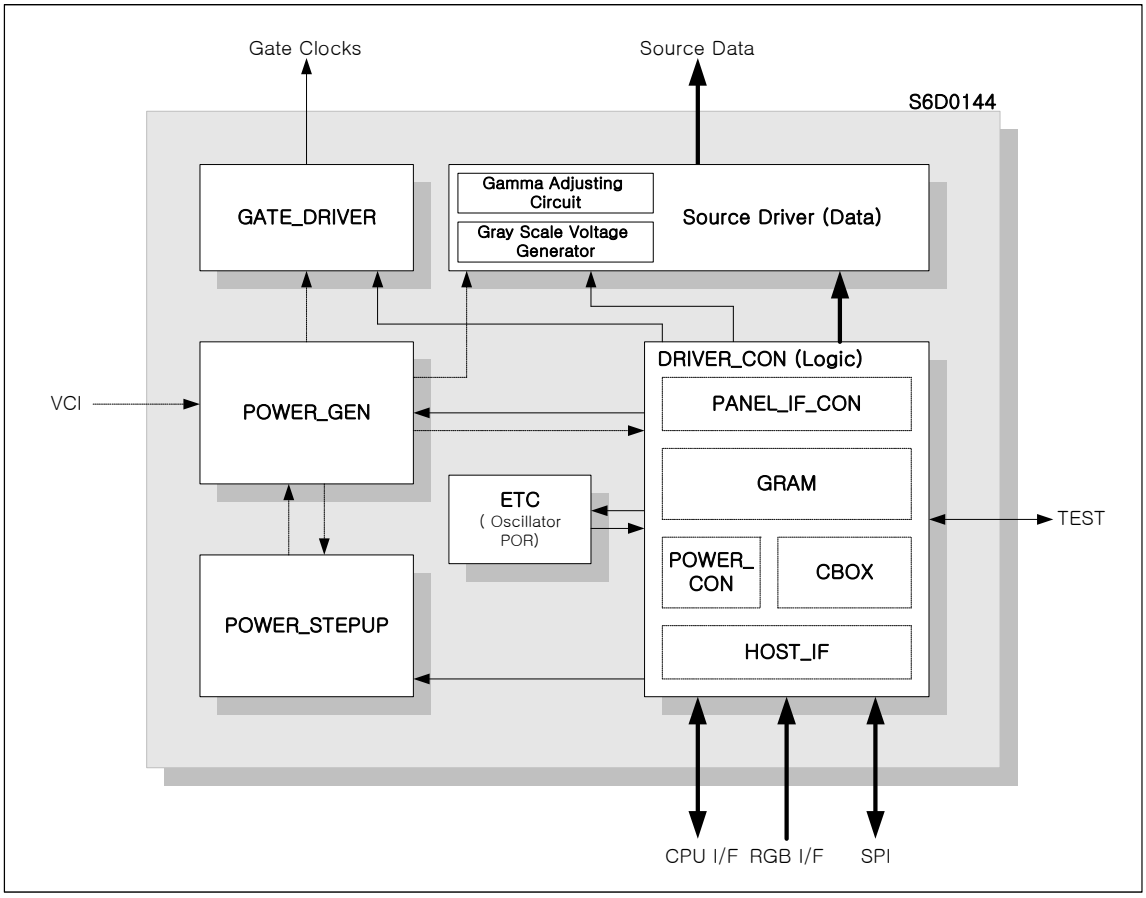


Figure 1 : Block Diagram of S6D0144

PHYSICAL INFORMATION

PAD CONFIGURATION

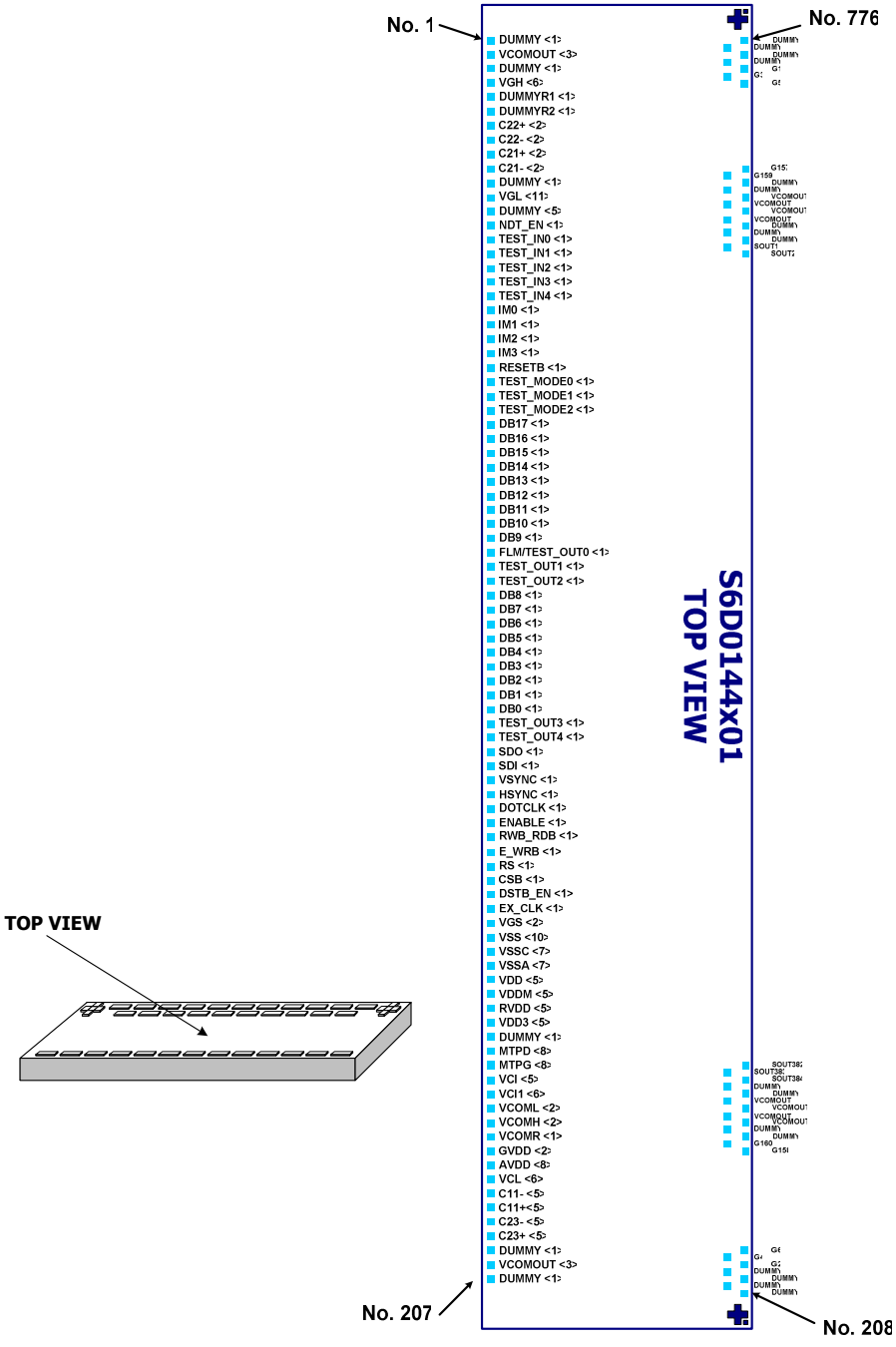
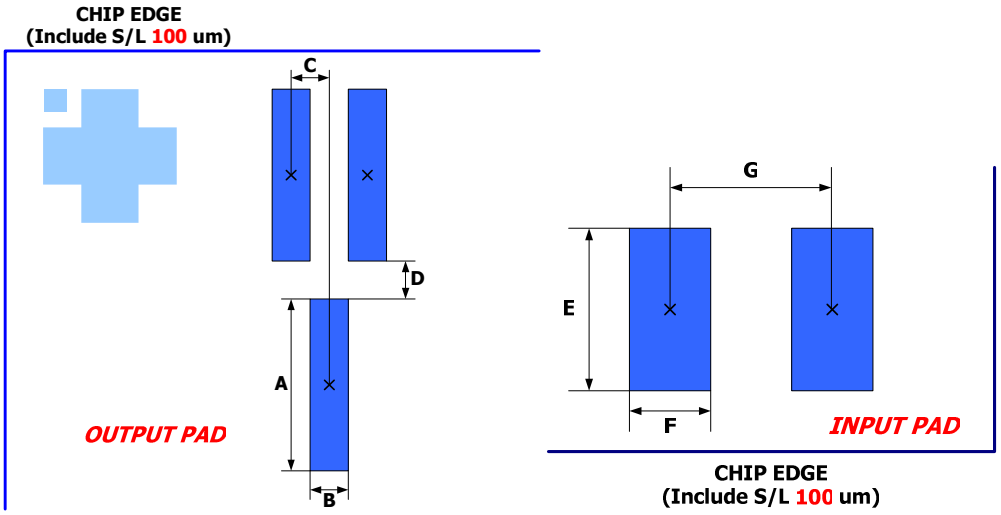


Figure 2 : Pad Configuration

Table 1 : S6D0144 Pad Dimensions

Items	Pad name.		Size	Unit
Chip size[1)]	X		12990	um
	Y		930	
Bump pad size	Input	E	91	
		F	40	
	Output	A	105	
		B	**21**	
Bump to Bump	Output	D	35	
Bump pad pitch	Input	G	60	
	Output	C	22	

[NOTE] Scribe lane included in this chip size (Scribe lane: 100 um)



ALIGN KEY CONFIGURATION

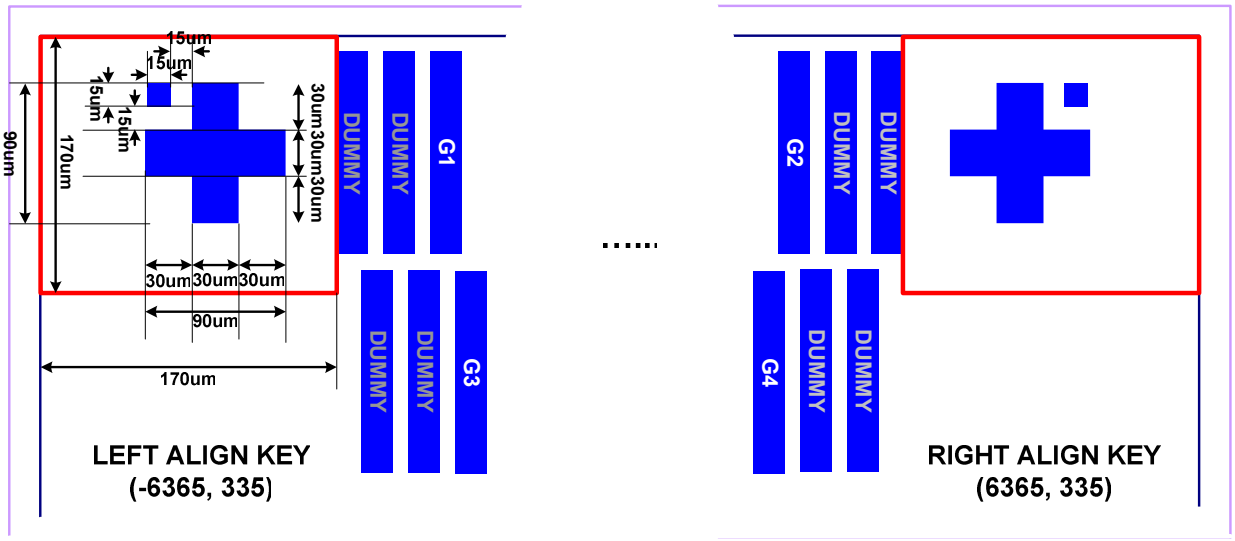


Figure 3 : COG align key

1. Gold bump height : 15 ± 3um (typ.)
2. wafer thickness : 470 um

PAD COORDINATES

Table 2 : Pad Center Coordinates

[Unit : um]

#	X	Y	Name	#	X	Y	Name	#	X	Y	Name
1	-6180	-362.5	DUMMY	51	-3180	-362.5	TEST_MODE1	101	-180	-362.5	VSSC
2	-6120	-362.5	VCOMOUT	52	-3120	-362.5	TEST_MODE2	102	-120	-362.5	VSSC
3	-6060	-362.5	VCOMOUT	53	-3060	-362.5	DB17	103	-60	-362.5	VSSC
4	-6000	-362.5	VCOMOUT	54	-3000	-362.5	DB16	104	0	-362.5	VSSC
5	-5940	-362.5	DUMMY	55	-2940	-362.5	DB15	105	60	-362.5	VSSC
6	-5880	-362.5	VGH	56	-2880	-362.5	DB14	106	120	-362.5	VSSC
7	-5820	-362.5	VGH	57	-2820	-362.5	DB13	107	180	-362.5	VSSA
8	-5760	-362.5	VGH	58	-2760	-362.5	DB12	108	240	-362.5	VSSA
9	-5700	-362.5	VGH	59	-2700	-362.5	DB11	109	300	-362.5	VSSA
10	-5640	-362.5	VGH	60	-2640	-362.5	DB10	110	360	-362.5	VSSA
11	-5580	-362.5	VGH	61	-2580	-362.5	DB9	111	420	-362.5	VSSA
12	-5520	-362.5	DUMMYR1	62	-2520	-362.5	FLM/TEST_OUT0	112	480	-362.5	VSSA
13	-5460	-362.5	DUMMYR2	63	-2460	-362.5	TEST_OUT1	113	540	-362.5	VSSA
14	-5400	-362.5	C22+	64	-2400	-362.5	TEST_OUT2	114	600	-362.5	VDD
15	-5340	-362.5	C22+	65	-2340	-362.5	DB8	115	660	-362.5	VDD
16	-5280	-362.5	C22-	66	-2280	-362.5	DB7	116	720	-362.5	VDD
17	-5220	-362.5	C22-	67	-2220	-362.5	DB6	117	780	-362.5	VDD
18	-5160	-362.5	C21+	68	-2160	-362.5	DB5	118	840	-362.5	VDD
19	-5100	-362.5	C21+	69	-2100	-362.5	DB4	119	900	-362.5	VDDM
20	-5040	-362.5	C21-	70	-2040	-362.5	DB3	120	960	-362.5	VDDM
21	-4980	-362.5	C21-	71	-1980	-362.5	DB2	121	1020	-362.5	VDDM
22	-4920	-362.5	DUMMY	72	-1920	-362.5	DB1	122	1080	-362.5	VDDM
23	-4860	-362.5	VGL	73	-1860	-362.5	DB0	123	1140	-362.5	VDDM
24	-4800	-362.5	VGL	74	-1800	-362.5	TEST_OUT3	124	1200	-362.5	RVDD
25	-4740	-362.5	VGL	75	-1740	-362.5	TEST_OUT4	125	1260	-362.5	RVDD
26	-4680	-362.5	VGL	76	-1680	-362.5	SDO	126	1320	-362.5	RVDD
27	-4620	-362.5	VGL	77	-1620	-362.5	SDI	127	1380	-362.5	RVDD
28	-4560	-362.5	VGL	78	-1560	-362.5	VSYNC	128	1440	-362.5	RVDD
29	-4500	-362.5	VGL	79	-1500	-362.5	HSYNC	129	1500	-362.5	VDD3
30	-4440	-362.5	VGL	80	-1440	-362.5	DOTCLK	130	1560	-362.5	VDD3
31	-4380	-362.5	VGL	81	-1380	-362.5	ENABLE	131	1620	-362.5	VDD3
32	-4320	-362.5	VGL	82	-1320	-362.5	RWB_RDB	132	1680	-362.5	VDD3
33	-4260	-362.5	VGL	83	-1260	-362.5	E_WRB	133	1740	-362.5	VDD3
34	-4200	-362.5	DUMMY	84	-1200	-362.5	RS	134	1800	-362.5	DUMMY
35	-4140	-362.5	DUMMY	85	-1140	-362.5	CSB	135	1860	-362.5	MTPD
36	-4080	-362.5	DUMMY	86	-1080	-362.5	DSTB_EN	136	1920	-362.5	MTPD
37	-4020	-362.5	DUMMY	87	-1020	-362.5	EX_CLK	137	1980	-362.5	MTPD
38	-3960	-362.5	DUMMY	88	-960	-362.5	VGS	138	2040	-362.5	MTPD
39	-3900	-362.5	NDT_EN	89	-900	-362.5	VGS	139	2100	-362.5	MTPD
40	-3840	-362.5	TEST_IN0	90	-840	-362.5	VSS	140	2160	-362.5	MTPD
41	-3780	-362.5	TEST_IN1	91	-780	-362.5	VSS	141	2220	-362.5	MTPD
42	-3720	-362.5	TEST_IN2	92	-720	-362.5	VSS	142	2280	-362.5	MTPD
43	-3660	-362.5	TEST_IN3	93	-660	-362.5	VSS	143	2340	-362.5	MTPG
44	-3600	-362.5	TEST_IN4	94	-600	-362.5	VSS	144	2400	-362.5	MTPG
45	-3540	-362.5	IM0	95	-540	-362.5	VSS	145	2460	-362.5	MTPG
46	-3480	-362.5	IM1	96	-480	-362.5	VSS	146	2520	-362.5	MTPG
47	-3420	-362.5	IM2	97	-420	-362.5	VSS	147	2580	-362.5	MTPG
48	-3360	-362.5	IM3	98	-360	-362.5	VSS	148	2640	-362.5	MTPG
49	-3300	-362.5	RESETB	99	-300	-362.5	VSS	149	2700	-362.5	MTPG
50	-3240	-362.5	TEST_MODE0	100	-240	-362.5	VSSC	150	2760	-362.5	MTPG

Table 3 : Pad Center Coordinates

[Unit : um]

#	X	Y	Name
151	2820	-362.5	VCI
152	2880	-362.5	VCI
153	2940	-362.5	VCI
154	3000	-362.5	VCI
155	3060	-362.5	VCI
156	3120	-362.5	VCI1
157	3180	-362.5	VCI1
158	3240	-362.5	VCI1
159	3300	-362.5	VCI1
160	3360	-362.5	VCI1
161	3420	-362.5	VCI1
162	3480	-362.5	VCOML
163	3540	-362.5	VCOML
164	3600	-362.5	VCOMH
165	3660	-362.5	VCOMH
166	3720	-362.5	VCOMR
167	3780	-362.5	GVDD
168	3840	-362.5	GVDD
169	3900	-362.5	AVDD
170	3960	-362.5	AVDD
171	4020	-362.5	AVDD
172	4080	-362.5	AVDD
173	4140	-362.5	AVDD
174	4200	-362.5	AVDD
175	4260	-362.5	AVDD
176	4320	-362.5	AVDD
177	4380	-362.5	VCL
178	4440	-362.5	VCL
179	4500	-362.5	VCL
180	4560	-362.5	VCL
181	4620	-362.5	VCL
182	4680	-362.5	VCL
183	4740	-362.5	C11-
184	4800	-362.5	C11-
185	4860	-362.5	C11-
186	4920	-362.5	C11-
187	4980	-362.5	C11-
188	5040	-362.5	C11+
189	5100	-362.5	C11+
190	5160	-362.5	C11+
191	5220	-362.5	C11+
192	5280	-362.5	C11+
193	5340	-362.5	C23-
194	5400	-362.5	C23-
195	5460	-362.5	C23-
196	5520	-362.5	C23-
197	5580	-362.5	C23-
198	5640	-362.5	C23+
199	5700	-362.5	C23+
200	5760	-362.5	C23+
201	5820	-362.5	C23+
202	5880	-362.5	C23+
203	5940	-362.5	DUMMY
204	6000	-362.5	VCOMOUT
205	6060	-362.5	VCOMOUT
206	6120	-362.5	VCOMOUT
207	6180	-362.5	DUMMY
208	6248	355.5	DUMMY
209	6226	215.5	DUMMY
210	6204	355.5	DUMMY
211	6182	215.5	DUMMY
212	6160	355.5	G2
213	6138	215.5	G4
214	6116	355.5	G6
215	6094	215.5	G8
216	6072	355.5	G10
217	6050	215.5	G12
218	6028	355.5	G14
219	6006	215.5	G16
220	5984	355.5	G18
221	5962	215.5	G20
222	5940	355.5	G22
223	5918	215.5	G24
224	5896	355.5	G26
225	5874	215.5	G28
226	5852	355.5	G30
227	5830	215.5	G32
228	5808	355.5	G34
229	5786	215.5	G36
230	5764	355.5	G38
231	5742	215.5	G40
232	5720	355.5	G42
233	5698	215.5	G44
234	5676	355.5	G46
235	5654	215.5	G48
236	5632	355.5	G50
237	5610	215.5	G52
238	5588	355.5	G54
239	5566	215.5	G56
240	5544	355.5	G58
241	5522	215.5	G60
242	5500	355.5	G62
243	5478	215.5	G64
244	5456	355.5	G66
245	5434	215.5	G68
246	5412	355.5	G70
247	5390	215.5	G72
248	5368	355.5	G74
249	5346	215.5	G76
250	5324	355.5	G78
251	5302	215.5	G80
252	5280	355.5	G82
253	5258	215.5	G84
254	5236	355.5	G86
255	5214	215.5	G88
256	5192	355.5	G90
257	5170	215.5	G92
258	5148	355.5	G94
259	5126	215.5	G96
260	5104	355.5	G98
261	5082	215.5	G100
262	5060	355.5	G102
263	5038	215.5	G104
264	5016	355.5	G106
265	4994	215.5	G108
266	4972	355.5	G110
267	4950	215.5	G112
268	4928	355.5	G114
269	4906	215.5	G116
270	4884	355.5	G118
271	4862	215.5	G120
272	4840	355.5	G122
273	4818	215.5	G124
274	4796	355.5	G126
275	4774	215.5	G128
276	4752	355.5	G130
277	4730	215.5	G132
278	4708	355.5	G134
279	4686	215.5	G136
280	4664	355.5	G138
281	4642	215.5	G140
282	4620	355.5	G142
283	4598	215.5	G144
284	4576	355.5	G146
285	4554	215.5	G148
286	4532	355.5	G150
287	4510	215.5	G152
288	4488	355.5	G154
289	4466	215.5	G156
290	4444	355.5	G158
291	4422	215.5	G160
292	4400	355.5	DUMMY
293	4378	215.5	DUMMY
294	4356	355.5	VCOMOUT
295	4334	215.5	VCOMOUT
296	4312	355.5	VCOMOUT
297	4290	215.5	VCOMOUT
298	4268	355.5	DUMMY
299	4246	215.5	DUMMY
300	4224	355.5	SOUT384

Table 4 : Pad Center Coordinates

[Unit : um]

#	X	Y	Name
301	4202	215.5	SOUT383
302	4180	355.5	SOUT382
303	4158	215.5	SOUT381
304	4136	355.5	SOUT380
305	4114	215.5	SOUT379
306	4092	355.5	SOUT378
307	4070	215.5	SOUT377
308	4048	355.5	SOUT376
309	4026	215.5	SOUT375
310	4004	355.5	SOUT374
311	3982	215.5	SOUT373
312	3960	355.5	SOUT372
313	3938	215.5	SOUT371
314	3916	355.5	SOUT370
315	3894	215.5	SOUT369
316	3872	355.5	SOUT368
317	3850	215.5	SOUT367
318	3828	355.5	SOUT366
319	3806	215.5	SOUT365
320	3784	355.5	SOUT364
321	3762	215.5	SOUT363
322	3740	355.5	SOUT362
323	3718	215.5	SOUT361
324	3696	355.5	SOUT360
325	3674	215.5	SOUT359
326	3652	355.5	SOUT358
327	3630	215.5	SOUT357
328	3608	355.5	SOUT356
329	3586	215.5	SOUT355
330	3564	355.5	SOUT354
331	3542	215.5	SOUT353
332	3520	355.5	SOUT352
333	3498	215.5	SOUT351
334	3476	355.5	SOUT350
335	3454	215.5	SOUT349
336	3432	355.5	SOUT348
337	3410	215.5	SOUT347
338	3388	355.5	SOUT346
339	3366	215.5	SOUT345
340	3344	355.5	SOUT344
341	3322	215.5	SOUT343
342	3300	355.5	SOUT342
343	3278	215.5	SOUT341
344	3256	355.5	SOUT340
345	3234	215.5	SOUT339
346	3212	355.5	SOUT338
347	3190	215.5	SOUT337
348	3168	355.5	SOUT336
349	3146	215.5	SOUT335
350	3124	355.5	SOUT334
351	3102	215.5	SOUT333
352	3080	355.5	SOUT332
353	3058	215.5	SOUT331
354	3036	355.5	SOUT330
355	3014	215.5	SOUT329
356	2992	355.5	SOUT328
357	2970	215.5	SOUT327
358	2948	355.5	SOUT326
359	2926	215.5	SOUT325
360	2904	355.5	SOUT324
361	2882	215.5	SOUT323
362	2860	355.5	SOUT322
363	2838	215.5	SOUT321
364	2816	355.5	SOUT320
365	2794	215.5	SOUT319
366	2772	355.5	SOUT318
367	2750	215.5	SOUT317
368	2728	355.5	SOUT316
369	2706	215.5	SOUT315
370	2684	355.5	SOUT314
371	2662	215.5	SOUT313
372	2640	355.5	SOUT312
373	2618	215.5	SOUT311
374	2596	355.5	SOUT310
375	2574	215.5	SOUT309
376	2552	355.5	SOUT308
377	2530	215.5	SOUT307
378	2508	355.5	SOUT306
379	2486	215.5	SOUT305
380	2464	355.5	SOUT304
381	2442	215.5	SOUT303
382	2420	355.5	SOUT302
383	2398	215.5	SOUT301
384	2376	355.5	SOUT300
385	2354	215.5	SOUT299
386	2332	355.5	SOUT298
387	2310	215.5	SOUT297
388	2288	355.5	SOUT296
389	2266	215.5	SOUT295
390	2244	355.5	SOUT294
391	2222	215.5	SOUT293
392	2200	355.5	SOUT292
393	2178	215.5	SOUT291
394	2156	355.5	SOUT290
395	2134	215.5	SOUT289
396	2112	355.5	SOUT288
397	2090	215.5	SOUT287
398	2068	355.5	SOUT286
399	2046	215.5	SOUT285
400	2024	355.5	SOUT284
401	2002	215.5	SOUT283
402	1980	355.5	SOUT282
403	1958	215.5	SOUT281
404	1936	355.5	SOUT280
405	1914	215.5	SOUT279
406	1892	355.5	SOUT278
407	1870	215.5	SOUT277
408	1848	355.5	SOUT276
409	1826	215.5	SOUT275
410	1804	355.5	SOUT274
411	1782	215.5	SOUT273
412	1760	355.5	SOUT272
413	1738	215.5	SOUT271
414	1716	355.5	SOUT270
415	1694	215.5	SOUT269
416	1672	355.5	SOUT268
417	1650	215.5	SOUT267
418	1628	355.5	SOUT266
419	1606	215.5	SOUT265
420	1584	355.5	SOUT264
421	1562	215.5	SOUT263
422	1540	355.5	SOUT262
423	1518	215.5	SOUT261
424	1496	355.5	SOUT260
425	1474	215.5	SOUT259
426	1452	355.5	SOUT258
427	1430	215.5	SOUT257
428	1408	355.5	SOUT256
429	1386	215.5	SOUT255
430	1364	355.5	SOUT254
431	1342	215.5	SOUT253
432	1320	355.5	SOUT252
433	1298	215.5	SOUT251
434	1276	355.5	SOUT250
435	1254	215.5	SOUT249
436	1232	355.5	SOUT248
437	1210	215.5	SOUT247
438	1188	355.5	SOUT246
439	1166	215.5	SOUT245
440	1144	355.5	SOUT244
441	1122	215.5	SOUT243
442	1100	355.5	SOUT242
443	1078	215.5	SOUT241
444	1056	355.5	SOUT240
445	1034	215.5	SOUT239
446	1012	355.5	SOUT238
447	990	215.5	SOUT237
448	968	355.5	SOUT236
449	946	215.5	SOUT235
450	924	355.5	SOUT234

Table 5 : Pad Center Coordinates

[Unit : um]

#	X	Y	Name
451	902	215.5	SOUT233
452	880	355.5	SOUT232
453	858	215.5	SOUT231
454	836	355.5	SOUT230
455	814	215.5	SOUT229
456	792	355.5	SOUT228
457	770	215.5	SOUT227
458	748	355.5	SOUT226
459	726	215.5	SOUT225
460	704	355.5	SOUT224
461	682	215.5	SOUT223
462	660	355.5	SOUT222
463	638	215.5	SOUT221
464	616	355.5	SOUT220
465	594	215.5	SOUT219
466	572	355.5	SOUT218
467	550	215.5	SOUT217
468	528	355.5	SOUT216
469	506	215.5	SOUT215
470	484	355.5	SOUT214
471	462	215.5	SOUT213
472	440	355.5	SOUT212
473	418	215.5	SOUT211
474	396	355.5	SOUT210
475	374	215.5	SOUT209
476	352	355.5	SOUT208
477	330	215.5	SOUT207
478	308	355.5	SOUT206
479	286	215.5	SOUT205
480	264	355.5	SOUT204
481	242	215.5	SOUT203
482	220	355.5	SOUT202
483	198	215.5	SOUT201
484	176	355.5	SOUT200
485	154	215.5	SOUT199
486	132	355.5	SOUT198
487	110	215.5	SOUT197
488	88	355.5	SOUT196
489	66	215.5	SOUT195
490	44	355.5	SOUT194
491	22	215.5	SOUT193
492	0	355.5	SOUT192
493	-22	215.5	SOUT191
494	-44	355.5	SOUT190
495	-66	215.5	SOUT189
496	-88	355.5	SOUT188
497	-110	215.5	SOUT187
498	-132	355.5	SOUT186
499	-154	215.5	SOUT185
500	-176	355.5	SOUT184
501	-198	215.5	SOUT183
502	-220	355.5	SOUT182
503	-242	215.5	SOUT181
504	-264	355.5	SOUT180
505	-286	215.5	SOUT179
506	-308	355.5	SOUT178
507	-330	215.5	SOUT177
508	-352	355.5	SOUT176
509	-374	215.5	SOUT175
510	-396	355.5	SOUT174
511	-418	215.5	SOUT173
512	-440	355.5	SOUT172
513	-462	215.5	SOUT171
514	-484	355.5	SOUT170
515	-506	215.5	SOUT169
516	-528	355.5	SOUT168
517	-550	215.5	SOUT167
518	-572	355.5	SOUT166
519	-594	215.5	SOUT165
520	-616	355.5	SOUT164
521	-638	215.5	SOUT163
522	-660	355.5	SOUT162
523	-682	215.5	SOUT161
524	-704	355.5	SOUT160
525	-726	215.5	SOUT159
526	-748	355.5	SOUT158
527	-770	215.5	SOUT157
528	-792	355.5	SOUT156
529	-814	215.5	SOUT155
530	-836	355.5	SOUT154
531	-858	215.5	SOUT153
532	-880	355.5	SOUT152
533	-902	215.5	SOUT151
534	-924	355.5	SOUT150
535	-946	215.5	SOUT149
536	-968	355.5	SOUT148
537	-990	215.5	SOUT147
538	-1012	355.5	SOUT146
539	-1034	215.5	SOUT145
540	-1056	355.5	SOUT144
541	-1078	215.5	SOUT143
542	-1100	355.5	SOUT142
543	-1122	215.5	SOUT141
544	-1144	355.5	SOUT140
545	-1166	215.5	SOUT139
546	-1188	355.5	SOUT138
547	-1210	215.5	SOUT137
548	-1232	355.5	SOUT136
549	-1254	215.5	SOUT135
550	-1276	355.5	SOUT134
551	-1298	215.5	SOUT133
552	-1320	355.5	SOUT132
553	-1342	215.5	SOUT131
554	-1364	355.5	SOUT130
555	-1386	215.5	SOUT129
556	-1408	355.5	SOUT128
557	-1430	215.5	SOUT127
558	-1452	355.5	SOUT126
559	-1474	215.5	SOUT125
560	-1496	355.5	SOUT124
561	-1518	215.5	SOUT123
562	-1540	355.5	SOUT122
563	-1562	215.5	SOUT121
564	-1584	355.5	SOUT120
565	-1606	215.5	SOUT119
566	-1628	355.5	SOUT118
567	-1650	215.5	SOUT117
568	-1672	355.5	SOUT116
569	-1694	215.5	SOUT115
570	-1716	355.5	SOUT114
571	-1738	215.5	SOUT113
572	-1760	355.5	SOUT112
573	-1782	215.5	SOUT111
574	-1804	355.5	SOUT110
575	-1826	215.5	SOUT109
576	-1848	355.5	SOUT108
577	-1870	215.5	SOUT107
578	-1892	355.5	SOUT106
579	-1914	215.5	SOUT105
580	-1936	355.5	SOUT104
581	-1958	215.5	SOUT103
582	-1980	355.5	SOUT102
583	-2002	215.5	SOUT101
584	-2024	355.5	SOUT100
585	-2046	215.5	SOUT99
586	-2068	355.5	SOUT98
587	-2090	215.5	SOUT97
588	-2112	355.5	SOUT96
589	-2134	215.5	SOUT95
590	-2156	355.5	SOUT94
591	-2178	215.5	SOUT93
592	-2200	355.5	SOUT92
593	-2222	215.5	SOUT91
594	-2244	355.5	SOUT90
595	-2266	215.5	SOUT89
596	-2288	355.5	SOUT88
597	-2310	215.5	SOUT87
598	-2332	355.5	SOUT86
599	-2354	215.5	SOUT85
600	-2376	355.5	SOUT84

Table 6 : Pad Center Coordinates

[Unit : um]

#	X	Y	Name
601	-2398	215.5	SOUT83
602	-2420	355.5	SOUT82
603	-2442	215.5	SOUT81
604	-2464	355.5	SOUT80
605	-2486	215.5	SOUT79
606	-2508	355.5	SOUT78
607	-2530	215.5	SOUT77
608	-2552	355.5	SOUT76
609	-2574	215.5	SOUT75
610	-2596	355.5	SOUT74
611	-2618	215.5	SOUT73
612	-2640	355.5	SOUT72
613	-2662	215.5	SOUT71
614	-2684	355.5	SOUT70
615	-2706	215.5	SOUT69
616	-2728	355.5	SOUT68
617	-2750	215.5	SOUT67
618	-2772	355.5	SOUT66
619	-2794	215.5	SOUT65
620	-2816	355.5	SOUT64
621	-2838	215.5	SOUT63
622	-2860	355.5	SOUT62
623	-2882	215.5	SOUT61
624	-2904	355.5	SOUT60
625	-2926	215.5	SOUT59
626	-2948	355.5	SOUT58
627	-2970	215.5	SOUT57
628	-2992	355.5	SOUT56
629	-3014	215.5	SOUT55
630	-3036	355.5	SOUT54
631	-3058	215.5	SOUT53
632	-3080	355.5	SOUT52
633	-3102	215.5	SOUT51
634	-3124	355.5	SOUT50
635	-3146	215.5	SOUT49
636	-3168	355.5	SOUT48
637	-3190	215.5	SOUT47
638	-3212	355.5	SOUT46
639	-3234	215.5	SOUT45
640	-3256	355.5	SOUT44
641	-3278	215.5	SOUT43
642	-3300	355.5	SOUT42
643	-3322	215.5	SOUT41
644	-3344	355.5	SOUT40
645	-3366	215.5	SOUT39
646	-3388	355.5	SOUT38
647	-3410	215.5	SOUT37
648	-3432	355.5	SOUT36
649	-3454	215.5	SOUT35
650	-3476	355.5	SOUT34
651	-3498	215.5	SOUT33
652	-3520	355.5	SOUT32
653	-3542	215.5	SOUT31
654	-3564	355.5	SOUT30
655	-3586	215.5	SOUT29
656	-3608	355.5	SOUT28
657	-3630	215.5	SOUT27
658	-3652	355.5	SOUT26
659	-3674	215.5	SOUT25
660	-3696	355.5	SOUT24
661	-3718	215.5	SOUT23
662	-3740	355.5	SOUT22
663	-3762	215.5	SOUT21
664	-3784	355.5	SOUT20
665	-3806	215.5	SOUT19
666	-3828	355.5	SOUT18
667	-3850	215.5	SOUT17
668	-3872	355.5	SOUT16
669	-3894	215.5	SOUT15
670	-3916	355.5	SOUT14
671	-3938	215.5	SOUT13
672	-3960	355.5	SOUT12
673	-3982	215.5	SOUT11
674	-4004	355.5	SOUT10
675	-4026	215.5	SOUT9
676	-4048	355.5	SOUT8
677	-4070	215.5	SOUT7
678	-4092	355.5	SOUT6
679	-4114	215.5	SOUT5
680	-4136	355.5	SOUT4
681	-4158	215.5	SOUT3
682	-4180	355.5	SOUT2
683	-4202	215.5	SOUT1
684	-4224	355.5	DUMMY
685	-4246	215.5	DUMMY
686	-4268	355.5	DUMMY
687	-4290	215.5	VCOM_OUT
688	-4312	355.5	VCOM_OUT
689	-4334	215.5	VCOM_OUT
690	-4356	355.5	VCOM_OUT
691	-4378	215.5	DUMMY
692	-4400	355.5	DUMMY
693	-4422	215.5	G159
694	-4444	355.5	G157
695	-4466	215.5	G155
696	-4488	355.5	G153
697	-4510	215.5	G151
698	-4532	355.5	G149
699	-4554	215.5	G147
700	-4576	355.5	G145
701	-4598	215.5	G143
702	-4620	355.5	G141
703	-4642	215.5	G139
704	-4664	355.5	G137
705	-4686	215.5	G135
706	-4708	355.5	G133
707	-4730	215.5	G131
708	-4752	355.5	G129
709	-4774	215.5	G127
710	-4796	355.5	G125
711	-4818	215.5	G123
712	-4840	355.5	G121
713	-4862	215.5	G119
714	-4884	355.5	G117
715	-4906	215.5	G115
716	-4928	355.5	G113
717	-4950	215.5	G111
718	-4972	355.5	G109
719	-4994	215.5	G107
720	-5016	355.5	G105
721	-5038	215.5	G103
722	-5060	355.5	G101
723	-5082	215.5	G99
724	-5104	355.5	G97
725	-5126	215.5	G95
726	-5148	355.5	G93
727	-5170	215.5	G91
728	-5192	355.5	G89
729	-5214	215.5	G87
730	-5236	355.5	G85
731	-5258	215.5	G83
732	-5280	355.5	G81
733	-5302	215.5	G79
734	-5324	355.5	G77
735	-5346	215.5	G75
736	-5368	355.5	G73
737	-5390	215.5	G71
738	-5412	355.5	G69
739	-5434	215.5	G67
740	-5456	355.5	G65
741	-5478	215.5	G63
742	-5500	355.5	G61
743	-5522	215.5	G59
744	-5544	355.5	G57
745	-5566	215.5	G55
746	-5588	355.5	G53
747	-5610	215.5	G51
748	-5632	355.5	G49
749	-5654	215.5	G47
750	-5676	355.5	G45

Table 7 : Pad Center Coordinates

[Unit : um]

#	X	Y	Name
751	-5698	215.5	G43
752	-5720	355.5	G41
753	-5742	215.5	G39
754	-5764	355.5	G37
755	-5786	215.5	G35
756	-5808	355.5	G33
757	-5830	215.5	G31
758	-5852	355.5	G29
759	-5874	215.5	G27
760	-5896	355.5	G25
761	-5918	215.5	G23
762	-5940	355.5	G21
763	-5962	215.5	G19
764	-5984	355.5	G17
765	-6006	215.5	G15
766	-6028	355.5	G13
767	-6050	215.5	G11
768	-6072	355.5	G9
769	-6094	215.5	G7
770	-6116	355.5	G5
771	-6138	215.5	G3
772	-6160	355.5	G1
773	-6182	215.5	DUMMY
774	-6204	355.5	DUMMY
775	-6226	215.5	DUMMY
776	-6248	355.5	DUMMY

PIN DESCRIPTION

Table 8 : Power supply pin description

Symbol	I/O	Description
VDD	O / Power	System power supply. S6D0144 has internal regulator. Regulated mode only : typ. 1.5V (1.4 ~ 1.6 V)
VDDM	I/ Power	System power supply for memory. Connect to VDD
VDD3	I / Power	VDD level for I/O. (VDD3 : 1.65 ~ 3.3V)
AVDD	O / Power	A power output pin for source driver block that is generated from power block. Connect a capacitor for stabilization. (AVDD: 3.5 ~ 5.5V)
GVDD	O / Power	A Standard level for grayscale voltage generator. Connect a capacitor for stabilization.
VCI	I / Power	A power supply for internal reference circuits. Connect VDD3 when VDD3 = 2.5 to 3.3V. Connect a 2.5 to 3.3V external-voltage power supply when VDD3 = 1.65 to 2.5V.
VSS	I / Power	System ground (0V)
VSSC	I / Power	System ground level for step up circuit block.
VSSA	I / Power	System ground level for analog circuit block.
VGS	I / Power	Reference voltage for gamma voltage generator.
VCI1	O/ Power	A reference voltage in step-up circuit 1. Connect a capacitor for stabilization.
VCL	Power	A power supply pin for generating VcomL. When VCL is higher than VSS, VcomL outputs VSS level. Connect a capacitor for stabilization.
VcomOUT	O	A power supply for the TFT-display counter electrode. Connect this pin to the TFT-display counter electrode. This pin is also used as equalizing function: When EQ = “High” period, all source drivers’ outputs are short to VcomOUT level (Hi-z).

Table 9 : Power supply pin description (continued)

Symbol	I/O	Description
VcomR	I	A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between GVDD and VSS. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
VcomH	O	This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization.
VcomL	O	When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
VGH	O/ Power	A positive power output pin for gate driver, internal step-up circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization.
VGL	O/ Power	A Negative power output pin for gate driver, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. When internal VGL generator is not used, connect an external-voltage power supply higher than –13.75 V. To protect IC against Latch up, connect the cathode of the schottky diode to the VSS pad. And the anode of the schottky diode to the VGL pad. Refer to application circuit. Connect a capacitor for stabilization.
C11+,C11-	-	Connect the step-up capacitor for generating the AVDD level.
C22+, C22- C21+, C21-	-	Connect a step-up capacitor for generating the VGL/VGH level.
C23+,C23-	-	Connect a step-up capacitor for generating the VCL level.

Table 10 : System interface pin description

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM[3:0] / ID</td><td>I</td><td>Selects the System interface mode.
<table>
<tr><th>IM[3:0]</th><th>Description</th></tr>
<tr><td>4’b0000</td><td>68-16bit CPU interface</td></tr>
<tr><td>4’b0001</td><td>68-8bit CPU interface</td></tr>
<tr><td>4’b0010</td><td>80-16bit CPU interface</td></tr>
<tr><td>4’b0011</td><td>80-8bit CPU interface</td></tr>
<tr><td>4’b010x</td><td>Serial peripheral interface (SPI)
IM[0] = ID</td></tr>
<tr><td>4’b011x</td><td>Reserved</td></tr>
<tr><td>4’b1000</td><td>68-18bit CPU interface</td></tr>
<tr><td>4’b1001</td><td>68-9bit CPU interface</td></tr>
<tr><td>4’b1010</td><td>80-18bit CPU interface</td></tr>
<tr><td>4’b1011</td><td>80-9bit CPU interface</td></tr>
<tr><td>4’b11xx</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>CSB</td><td>I</td><td>Selects the S6D0144:
- Low: S6D0144 is selected and can be accessed.
- High: S6D0144 is not selected and cannot be accessed.
Must be fixed to VDD3 level when not used.</td></tr>
<tr><td>RS</td><td>I</td><td>Selects the register.
- Low : Index / status
- High : Control
Must be fixed to VDD3 or VSS level when SPI mode.</td></tr>
<tr><td>E_WRB /
SCL</td><td>I</td><td>In 68-system mode, this serves as write/read enable strobe (E).
In 80-system mode, this serves as a write strobe signal (WRB).
In SPI mode, it serves as a synchronous clock (SCL).</td></tr>
<tr><td>RWB_RDB</td><td>I</td><td>In 68-system mode, this is used to select operation, read or write. (RWB)
In 80-system mode, this serves as a read strobe signal. (RDB).
Must be fixed to VDD3 or VSS level when SPI mode.</td></tr>
<tr><td>DB[17:0]
[NOTE]</td><td>I/O</td><td>Data Bus.
<table>
<tr><th colspan="2">Interface Mode</th><th colspan="2">Description</th></tr>
<tr><th>IM[3:0]</th><th></th><th>Index</th><th>Data</th></tr>
<tr><td>4’b0000</td><td>68-16bit CPU interface</td><td>DB[8:1]</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>4’b0001</td><td>68-8bit CPU interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>4’b0010</td><td>80-16bit CPU interface</td><td>DB[8:1]</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>4’b0011</td><td>80-8bit CPU interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr>
<tr><td>4’b010x</td><td>Serial peripheral interface (SPI)</td><td>-</td><td>-</td></tr>
<tr><td>4’b011x</td><td>Reserved</td><td>-</td><td>-</td></tr>
<tr><td>4’b1000</td><td>68-18bit CPU interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>4’b1001</td><td>68-9bit CPU interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>4’b1010</td><td>80-18bit CPU interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr>
<tr><td>4’b1011</td><td>80-9bit CPU interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr>
<tr><td>4’b11xx</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table>
Must be fixed to VDD3 or VSS level when not used.</td></tr>
<tr><td>SDI</td><td>I</td><td>Serial input data. Must be fixed to VDD3 or VSS level when not used.</td></tr>
<tr><td>SDO</td><td>O</td><td>Serial output data. Leave this pin open when not used.</td></tr>
</table>

[NOTE] When used as system interface.

Table 11 : RGB interface pin description (Continued)

Symbol	I/O	Description
ENABLE	I	Data enable signal of RGB interface. When ENABLE is in active state data on RGB bus is valid, but when this is not in active state data on RGB bus is invalid. (For details, refer to the description of EPL register) Must be fixed to VDD3 level when not used.
VSYNC	I	Synchronous signal of frame. (Active Low Pin) Must be fixed to VDD3 or VSS level when not used.
HSYNC	I	Synchronization signal of a horizontal line. (Active Low Pin) Must be fixed to VDD3 or VSS level when not used.
DOTCLK	I	Data Clock of RGB interface. Must be fixed to VDD3 or VSS level when not used.
DB[17:0] **[NOTE]**	I	Serves as an input data bus for RGB I/F. - 6-bit interface: DB[17:12] - 16-bit interface: {DB[17:13], DB[11:1]} - 18-bit interface: DB[17:0] Must be fixed to VDD3 or VSS level when not used.

[NOTE] When used as RGB I/F

Table 12 : Display pin description

Symbol	I/O	Description
S1 - S384	O	Source driver output pins. The SS bit can change the shift direction of the source signal. For example, if SS = 0, gray data of S1 is read from RAM address 0000h. If SS = 1, contents of RAM address 0000h is out from S384. S1, S4, S7, ... S(3n-1) : display Red (R) (SS = 0) S2, S5, S8, ... S(3n-2) : display Green (G) (SS = 0) S3, S6, S9, ... S(3n) : display Blue (B) (SS = 0)
G1 - G160	O	Gate driver output pins. The output of driving circuit is whether VGH or VGL VGH : gate-ON level VGL : gate-OFF level

Table 13 : Oscillator and internal power regulator pin description

Symbol	I/O	Description
MTPD	I	MTP Program pin.16V ~ 16.5V. Leave this pin open when not used.
MTPG	I	MTP Erase initial pin. 19V ~ 19.5V. Leave this pin open when not used.
RESETB	I	Reset pin. Initializes the LSI when low. Must be reset after power-on. Leave this pin open when not used.
DSTB_EN	I	Deep standby mode enable : fix to VDD3 level. Deep standby mode disable : fix to VSS level.
RVDD	O	Internal power regulated-RVDD output (typ. 1.5V). Connect a capacitor for stabilization.

Table 14 : DUMMY pin description

Symbol	I/O	Description
TEST_IN[4:0]	I	Test pin. In normal operation, leave this pin open or fix to VSS level.
TEST_MODE[2:0]	I	Test pin. In normal operation, leave this pin open or fix to VSS level.
FLM/TEST_OUT[0]	O	Frame start signal. Leave this pin open when not used.
TEST_OUT[4:1]	O	Test pin. In normal operation, leave this pin open.
DUMMY	-	Dummy pin. These pins have no connection to the internal circuit.
EX_CLK	I	Test pin. In normal operation, leave this pin open or fix to VDD3 level. (Test Mode : 140kHz ~ 340kHz)
NDT_EN	I	Test signal input pin. In normal operation, leave this pin open or fix to VSS level.
DUMMYR1 DUMMYR2	-	Contact resistance measurement pin. In normal operation, leave this pin open.

FUNCTIONAL DESCRIPTION

SYSTEM INTERFACE

S6D0144 has nine high-speed system interfaces: 80-system 18/16/9/8bit CPU Interfaces, 68-system 18/16/9/8bit CPU Interfaces and a serial peripheral (SPI: Serial Peripheral Interface). The IM[3:0] pin determines the interface mode.

Users may write/read data to/from internal GRAM (Graphics RAM) as well as a lot of internal control registers through these system interfaces.

All instructions except Oscillation Start performed with 0-cycle, so the instructions can be written in succession.

When users want to access the LSI, they must generate control signals as shown below.

Table 15 : Register Selection (80/68-8/9/16/18bit CPU Interface)

E / WRB	RWB / RDB	RS	Operations
1 / 0	0 / 1	0	Write indexes into IR (Index Register).
1 / 1	1 / 0	0	Read internal status.
1 / 0	0 / 1	1	Write into control registers or GRAM.
1 / 1	1 / 0	1	Read data from control registers or GRAM.

Table 16 : Register Selection (Serial Peripheral Interface)

RWB Bit	RS Bit	Operations
0	0	Write indexes into IR (Index Register).
1	0	Read internal status.
0	1	Write into control registers or GRAM.
1	1	Read data from control registers or GRAM.

RGB INTERFACE

S6D0144 has RGB interface for the reproduction of motion picture display. When the RGB interface is used, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for the display operation. The data for display (DB[17:0]) are written according to the values of ENABLE and DOTCLK. This allows flicker-free update of screen.

COMMAND BOX

S6D0144 has a command box to control internal operations and many internal analog blocks including Power Blocks, Source Driver and Gate Driver.

GRAPHICS RAM

The graphics RAM (GRAM) has 18 bits/pixel and stores the bit-pattern data of 128-RGB x 160 pixels.

S6D0144 has an address counter for GRAM access. The address counter (AC) assigns addresses to the GRAM. When an address set instruction is performed, the address from system interface is sent to this AC. After writing into GRAM, the AC is automatically increased (or decremented) by 1. But after reading data from GRAM, the AC is not updated.
Window Address Function allows data to be written only into the Window specified by some control registers.

PANEL INTERFACE CONTROLLER

The Panel Interface Controller generates timing signals for TFT-LCD Driver and control signals for the operation of internal circuits such as source driver and GRAM. The GRAM read operations done by this Panel Interface Controller and GRAM write operations done through system interface are performed independently to avoid the interference between them.

GRAYSCALE VOLTAGE GENERATOR

The grayscale voltage circuit generates a certain voltage level that is specified by the grayscale ϒ-adjusting resistor for LCD driver circuit. By use of the generator, 262,144 colors can be displayed at the same time. For details, see the ϒ-adjusting resistor section.

OSCILLATION CIRCUIT (OSC)

The S6D0144 can provide R-C oscillation without external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the register setting value[R61h]. Clock pulse can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

SOURCE DRIVER CIRCUIT

The liquid crystal display source driver circuit consists of 384 drivers (S1 to S384).
Display pattern data is latched when 384-bit data has arrived. Then the latched data enables the source drivers to output to expected voltage level. The SS bit can change the shift direction of 384-bit data by selecting an appropriate direction for the device-mounted configuration.

GATE DRIVER CIRCUIT

The liquid crystal display gate driver circuit consists of 160 gate drivers (G1 to G160).
The VGH or VGL level is output by the signal from the gate control circuit. G1 and G160 are IC maker's test pins.

GRAM ADDRESS MAP

The image data stored in GRAM corresponds to real pixel on display as shown below.

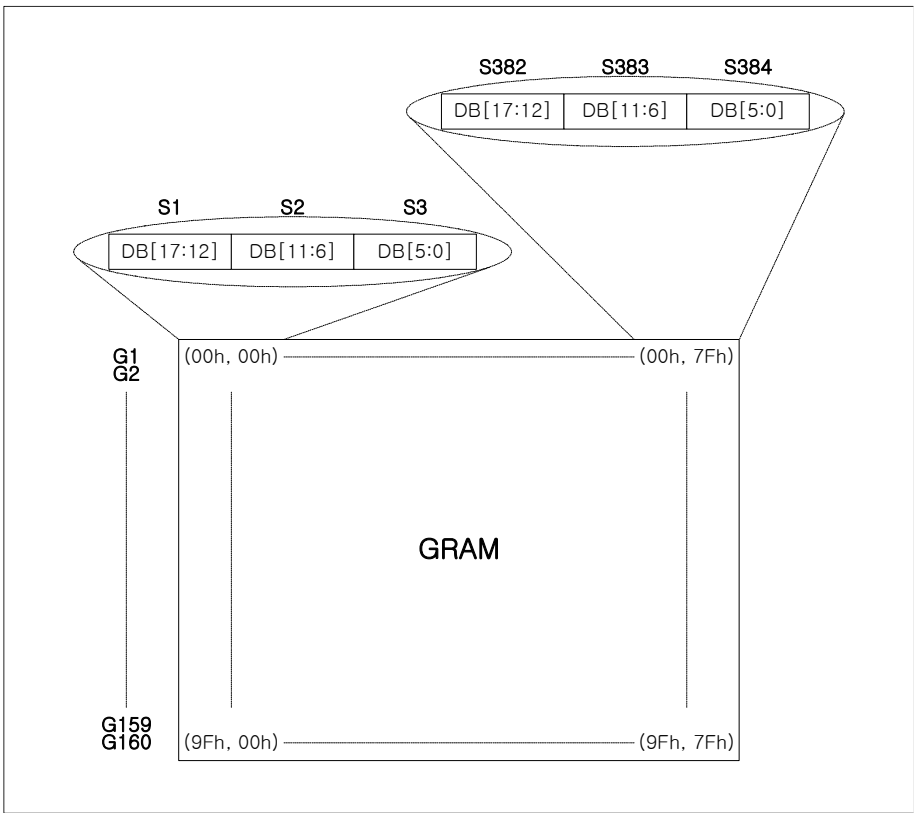


Figure 4 : GRAM Address and Display Image

[NOTE] The display condition of this figure is like this.
SS = 0, BGR = 0, GS = 0.

INSTRUCTIONS

OUTLINE

S6D0144 uses 18bit bus architecture. To execute an instruction of the S6D0144, control information from external 18/16/9/8bit data is stored in Index Register (IR) and Control Register (CR) as described later to allow high-speed interface to high-performance microcomputer.

The internal operation of S6D0144 is determined by the signals sent from microcomputer. These signals, which include the register selection signal (RS), the write/read signals (E/RWB for 68-system, WRB/RDB for 80-system), and the internal 16-bit data bus signals (IB15 to IB0), make up S6D0144 instructions.

There are eight categories of instructions that

- Specifies the index
- Reads the status
- Controls the display
- Controls power management
- Processes the graphics data
- Sets internal GRAM addresses
- Transfers data to and from the internal GRAM
- Sets grayscale level for the internal grayscale palette table

Normally, instructions writing data are used the most frequently. So, the automatic update of internal GRAM address after each data write can lighten the microcomputer's load. Because instructions are executed in 0 cycles, they can be written in succession.

The 16bit instruction assignment varies with interface mode specified by IM. And you can see the assignment for each interface mode in SYSTEM INTERFACE section described later.

INSTRUCTION TABLE

Table 17 : Instruction table 1

Reg.No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Register Name / Description
IR	W	0	X	X	X	X	X	X	X	X	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	**Status read /** Reads the internal status of the S6D0144
R00h	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	**Start Oscillation(R00H) /** Starts/Stops the oscillation circuit
	R	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	**Device code read /** Read 0144H
R01h	W	1	X	X	X	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)	X	X	X	NL4 (1)	NL3 (0)	NL2 (1)	NL1 (0)	NL0 (0)	**Driver output control(R01H) /** DPL: set polarity of DOTCLK pin while using RGB interface. EPL: set polarity of ENABLE pin while using RGB interface. SM: gate driver division drive control GS: gate driver shift direction SS: source driver shift direction NL4-0: number of driving lines
R02h	W	1	X	X	X	X	X	X	FL1 (0)	FL0 (0)	X	X	X	FLD (0)	X	X	X	X	**LCD-Driving-waveform control (R02H)/** FL1-0 : Line/Frame inversion setting FLD : Interlace Mode Control
R03h	W	1	X	X	X	BGR (0)	X	X	MDT1 (0)	MDT0 (0)	X	X	I/D1 (1)	I/D0 (1)	AM (0)	X	X	X	**Entry mode(R03H) /** BGR: RGB swap control MDT2-1: Multiple Data Transfer I/D1-0: address counter Increment / Decrement control AM: horizontal / vertical RAM update
R07h	W	1	X	X	X	PT1 (0)	PT0 (0)	X	X	SPT (0)	X	X	GON (0)	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	**Display control (R07H) /** PT1-0: Non-display area source output control SPT: 1st/2nd partial display enable GON: gate-off to be VSS level DTE:DISPTMG to be VSS level CL: 8-color display mode enable REV: display area inversion drive D1-0: source output control
R08h	W	1	X	X	X	X	FP3 (0)	FP2 (0)	FP1 (1)	FP0 (0)	X	X	X	X	BP3 (0)	BP2 (0)	BP1 (1)	BP0 (0)	**Blank period control 1 (R08H)/** BP3-0: Back porch setting FP3-0: Front porch setting
R0Bh	W	1	X	X	X	X	X	X	DIV1 (0)	DIV0 (0)	X	X	X	X	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	**Frame cycle control (R0BH)/** DIV1-0: division ratio of internal clock setting RTN3-0: set the 1-H period
R0Ch	W	1	X	X	X	X	X	X	X	RM (0)	X	X	DM1 (0)	DM0 (0)	X	X	RIM1 (0)	RIM0 (0)	**External interface control(R0CH) /** RM: specify the interface for RAM access DM1-0: specify display operation mode RIM1-0: specify RGB-I/F mode
R10h	W	1	DSTB (0)	X	SAP2 (0)	SAP1 (0)	SAP0 (0)	BT2 (0)	BT1 (0)	BT0 (0)	DC2 (0)	DC1 (0)	DC0 (0)	AP2 (0)	AP1 (0)	AP0 (0)	SLP (0)	STB (0)	**Power control 1 (R10H) /** SAP2-0: Adjust the amount of fixed current in the op Amp for the source driver BT2-0: Adjust scale factor of the step-up DC2-0: Select operating frequency in the step-up circuit AP2-0: Adjust the amount of fixed current in the op Amp for the power supply SLP: enters the sleep mode STB: enters the standby mode DSTB : enters the deep standby mode.
R11h	W	1	VR1C (0)	X	X	VRN14 (0)	VRN13 (0)	VRN12 (0)	VRN11 (0)	VRN10 (0)	X	X	X	VRP14 (0)	VRP13 (0)	VRP12 (0)	VRP11 (0)	VRP10 (0)	**Gamma control 1 (R11H)/** VR1C : Control step of amplitude positive and negative of 64-grayscale VRN14-10: Control amplitude (positive polarity) of 64-grayscale. VRP14-10: Control amplitude (negative polarity) of 64-grayscale.
R12h	W	1	X	X	X	X	X	X	X	X	SVC3 (0)	SVC2 (0)	SVC1 (0)	SVC0 (0)	X	VC2 (0)	VC1 (0)	VC0 (0)	**Power control 2 /** **SVC3-0:**set VCI1 voltage VC2-0: set reference voltage of VREFS
R13h	W	1	X	X	X	X	VCMR (1)	X	X	X	X	X	X	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	**Power control 3 /** VCMR : select VCOMH voltage adjusting method PON : Power circuit ON/OFF setting VRH3-0 : Set GVDD voltage
R14h	W	1	X	VDV6 (0)	VDV5 (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	VCOMG (0)	VCM6 (0)	VCM5 (0)	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	**Power control 4 /** VCOMG : VCOML voltage level negative voltage setting VDV6-0 : COM output amplitude setting VCM6-0 : VCOMH voltage level setting
R21h	W	1	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	**RAM address register /** AD15-AD0
R22h	W	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	**Write data to GRAM /** WD15-WD0
	R	1	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	**Read data from GRAM /** RD15-RD0
R30h	W	1	X	X	X	X	X	PKP12 (0)	PKP11 (0)	PKP10 (0)	X	X	X	X	X	PKP02 (0)	PKP01 (0)	PKP00 (0)	**Gamma control 2/** PKP12-10, PKP02-00: Micro adjustment setting
R31h	W	1	X	X	X	X	X	PKP32 (0)	PKP31 (0)	PKP30 (0)	X	X	X	X	X	PKP22 (0)	PKP21 (0)	PKP20 (0)	**Gamma control 2/** PKP32-30, PKP22-20: Micro adjustment setting
R32h	W	1	X	X	X	X	X	PKP52 (0)	PKP51 (0)	PKP50 (0)	X	X	X	X	X	PKP42 (0)	PKP41 (0)	PKP40 (0)	**Gamma control 2/** PKP52-50, PKP42-40: Micro adjustment setting
R33h	W	1	X	X	X	X	X	PRP12 (0)	PRP11 (0)	PRP10 (0)	X	X	X	X	X	PRP02 (0)	PRP01 (0)	PRP00 (0)	**Gamma control 2/** PRP12-10, PRP02-00: Gradient adjustment setting
R34h	W	1	X	X	X	X	X	PKN12 (0)	PKN11 (0)	PKN10 (0)	X	X	X	X	X	PKN02 (0)	PKN01 (0)	PKN00 (0)	**Gamma control 2/** PKN12-10, PKN2-0: Micro adjustment setting
R35h	W	1	X	X	X	X	X	PKN32 (0)	PKN31 (0)	PKN30 (0)	X	X	X	X	X	PKN22 (0)	PKN21 (0)	PKN20 (0)	**Gamma control 2/** PKN32-30, PKN22-20: Micro adjustment setting
R36h	W	1	X	X	X	X	X	PKN52 (0)	PKN51 (0)	PKN50 (0)	X	X	X	X	X	PKN42 (0)	PKN41 (0)	PKN40 (0)	**Gamma control 2/** PKN52-50, PKN42-40: Micro adjustment setting
R37h	W	1	X	X	X	X	X	PRN12 (0)	PRN11 (0)	PRN10 (0)	X	X	X	X	X	PRN02 (0)	PRN01 (0)	PRN00 (0)	**Gamma control 2/** PRN12-10, PRN02-00: Gradient adjustment setting
R38h	W	1	X	X	X	X	VRN03 (0)	VRN02 (0)	VRN01 (0)	VRN00 (0)	X	X	X	X	VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)	**Gamma control 3/** VRN03-00 : gamma amplitude setting(negative polarity) VRP03-00 : gamma amplitude setting(positive polarity)
R40h	W	1	X	X	X	X	X	X	X	X	X	X	X	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	**Gate Scan Position /** SCN4-0 : scan starting position of gate
R42h	W	1	SE17 (1)	SE16 (0)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	**1st screen driving position/** SE17-10 : 1st screen end position setting SS17-10 : 1st screen start position setting
R43h	W	1	SE27 (1)	SE26 (0)	SE25 (0)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	**2nd screen driving position/** SE27-20 : 2nd screen end position setting SS27-20 : 2nd screen start position setting
R44h	W	1	HEA7 (0)	HEA6 (1)	HEA5 (1)	HEA4 (1)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	**Horizontal window address/** HEA7-0 : Horizontal window address end position HSA7-0 : Horizontal window address start position
R45h	W	1	VEA7 (1)	VEA6 (0)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	**Vertical window address/** VEA7-0 : Vertical window address end position VSA7-0 : Vertical window address start position

Table 18 : Instruction table 2

Reg.No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	Register Name / Description
R61h	W	1	X	X	X	X	X	X	X	X (0)	X	X	X	RADJ4 (1)	RADJ3 (1)	RADJ2 (0)	RADJ1 (0)	RADJ0 (0)	Sets internal oscillator oscillation frequency (RADJ4-0)
R69h	W	1	X	X	X	X	X	X	X	X	X	X	X	NLDC3 (0)	NLDC2 (1)	NLDC1 (1)	NLDC0 (0)	NLPM (0)	**Low power mode (LPM) setting register** Sets Low power mode (NLPM) Sets DC/DC converter clock for AVDD at LPM (NLDC1-0) Sets DC/DC converter clock for VGH/L at LPM (NLDC3-2) Select capability of DC/DC converter for VGH/L (NLPDC)
R70h	W	1	X	X	X	X	X	X	X	X	SDT1 (0)	SDT0 (0)	X	X	X	X	EQ1 (0)	EQ0 (0)	**Sets source output pre-driving period** Specifies equalize period (EQ 1-0) Specifies source output delay term (SDT1-0)
R71h	W	1	X	X	X	X	GNO1 (0)	GNO0 (0)	X	X	X	X	X	X	X	X	X	X	**Sets the amount of non-overlap period of gate outputs**
R72h	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SR(1)	Software Reset Control
R73h	W	1	X	X	X	X	X	X	X	X	TEST_ KEY7 (0)	TEST_ KEY6 (0)	TEST_ KEY5 (0)	TEST_ KEY4 (0)	TEST_ KEY3 (0)	TEST_ KEY2 (0)	TEST_ KEY1 (0)	TEST_ KEY0 (0)	Test Key to update MTP Value. 'hA5 should be written to do it.
RB3h	W	1	X	X (0)	X (0)	X (0)	X	X (0)	X (1)	X (0)	X	X	X	DCR_ EX (0)	X	X	X	X (0)	**DCR_EX** Select Source of Pumping Clock
RB4h	W	1	X	X	X	MTP_ SEL (1)	X	X	X	MTP_ INIT (0)	X	X	X	MTP_ WRB (1)	X	X	X	MTP_ LOAD (0)	**MTP Control Registers**
RBDh	R/W	1	X	X	X	X	X	X	X	DISEN (0)	X	MTP_ DOUT6	MTP_ DOUT5	MTP_ DOUT4	MTP_ DOUT3	MTP_ DOUT2	MTP_ DOUT1	MTP_ DOUT0	**DISEN : VGL/VCL Discharge Enable** **MTP Read Registers.**
RBEh	W	1	X	X	X	X	X	X	X	X	X	X	X	IM_SEL	IM_3	X	X	X	**Interface mode selection**

INSTRUNCTION DESCRIPTIONS

INDEX REGISTER (IR)

The index instruction specifies indexes. It can set the register number in the range of 00000000b to 10111101b in binary form. However, do not access index registers and instruction bits those are not allocated in this document.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

STATUS READ

The status read instruction allows read operation of the internal status of S6D0144. The status indicates the position of horizontal line currently being driven.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

SYSTEM CONTROL (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
R	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0

Issuing this instruction forces the internal oscillator to start oscillation.
It can be used to restart the internal oscillator from the halt state in standby mode.
After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction.
(See the Standby Mode section.)

If this register (00h) is read forcibly, “0144h” is read.

DRIVER OUTPUT CONTROL (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	DPL	EPL	SM	GS	SS	X	X	X	NL4	NL3	NL2	NL1	NL0

DPL

Determine the active polarity of DOTCLK for using RGB interface.

Table 19 : DPL and DOTCLK polarity

DPL	DOTCLK	Description
0 (1)	↑ (↓)	Valid (Valid)
0 (1)	↓ (↑)	Invalid (Invalid)

EPL

Determine the active polarity of ENABLE for using RGB interface.

Table 20 : EPL, ENABLE and RAM access

EPL	ENABLE	RAM Write	RAM Address
0 (1)	0 (1)	Valid (Valid)	Updated (Updated)
0 (1)	1 (0)	Invalid (Invalid)	Hold (Hold)

SM

Select the division drive method of the gate driver. When SM = 0, even/odd division is selected; SM = 1, upper/lower division drive is selected. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

GS

Set the order of Gate Clock generation. When GS = 0, G1 is output first and G160 is finally output. When GS = 1, G160 is output first and G1 is finally output (NL = 5'b10100). But in case of NL = 5'b00001, when GS = 0, G1 is output first and G8 is finally output, and when GS = 1, G8 is output first and G1 is finally output

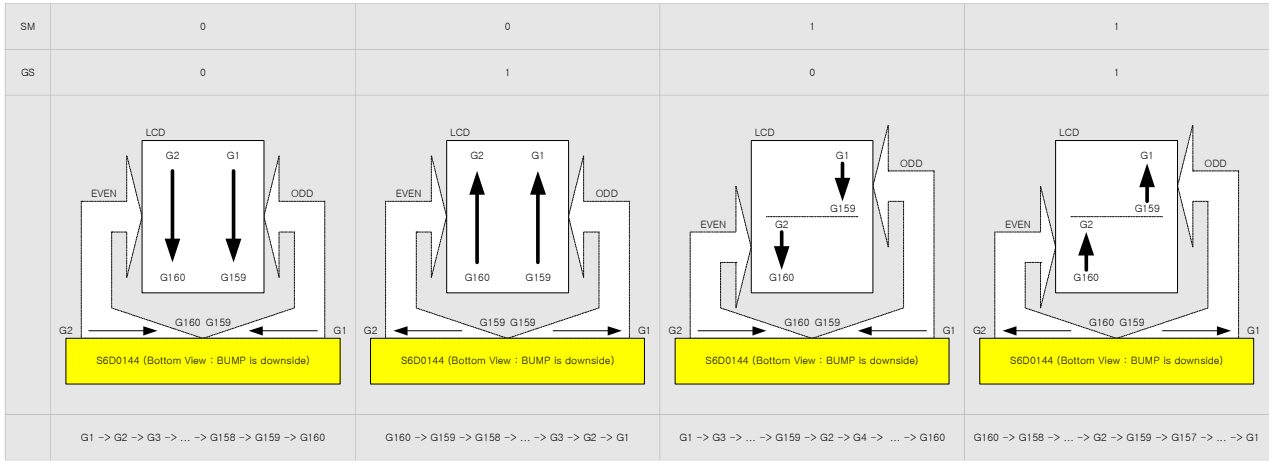


Figure 5 : Gate Clock Generation order selection using GS and SM (NL = 5'b10100, SCN = 5'b00000)

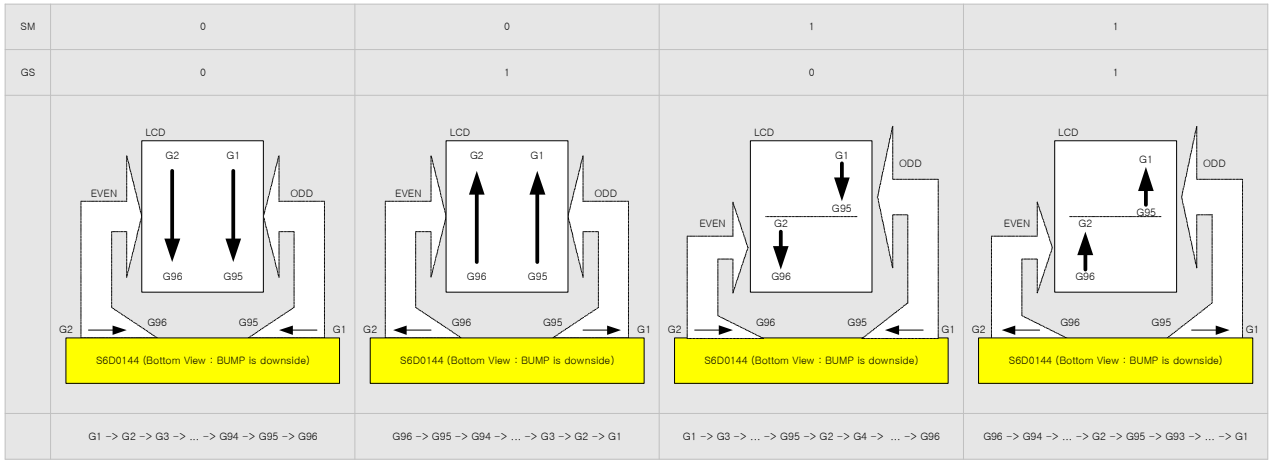


Figure 6 : Gate Clock Generation order selection using GS and SM (NL = 5'b01100, SCN = 5'b00000)

SS

Select the direction of the source driver channel in pixel unit.
When user changes the value of SS, memory should be updated to apply the change.

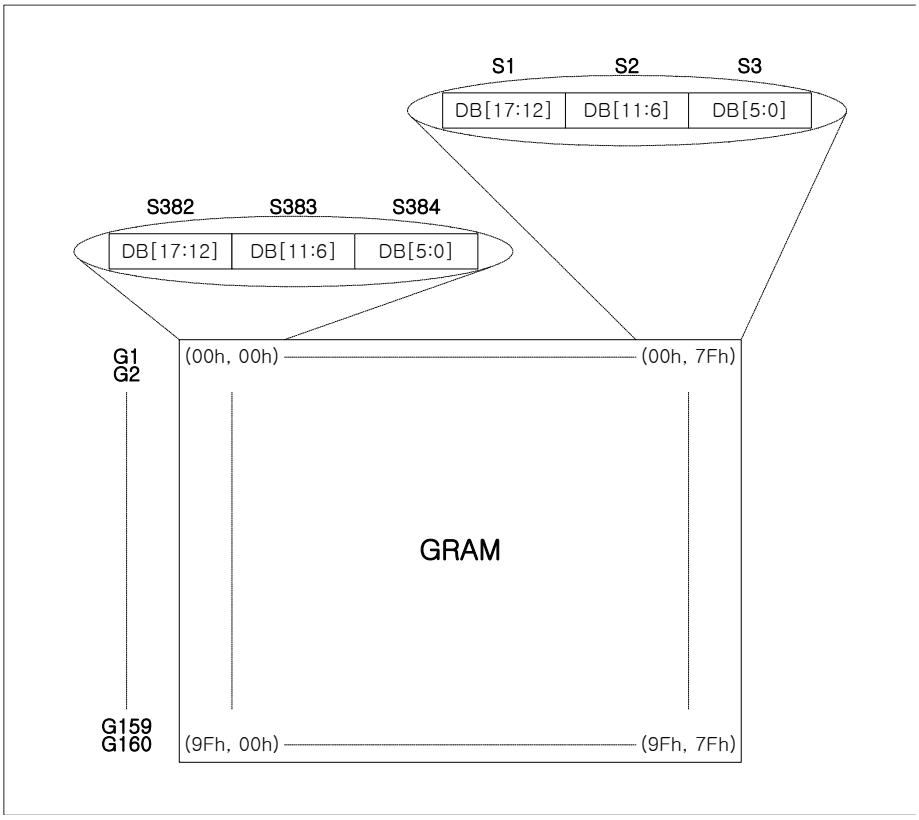


Figure 7 : Image mirroring using SS register (SS = "1")

[NOTE] The display condition of this figure is like this.
SS = 1, BGR = 0, GS = 0.

NL

Specify the number of horizontal lines to be driven. The number of the lines can be adjusted in units of eight. GRAM address mapping is independent of this setting. The set value should be higher than the panel size.

Table 21 : NL bit and Drive Duty (SCN = "00000")

NL[4:0]	Display Size	Drive Line	Gate Driver- Lines Used
00000	*Reserved*		
00001	384 X 8 dots	8	G1 to G8
00010	384 X 16 dots	16	G1 to G16
00011	384 X 24 dots	24	G1 to G24
00100	384 X 32 dots	32	G1 to G32
00101	384 X 40 dots	40	G1 to G40
00110	384 X 48 dots	48	G1 to G48
00111	384 X 56 dots	56	G1 to G56
01000	384 X 64 dots	64	G1 to G64
01001	384 X 72 dots	72	G1 to G72
01010	384 X 80 dots	80	G1 to G80
01011	384 X 88 dots	88	G1 to G88
01100	384 X 96 dots	96	G1 to G96
01101	384 X 104 dots	104	G1 to G104
01110	384 X 112 dots	112	G1 to G112
01111	384 X 120 dots	120	G1 to G120
10000	384 X 128 dots	128	G1 to G128
10001	384 X 136 dots	136	G1 to G136
10010	384 X 144 dots	144	G1 to G144
10011	384 X 152 dots	152	G1 to G152
10100	384 X 160 dots	160	G1 to G160

[NOTE] A FP (front porch) and BP (back porch) period will be inserted as blanking period (All gates output VGL level) before / after the driver scan through all of the scans.

LCD INVERSION CONTROL (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	FL1	FL0	X	X	X	FLD	X	X	X	X

F/L

Set LCD inversion method as show below

Table 22 : LCD inversion selection

FL[1:0]	Description
00	Frame Inversion
01	Line Inversion
10	No Inversion. Active with positive polarity (VCOM = Low)
11	No Inversion. Active with negative polarity (VCOM = High)

For more detail information about inversion, refer to PANEL CONTROL INTERFACE described later.

FLD

Enables or disables 3-field interlaced scanning function like below. When you want to save power consumption, you'd better enable 3 field interfaced scanning function.

Table 23 : LCD interlaced scanning method control

FLD	Description
0	1 field interlace (normal)
1	3 field interlace

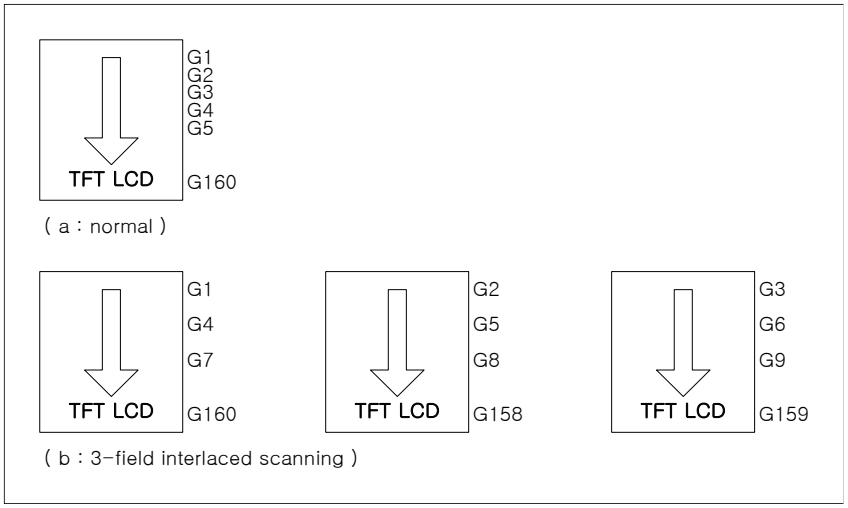


Figure 8 : Interlaced scanning methods

ENTRY MODE (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	BGR	X	X	MDT 1	MDT 0	X	X	ID1	ID0	AM	X	X	X

BGR

When 18-bit data is written to GRAM through DB bus, RGB assignment can be changed.

- BGR = 0 ; {DB[17:12], DB[11:6], DB[5:0]} is assigned to {R, G, B}. Actually the analog value that corresponds to DB[17:12] is output firstly at source output
- BGR = 1 ; {DB[17:12], DB[11:6], DB[5:0]} is assigned to {B, G, R}. Actually the analog value that corresponds to DB[5:0] is output firstly at source output.

MDT

When user wants to transfer 260k color data on 8/16-bit parallel bus, MDT (Multiple Times Data Transfer mode control) register may be used for that.

Table 24 : Multiple Data Transfer Mode Control

MDT[1:0]	IM[3:0]	Description
0X	X	Normal Data Transfer
10	8-bit	260k color data is transferred by 3-times Data Transfer.
	16-bit	260k color data is transferred by 2-times Data Transfer.
11	8-bit	65k color data is transferred by 3-times Data Transfer.
	16-bit	260k color data is transferred by 2-times Data Transfer.

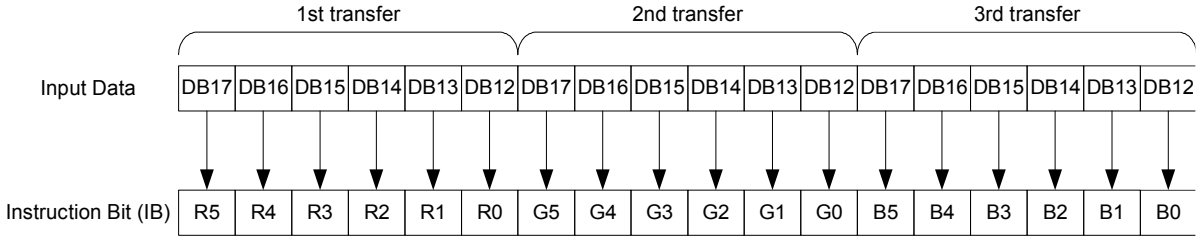


Figure 9 : 260k color data transfer on 8-bit parallel bus (MDT = 2'b10)

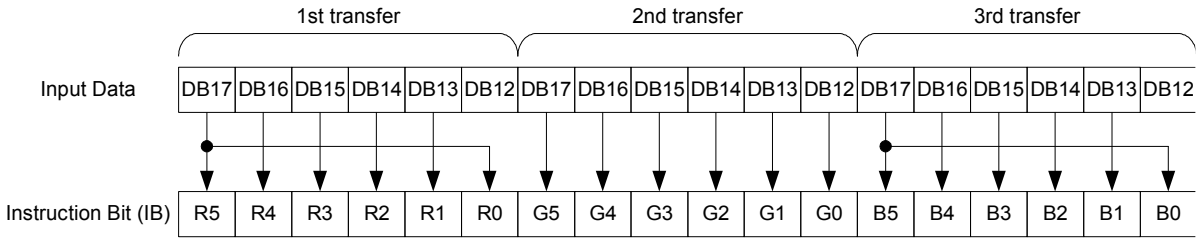


Figure 10 : 65k color data transfer on 8-bit parallel bus by 3-times Data Transfer (MDT = 2'b11)

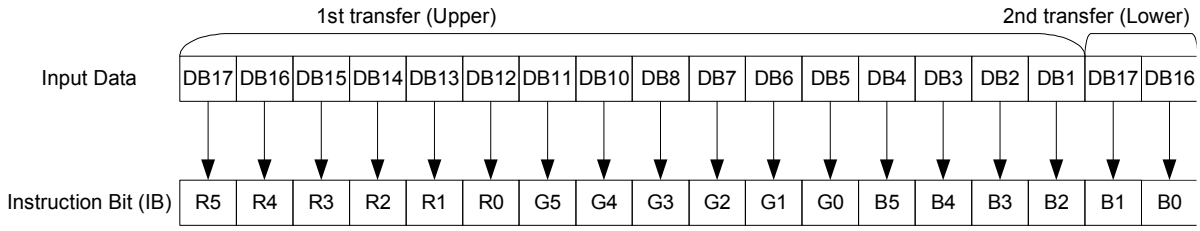


Figure 11 : 260k color data transfer on 16-bit parallel bus (MDT = 2'b10)

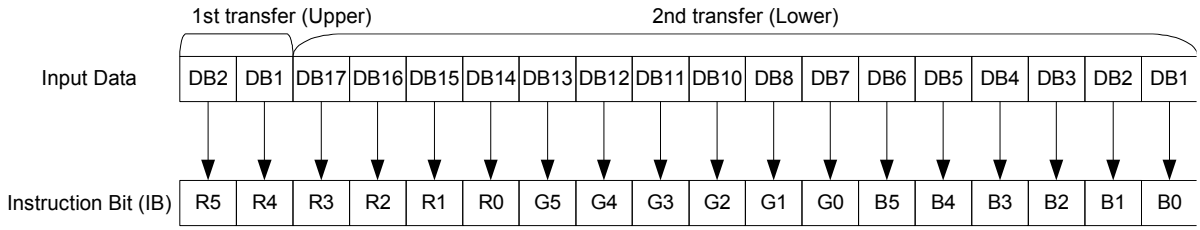


Figure 12 : 260k color data transfer on 16-bit parallel bus (MDT = 2'b11)

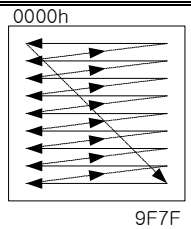
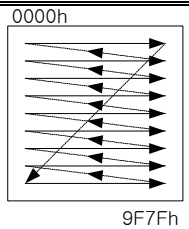
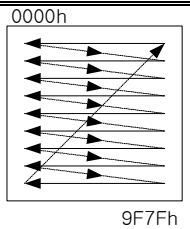
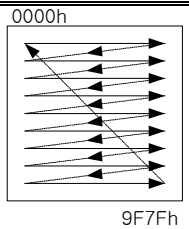
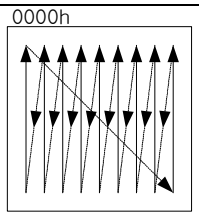
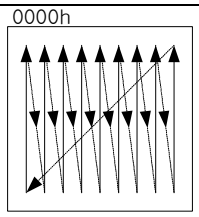
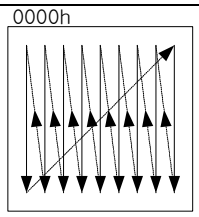
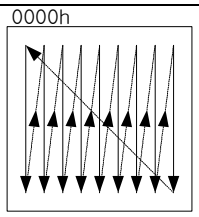
ID

When ID[1], ID[0] = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM.
When ID[1], ID[0] = 0, the AC is automatically decreased by 1 after the data is written to the GRAM.
The increment/decrement setting of the address counter using ID[1:0] is done independently for the horizontal address and vertical address.

AM

Set the automatic update method of the AC after the data is written to GRAM. When AM = “0”, the data is continuously written in horizontally. When AM = “1”, the data is continuously written vertically. When window addresses are specified, the GRAM in the window range can be written to according to the ID[1:0] and AM.

Table 25 : Address Direction Setting

	ID[1:0] = “00” H: decrement V: decrement	ID[1:0] = “01” H: increment V: decrement	ID[1:0] = “10” H: decrement V: increment	ID[1:0] = “11” H: increment V: increment
AM=”0” Horizontal Update				
AM=”1” Vertical Update				

[NOTE] When window addresses have been set, the GRAM can only be written within the window.

When AM or ID is set, the start address should be written accordingly prior to memory write.

DISPLAY CONTROL (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	PT1	PT0	X	X	SPT	X	X	GON	DTE	CL	REV	D1	D0

PT

Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the Screen-division Driving Function section.
You should note that the control with PT is not affected by REV.

Table 26 : Non-Displayed Area Control

PT[1:0]	Source Output for Non-display Area		Gate Output for Non-display Area
	Positive Polarity	Negative Polarity	
00	V63	V0	Normal Drive
01	V0	V63	Normal Drive
10	GND	GND	VGL
11	Hi-z	Hi-z	VGL

[NOTE] In this table, GND means source driver's outputs are short to VcomOUT level.

SPT

When SPT = "1", the Split Screen Driving Function is performed. This function is not available when RGB interface is in use.
For details, see "Split Screen Driving Function section" describe later.

GON / DTE

GON and DTE set gate output (G1 to G160) as following table.

Table 27 : Gate Clock Control

GON	DTE	Gate output	VCOMOUT
0	X	VGH	Halt (VSS)
1	0	VGL	Normal operation
	1	VGH/VGL	Normal operation

CL

CL = 1 selects 8-color display mode. For details, see the section on 8-color display mode.

Table 28 : Color Depth Control

CL	Color Depth
0	262,144 colors / 65,536 colors
1	8 colors

REV

Displays all character and graphics display sections with reversal when REV = 1. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

Table 29 : Source Output Control in operation

REV	GRAM data	Source output level									
		Display Area		Non-display area							
				PT[1:0] = ”00”		PT[1:0] = ”01”		PT[1:0] = “10”		PT[1:0] = “11”	
		Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative
0	6’b000000 : 6’h111111	V63 : V0	V0 : V63	V63	V0	V0	V63	VSS	VSS	Hi-z	Hi-z
1	6’b000000 : 6’h111111	V0 : V63	V63 : V0								

D

Display is on when D[1] = “1” and off when D[1] = “0”. When off, the display data remains in the GRAM, and can be re-displayed instantly by setting D[1] = “1”. When D[1] is “0”, the display is off with the entire source outputs set to the VSS level. Because of this, the S6D0144 can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE. For details, see the Instruction Set-Up Flow.

When D[1:0] = “01”, the internal display of the S6D0144 is performed although the display is off. When D[1:0] = “00”, the internal display operation halts and the display is off.

Table 30 : Source Output Control

D[1:0]	Source output	internal operation
00	GND	Halt
01	GND	Operate
10	White on Normally White Panel Black on Normally Black Panel	Operate
11	Display	Operate

[NOTE]

1. Writing from MCU to GRAM is independent from D.
2. In sleep and standby mode, S6D0144 operates as D[1:0] = “00”. However, the register of D is not modified·
3. In this table, GND means source driver’s outputs are short to VcomOUT level.

BLANK PERIOD CONTROL 1 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	FP3	FP2	FP1	FP0	X	X	X	X	BP3	BP2	BP1	BP0

FP/BP

Set the period of Blank Period, which is placed at the beginning and the end of a frame. FP[3:0] is for a Front Porch and BP[3:0] is for a Back Porch. When Front Porch and Back Porch are set, the settings should meet the following conditions.

BP+FP ≤ 16 lines
FP ≥ 2 lines
BP ≥ 2 lines

When S6D0144 operates in External Clock Operation mode, the Back Porch (BP) will start on the falling edge of the VSYNC signal and display operation begins just after the Back Porch period. The Front Porch (FP) will start when data of the number of lines specified by the NL has been displayed. During the period between the completion of the Front Porch and the next VSYNC signal, the display will remain blank.

Table 31 : Blank Period Control with FP and BP

FP[3:0] (BP[3:0])	Number of Raster Periods In Front (Back) Porch
0000	*Reserved*
0001	*Reserved*
0010	2
0011	3
0100	4
---	---
1000	8
---	---
1100	12
1101	13
1110	14
1111	*Reserved*

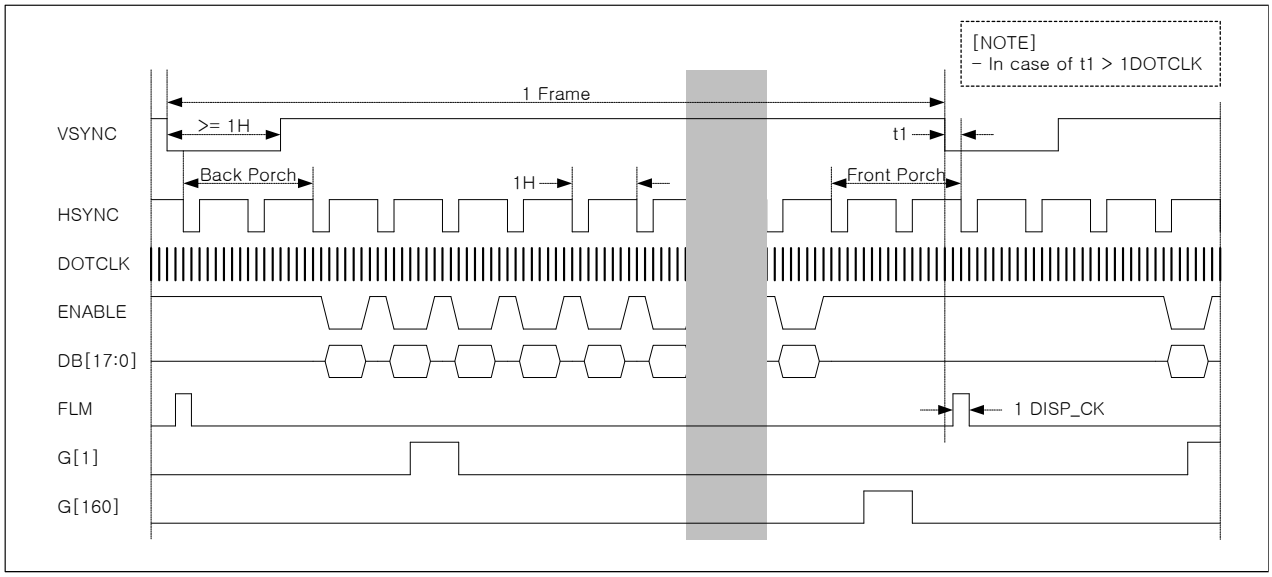


Figure 13 : BP & FP in External Clock Operation Mode (DM[0] = "1")

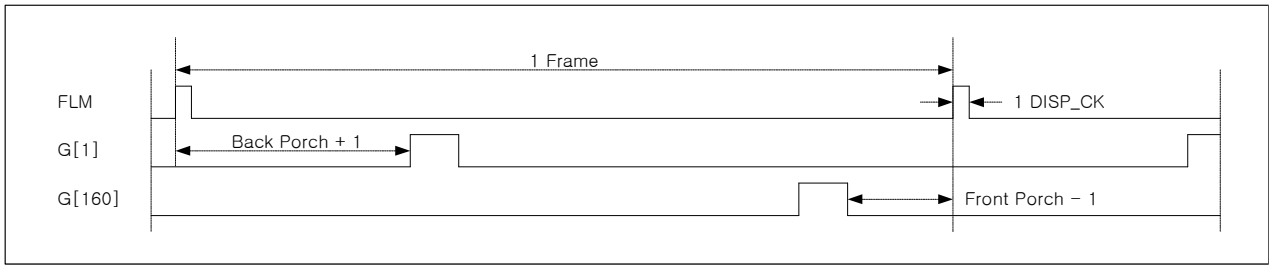


Figure 14 : BP & FP in Internal Clock Operation Mode (DM[0] = "0")

[NOTE] DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)

FRAME CYCLE CONTROL (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	DIV1	DIV0	X	X	X	X	RTN3	RTN2	RTN1	RTN0

DIV

Set the division ratio of clocks for internal operation. Internal operations are driven by clocks, which are frequency divided according to the value of this register. Frame frequency can be adjusted with this. When changing number of the drive cycle, adjust the frame frequency.

Table 32 : Frame Frequency Control

DIV[1:0]	Division Ratio	Internal operation clock frequency
00	1	fosc/1
01	2	fosc/2
10	4	fosc/4
11	8	fosc/8

[NOTE] fosc = R-C oscillation frequency. The clock which is divided by DIV is called as INCLK below

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 15 : Formula for the frame frequency

RTN

Set the 1H period.

Table 33 : Clock Cycles per horizontal line

RTN[3:0]	Clock Cycles per horizontal Line
0000	16 (INCLKs)
0001	17 (INCLKs)
---	---
1110	30 (INCLKs)
1111	31 (INCLKs)

EXTERNAL DISPLAY INTERFACE CONTROL (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	RM	X	X	DM1	DM0	X	X	RIM1	RIM0

RM

Specify the interface for GRAM access as shown below. This register and DM register can be set independently. The display data can be written through System Interface by clearing this register while the RGB interface is used.

Table 34 : RM and GRAM Access Interface

RM	GRAM Access Interface
0	System interface
1	RGB interface

DM

Specify the display operation mode. The interface can be set based on the bits of DM[1:0]. In Internal Clock Opeartion mode the source clock for display operation comes from internal oscillator while in External Clock Opeartion mode it comes from RGB interface(DOTCLK, VSYNC, HSYNC).

Table 35 : DM and Display Operation Mode

DM[1:0]	Display operation mode
00	Internal clock operation
01	External clock operation
10	*Reserved*
11	*Reserved*

RIM

Specify RGB interface mode when the RGB interface is used. This register is valid when RM is set to “1”. DM and this register should be set before proper display operation is performed through the RGB interface.

Table 36 : RIM and RGB Interface Mode

RIM[1:0]	RGB Interface mode
00	6-bit RGB interface (three transfers per pixel)
01	16-bit RGB interface (one transfer per pixel)
10	18-bit RGB interface (one transfer per pixel)
11	*Reserved*

POWER CONTROL 1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DSTB	X	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB

DSTB

When DSTB = 1, the S6D0144 enters the deep standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator and RVDD regulator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Any instructions can not be executed during the deep standby mode.

SAP

Adjust the slew-rate of the operational amplifier for the source driver. If higher SAP2-0 is set, LCD panel having higher resolution or higher frame frequency can be driven because the slew-rate of the operational amplifier is increased. But, these bits must be set as adequate value because the amount of fixed current of the operational amplifier is also adjusted. During non-display, when SAP2-0 = “000”, the current consumption can be reduced.

Table 37 : Current and Slew Rate Control

SAP[2:0]	Slew-Rate of Operational Amplifier	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier halted.	
001	Setting disabled	Setting disabled
010	Slow or medium	Small or medium
011	Medium	Medium
100	Medium or fast	Medium or large
101	Fast	Large
110	Setting disabled	Setting disabled
111	Setting disabled	Setting disabled

*To use SAP=001, please contact SEC engineer.

BT

The output factor of step-up is switched. Adjust scale factor of the step-up circuit by the voltage used. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

Table 38 : Step-Up Control

BT[2:0]	VGH Output	VGL Output	Notes
000	AVDD X 3	-(AVDDx2+VCI1)	VGH = Vci1 X six times
001		-(AVDDx2)	VGH = Vci1 X six times
010		-(AVDD+VCI1)	VGH = Vci1 X six times
011	AVDD X 2 + VCI1	-(AVDDx2+VCI1)	VGH = Vci1 X five times
100		-(AVDDx2)	VGH = Vci1 X five times
101		-(AVDD+VCI1)	VGH = Vci1 X five times
110	AVDD X 2	-(AVDDx2)	VGH = Vci1 X four times
111		-(AVDD+VCI1)	VGH = Vci1 X four times

DC

The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

Table 39 : Step-Up Control

DC[2:0]	Step-up Cycle in Step-up Circuit for	
	AVDD, VCL	VGH, VGL
000	DCCLK / 1	DCCLK / 2
001	DCCLK / 2	DCCLK / 2
010	DCCLK / 4	DCCLK / 2
011	DCCLK / 2	DCCLK / 8
100	DCCLK / 1	DCCLK / 4
101	DCCLK / 2	DCCLK / 4
110	DCCLK / 4	DCCLK / 4
111	DCCLK / 4	DCCLK / 8

[NOTE] DCCLK is asynchronous with Hoizontal Line Clock (as it has been called CL1).

AP

The amount of fixed current in the operational amplifier for the power supply can be adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP2-0 = “000”, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

Table 40 : Current Control

AP[2:0]	Amount of Current in Operational Amplifier
000	Operation of the operational amplifier and step-up circuit stops.
001	Small
010	Small or medium
011	Medium
100	Medium or large
101	Large
110	Setting Inhibited
111	Setting Inhibited

SLP

When SLP = 1, the S6D0144 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

– Power control (BT2–0, DC3–0, AP2–0, SLP, STB, VC3-0, VRH3-0, VCOMG, VDV6-0, and VCM6-0 bits)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained and G1 to G160output is fixed to VSS level, and register set-up is protected (maintained).

STB

When STB = 1, the S6D0144 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

– Standby mode cancel(STB = “0”)
– Start oscillation

Table 41 : Operation Mode Summary

Mode	Operation	Oscillator	RVDD
Normal	Active	Active	Active
Sleep	Inactive	Active	Active
Standby	Inactive	Inactive	Active
Deep Standby	Inactive	Inactive	Inactive

GAMMA CONTROL 1 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VR1C	X	X	VRN14	VRN13	VRN12	VRN11	VRN10	X	X	X	VRP14	VRP13	VRP12	VRP11	VRP10

VR1C

Control step of amplitude positive and negative of 64-grayscale. For details, see the amplitude Adjusting Circuit section.

VRP1[4:0]

Control amplitude positive polarity of 64-grayscale. For details, see the amplitude Adjusting Circuit section.

VRN1[4:0]

Control amplitude negative polarity of 64-grayscale. For details, see the amplitude Adjusting Circuit section.

POWER CONTROL 2 (R12h)

POWER CONTROL 3 (R13h)

POWER CONTROL 4 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	SVC 3	SVC 2	SVC 1	SVC 0	X	VC2	VC1	VC0
W	1	X	X	X	X	VCM R	X	X	X	X	X	X	PON	VRH 3	VRH 2	VRH 1	VRH 0
W	1	X	VDV 6	VDV 5	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0	VCO MG	VCM 6	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0

SVC

Adjust reference voltage of AVDD, VGH, VGL and VCL

Table 42 : VCI1 voltage setting

SVC[3:0]	VCI1 [Without Load]
0000	2.10 V
0001	2.16 V
0010	2.22 V
0011	2.28 V
0100	2.34 V
0101	2.40 V
0110	2.46 V
0111	2.52 V
1000	2.58 V
1001	2.64 V
1010	2.70 V
1011	2.76 V
1100	Setting Disable
1101	Setting Disable
1110	Setting Disable
1111	Setting Disable

[Note] VCI = VCI1, when VCI is lower than VCI1.

VC

Adjust reference voltage of VREFS for GVDD.

Table 43 : Internal Reference Voltage Control

VC[2:0]	Internal Reference Voltage VREFS
000	2.879
001	2.648
010	Setting disabled
011	2.389
100	Setting disabled
101	Setting disabled
110	2.101
111	2.879

[NOTE] Let VREFS < VCI.

PON

The operational amplifier ON/OFF signal. PON = 0 is to stop and PON = 1 to start operation. For further information about timing, please refer to the set up flow of power supply circuit.

VCMR

Select VCOMH adjusting method. It is selected from external resistor setting (VCOMR) or internal electronic volume setting(VCM).

Table 44 : VCOMH Control

VCMR	VCOMH voltage
0	VCOMR
1	Internal electronic volume

VRH

Set the amplified factor of the GVDD voltage

Table 45 : GVDD Control

VRH[3:0]	GVDD Voltage
0000	Setting disabled
…	Setting disabled
0111	Setting disabled
1000	VREFS x 1.38
1001	VREFS x 1.45
1010	VREFS x 1.53
1011	VREFS x 1.60
1100	VREFS x 1.68
1101	VREFS x 1.75
1110	VREFS x 1.83
1111	Setting disabled

[NOTE] 1) Adjust the VRH so that the GVDD voltage is lower than 5.0 V.

VCOMG

When VCOMG = 1, VcomL voltage can output to negative voltage (-2.8V).
When VCOMG = 0, VcomL voltage becomes VSS and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, When VCOMG = 0 and when Vcom is driven in A/C, set up of the VDV6-0 is invalid. In this case, adjustment of Vcom A/C amplitude must be adjusted VcomH with VCM6-0.

VDV

Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify Vcom 0.534 to 1.20 times the GVDD voltage. When the Vcom alternation is not driven, the settings become invalid.

Table 46 : Vcom Amplitude Control

VDV[6:0]	Vcom Amplitude
0000000	Setting disable
:	Setting disable
0001111	Setting disable
0010000	GVDD X 0.534
0010001	GVDD X 0.540
:	:
0010101	GVDD X 0.564
0010110	GVDD X 0.570
0010111	GVDD X 0.576
:	:
1111110	GVDD X 1.194
1111111	GVDD X 1.200

[NOTE] Adjust the settings between GVDD and VDV0 to VDV6 so that the Vcom amplitudes are lower than 6.0 V.
VcomL voltage should be : VCL+0.5 < VcomL <0.0V

VCM

Set the VcomH voltage (a high-level voltage at the Vcom alternating drive). These bits amplify the VcomH voltage 0.36 to 0.98 times the GVDD voltage. When VCOMR = 0, the adjustment of the internal volume stops, and VcomH can be adjusted from VcomR by an external resistor.

Table 47 : VcomH Control

VCM[6:0]	VcomH Voltage
0000000	GVDD X 0.360
0000001	GVDD X 0.365
0000010	GVDD X 0.370
:	:
0001100	GVDD X 0.420
0001101	GVDD X 0.425
0001110	GVDD X 0.430
:	:
1111011	GVDD X 0.975
1111100	GVDD X 0.980
1111101	Setting disable
1111110	Setting disable
1111111	Setting disable

GRAM ADDRESS SET (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD

You can write initial GRAM address into internal Address Counter (AC). When GRAM data is transferred through System Interface or RGB Interface, the AC is automatically updated according to AM and ID. This allows consecutive write without re-setting address in AC. But when GRAM data is read, the AC is not automatically updated.
GRAM address setting is not allowed in Standby mode. Ensure that the address is set within the specified window area specified with VSA, VEA, HSA and HEA.
When RGB interface is used (RM="1") to access GRAM, AD[16:0] will be set in the address counter at the falling edge of the VSYNC signal. And when one uses System Interface to access GRAM (RM = "0"), AD[16:0] will be set upon the execution of an instruction.

Table 48 : GRAM Address Range

AD[15:0]	GRAM setting
"0000H" to "007F"H	Bitmap data for G1
"0100H" to "017F"H	Bitmap data for G2
"0200H" to "027F"H	Bitmap data for G3
"0300H" to "037F"H	Bitmap data for G4
: : :	: : :
"9C00H" to "9C7F"H	Bitmap data for G157
"9D00H" to "9D7F"H	Bitmap data for G158
"9E00H" to "9E7F"H	Bitmap data for G159
"9F00H" to "9F7F"H	Bitmap data for G160

WRITE DATA TO GRAM (R22h)

R/W	RS	
W	1	RAM write data (WD17 ~ WB0). ※Interface mode controls the width of WD

WDR

Data on DB bus is expanded to 18-bits before being written to GRAM and the data determines grayscale level of S6D0144's source output. Please keep in mind that the expansion format varies with interface mode.
GRAM cannot be accessed in Standby mode. When data is written to GRAM via system interface while another data is being written to through RGB interface, please make sure that the two write operations does not conflict.

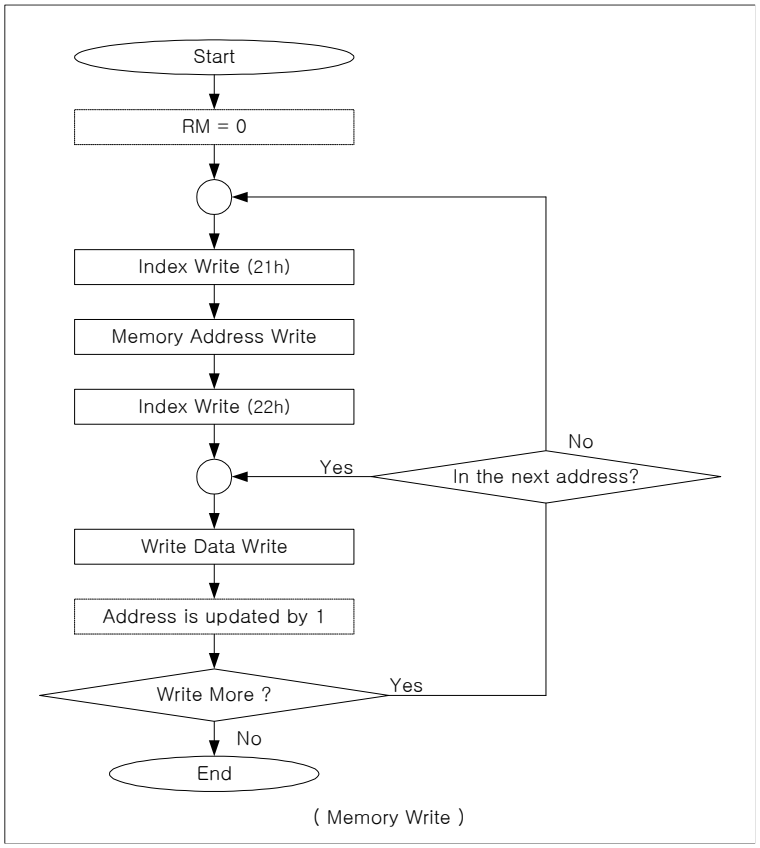


Figure 16 : Memory Data Write Sequence

READ DATA FROM GRAM (R22h)

RDR

You may read data from GRAM using this register. When you make read operations, you can get a proper data on the second read operation as shown below. The first word you get just after address setting may be invalid.

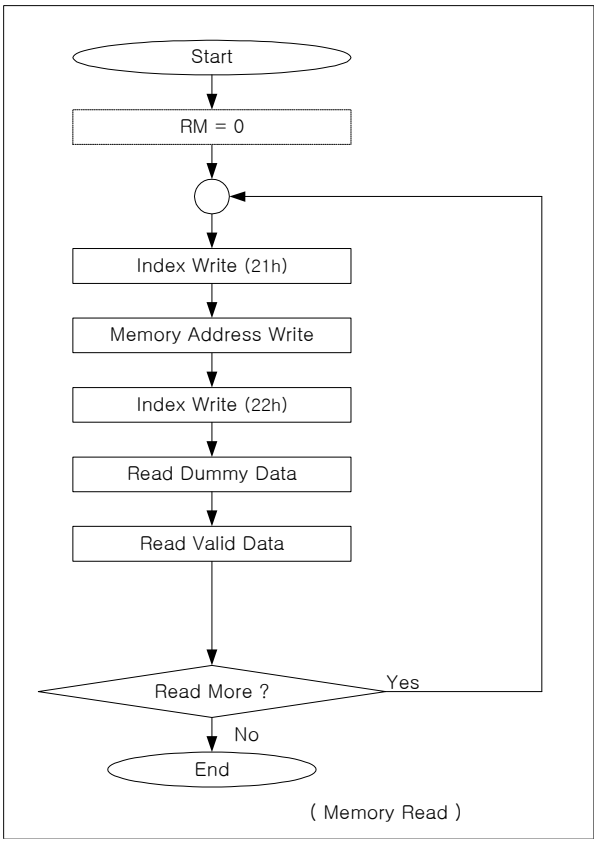


Figure 17 : Memory Data Read Sequence

GAMMA CONTROL 2 (R30h to R37h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	PKP 12	PKP 11	PKP 10	X	X	X	X	X	PKP 02	PKP 01	PKP 00
W	1	X	X	X	X	X	PKP 32	PKP 31	PKP 30	X	X	X	X	X	PKP 22	PKP 21	PKP 20
W	1	X	X	X	X	X	PKP 52	PKP 51	PKP 50	X	X	X	X	X	PKP 42	PKP 41	PKP 40
W	1	X	X	X	X	X	PRP 12	PRP 11	PRP 10	X	X	X	X	X	PRP 02	PRP 01	PRP 00
W	1	X	X	X	X	X	PKN 12	PKN 11	PKN 10	X	X	X	X	X	PKN 02	PKN 01	PKN 00
W	1	X	X	X	X	X	PKN 32	PKN 31	PKN 30	X	X	X	X	X	PKN 22	PKN 21	PKN 20
W	1	X	X	X	X	X	PKN 52	PKN 51	PKN 50	X	X	X	X	X	PKN 42	PKN 41	PKN 40
W	1	X	X	X	X	X	PRN 12	PRN 11	PRN 10	X	X	X	X	X	PRN 02	PRN 01	PRN 00

PKP5[2:0], PKP4[2:0], PKP3[2:0], PKP2[2:0], PKP1[2:0], PKP0[2:0]

The gamma fine adjustment registers for the positive polarity output

PRP1[2:0], PRP0[2:0]

The gradient adjustment registers for the positive polarity output

PKN5[2:0], PKN4[2:0], PKN3[2:0], PKN2[2:0], PKN1[2:0], PKN0[2:0]

The gamma fine adjustment registers for the negative polarity output

PRN1[2:0], PRN0[2:0]

The gradient adjustment registers for the negative polarity output

For details, see the Gamma Adjustment Function.

GAMMA CONTROL 3 (R38h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	VRN 03	VRN 02	VRN 01	VRN 00	X	X	X	X	VRP 03	VRP 02	VRP 01	VRP 00

VRP0[3:0]

Control amplitude positive polarity of 64-grayscale. For details, see the amplitude Adjusting Circuit section.

VRN0[3:0]

Control amplitude negative polarity of 64-grayscale. For details, see the amplitude Adjusting Circuit section.

GATE SCAN POSITION (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0

SCN

Set the scanning starting position of the gate driver.

Table 49 : Gate Scan Position Control

SCN[4:0]	Start Position	
	GS = 0	GS = 1
00000	G1	G160
00001	G9	G152
00010	G17	G144
---	---	---
10001	G137	G24
10010	G145	G16
10011	G153	G8

[NOTE] Ensure that gate start position (SCN) + the number of LCD driver lines (NL) ≤ 160 when GS = 0, and that gate start position (SCN) - the number of LCD driver lines (NL) ≥ 0 when GS = 1

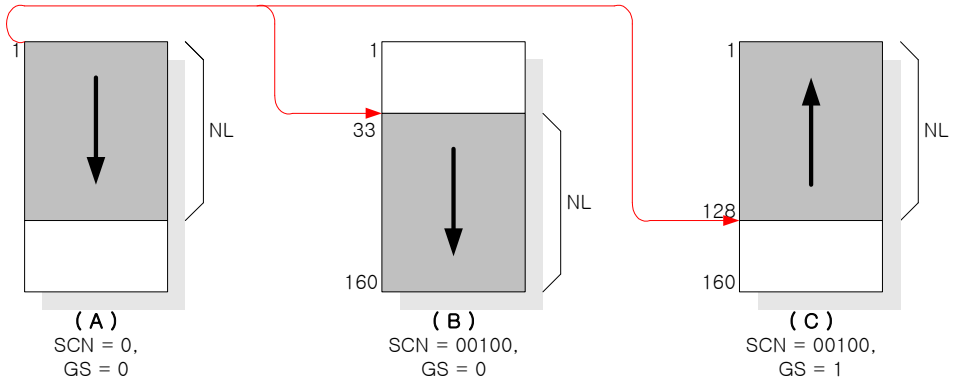


Figure 18 : Gate Scan Position Control

1st SCREEN DRIVING POSITION (R42h)
2nd SCREEN DRIVING POSITION (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS1

Specify the start position of the first screen to drive in a line unit. The LCD display starts from “SS1 + 1”.

SE1

Specify the end position of the first screen to drive in a line unit. The LCD display is performed to the “SE1 + 1”. For instance, when SS[7:0] = “07h” and SE[7:0] = “10h” are set, the LCD display is performed from G8 to G17, and white or black display is performed according to PT for G1 to G7, G18 and others. Ensure that SS1[7:0] ≤ SE1[7:0] ≤”9F”h.
For details, see “SPLIT SCREEN DRIVING FUNCTION” described later.

SS2

Specify the start position of the second screen to display in a line unit. The LCD display starts from the “SS2 + 1”. The second screen is displayed when SPT = “1”.

SE2

Specify the end position of the second screen to display in a line unit. The LCD display is performed to the “SE2 + 1”. For instance, when SS2[7:0] = “20h”, SE2[7:0] = “4Fh” and SPT = “1” are set, the LCD display is performed from G33 to G80. Ensure that “00h”≤SS1[7:0] ≤ SE1[7:0] ≤ SS2[7:0] ≤ SE2[7:0] ≤ ”9Fh”.
For details, see “SPLIT SCREEN DRIVING FUNCTION” described later.

HORIZONTAL RAM ADDRESS POSITION (R44h)

VERTICAL RAM ADDRESS POSITION (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
W	1	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

VSA, VEA

Specify the vertical start/end positions of a window for access to the specified partial memory (Window). Data can be written to GRAM from the address specified by VEA[7:0] to the address specified by VSA[7:0]. Note that the Window Addresses must be set before GRAM is updated. Ensure 00h ≤ VSA[7:0] ≤ VEA[7:0] ≤ ”9F”h.

HSA, HEA

Specify the horizontal start/end positions of a Window for access to the specified partial memory (Window). Data can be written to GRAM from the address specified by HSA[7:0] to the address specified by HEA[7:0]. Note that the Window Addresses must be set before GRAM is updated. Ensure 00h ≤ HSA[7:0] ≤ HEA[7:0] ≤ ”7F”h.

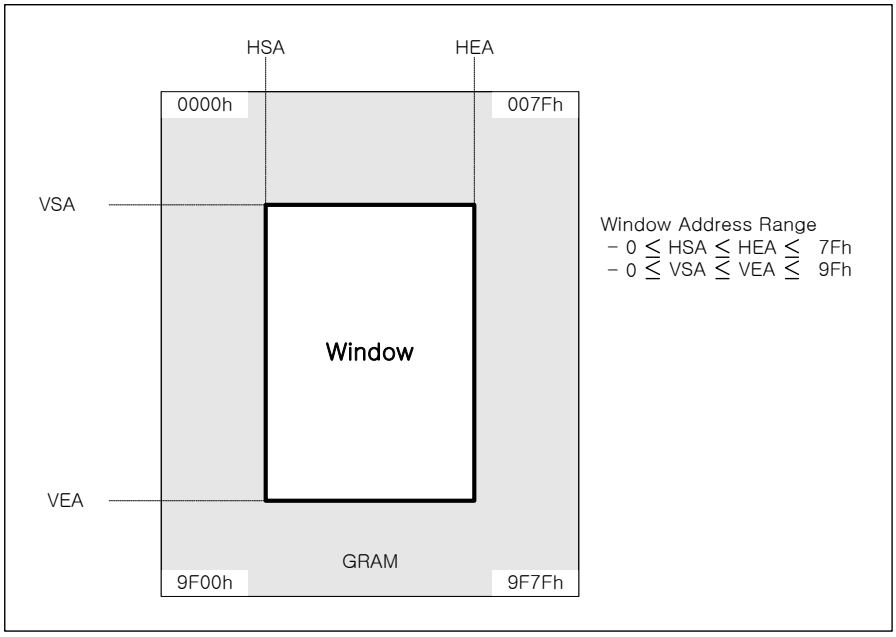


Figure 19 : Window Address Function

[NOTE] Ensure that the Window addresses are within the GRAM address space.

■ SPLIT SCREEN DRIVING FUNCTION

S6D0144 can select and drive two screens at any position with the screen-driving position registers. Any of the two screens required for display are selectively driven and so you can reduce power consumption.

For the 1st divided screen, start line and end line are specified by the 1st screen-driving position registers (SS1[7:0], SE1[7:0]). For the 2nd division screen, start line and end line are specified by the 2nd screen-driving position registers (SS2[7:0], SE2[7:0]).

The 2nd screen control is effective when SPT is set to "1". The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

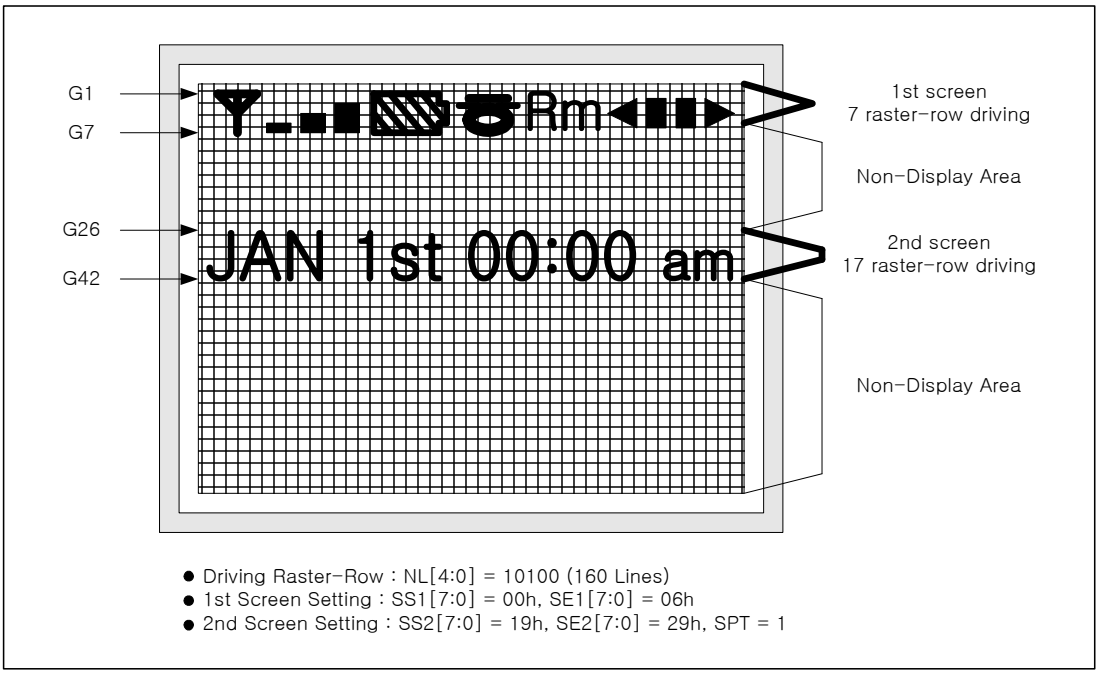


Figure 20 : Split Screen Driving Function

■ Examples of Split Screen Driving Function

Table 50 : Split Screen Driving Function with SPT = 0

Register Value	Display Operation
SE1[7:0] – SS1[7:0] = NL	Full screen display Normally display from SS1[7:0] to SE1[7:0]
SE1[7:0] – SS1[7:0] < NL	Partial display Normally display from SS1[7:0] to SE1[7:0] Black or White display according to PT in remained area (GRAM data is not related at all)
SE1[7:0] – SS1[7:0] > NL	Setting disabled

[NOTE] SS2[7:0] and SE2[7:0] are ignored

Table 51 : Split Screen Driving Function with SPT = 1

Register Value	Display Operation
SE1[7:0] – SS1[7:0] + SE2[7:0] – SS2[7:0] = NL	Full screen display Normally display from SS1[7:0] to SE2[7:0]
SE1[7:0] – SS1[7:0] + SE2[7:0] – SS2[7:0] < NL	Partial display Normally displays from SS1[7:0] to SE1[7:0] and from SS2[7:0] to SE2[7:0] Black or White display according to PT in remained area (RAM data is not related at all)
SE1[7:0] – SS1[7:0] + SE2[7:0] – SS2[7:0] > NL	Setting disabled

■ PARTIAL DISPLAY SETUP FLOW

Refer to the following flowchart to set up Partial Display. It is possible to determine the output levels of the driver in Non-Display Area (the area out of partial display), so one can select appropriate level depending on the panel's condition.

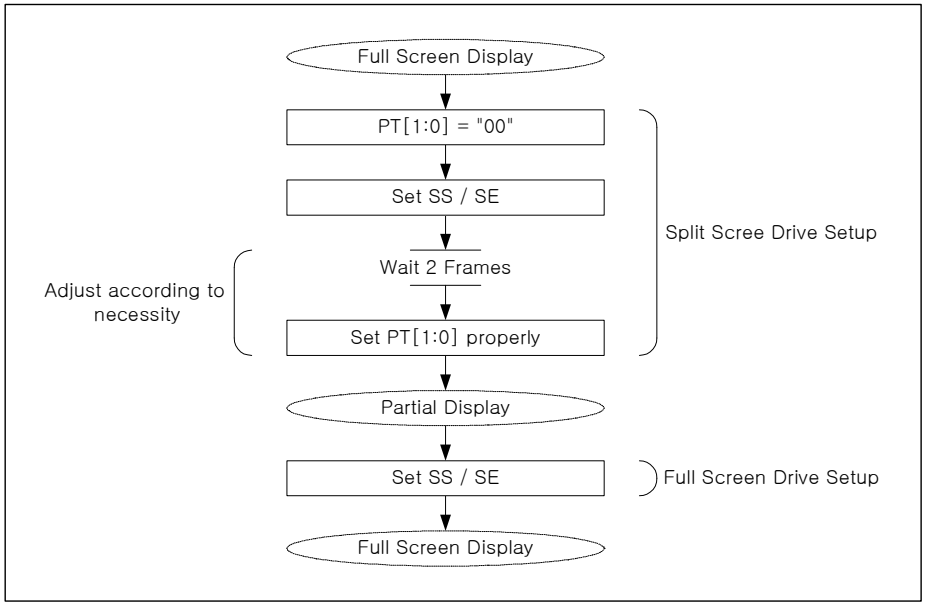


Figure 21 : Partial Display Set Up Flow

■ DATA UPDATE WITH WINDOW ADDRESS FUNCTION

When data is written to the internal GRAM, the Window that is specified by the horizontal address register (HSA[7:0], HEA[7:0]) and the vertical address register (VSA[7:0], VEA[7:0]) can be updated consecutively. Data is written in the direction specified by AM (horizontally / vertically) and ID (incrementally / decrementally). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.
The Window must be specified to be within GRAM address area as described below and the start address for write must be set within the Window.

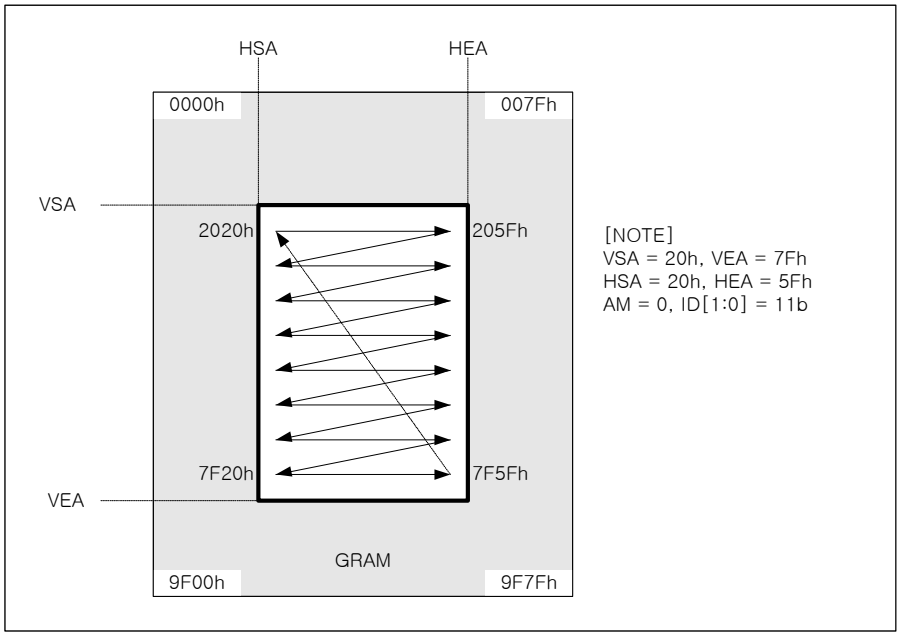


Figure 22 : Example of Data Update with Window Address Function

OSCILLATOR CONTROL (R61h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	RADJ4	RADJ3	RADJ2	RADJ1	RADJ0

RADJ

Select the oscillation frequency of internal oscillator.

Table 52 : RADJ and Internal oscillator oscillation frequency

RADJ[4:0]	Oscillation Speed	
00000	Setting disabled	
:	Setting disabled	
10000	Setting disabled	
10001	x 0.768	Min.
10010	X 0.795	
10011	x 0.823	
10100	x 0.853	
10101	x 0.885	
10110	x 0.921	
10111	x 0.958	
11000	x 1.000	Default
11001	x 1.045	
11010	x 1.095	
11011	x 1.148	
11100	x 1.210	
11101	x 1.276	Max.
11110	Setting disabled	
11111	Setting disabled	

[Note] Setting example)If the default oscillation frequency is 240kHz and the register setting of RADJ[4:0] is 10001, internal oscillator oscillation frequency is 240kHz x 0.768 =184kHz.

DC/DC CONVERT LOW POWER MODE SETTING (R69h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	NLDC3	NLDC2	NLDC1	NLDC0	NLPM

NLPM

Set DC/DC converter to the Low power mode.

Table 53 : VGH,VGL DC/DC converter operation mode

NLPM	Operation mode
0	Normal operation mode
1	Low power mode

NLDC

Set the operation clock speed of each DC/DC converter circuit as following table while the low power mode. These setting are valid in NLPM=1.

Table 54 : AVDD DC/DC converter operation while low power mode

NLDC[1:0]	AVDD, VCL DC/DC converter operation clock
00	DCCLK/1
01	DCCLK/2
10	DCCLK/4
11	DCCLK/8

Table 55 : VGH DC/DC converter operation while low power mode

NLDC[3:2]	VGH, VGL DC/DC converter operation clock
00	DCCLK/2
01	DCCLK/4
10	DCCLK/8
11	DCCLK/16

SOURCE DRIVER PRE-DRIVING PERIOD SETTING (R70h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	SDT 1	SDT 0	X	X	X	X	EQ1	EQ0

The S6D0144 generates the TFT-LCD drive timing inside. The TFT-LCD panel is driven at the timing of one line display period(1H) generated based on RTN[3:0](R0Bh) setting.

EQ

EQ period is sustained for the number of clock cycle that is set in EQ1-0. When VcomL<0V, use AVDD-VcomL<6V or set these bits as “00” for preventing the abnormal function.

Table 56 : Equalization Control

EQ	EQ Period Internal Operation (synchronized with internal clock)
00	No EQ
01	1 DISP_CK
10	2 DISP_CKs
11	3 DISP_CKs

[NOTE] DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2’b00) or DOTCLK divided by 8(DM = 2’b01 and RIM[1] = 1’b1)
f(EQ) + f(SDT) + f(GNO) < 15 DISP_CKs

SDT

Set delay amount from 1H start timing to source output.

Table 57 : Source Output Delay Control

SDT	Delay Amount of the Source Output
00	1 DISP_CK
01	2 DISP_CKs
10	3 DISP_CKs
11	4 DISP_CK s

[NOTE] DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2’b00) or DOTCLK divided by 8(DM = 2’b01 and RIM[1] = 1’b1)
f(EQ) + f(SDT) + f(GNO) < 15 DISP_CKs

For detail, refer to “PANEL CONTROL INTERFACE TIMING DIAGRAMS” described later.

GATE OUTPUT PERIOD CONTROL (R71h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	GNO 1	GNO 0	X	X	X	X	X	X	X	X	X	X

GNO

Control the amount of non-overlap period between gate outputs.

Table 58 : Non-Overlap Period Control

GNO	Non-Overlap Period
00	2 DISP_CKs
01	4 DISP_CKs
10	6 DISP_CKs
11	8 DISP_CK s

[NOTE] DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)
f(EQ) + f(SDT) + f(GNO) < 15 DISP_CKs

SOFTWARE RESET CONTROL (R72h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SR

SR

User can reset the internal status of S6D0144 by setting this register to “0”. This register is automatically set to “1” after about 100ns.

TEST_KEY (R73h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	TEST_KEY[7:0]							

TEST_KEY

When you want to update MTP data, “A5” should be written to this register. And you should write different value for MTP data not to be corrupted.

PUMPING CLOCK SOURCE SELECTION (RB3h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	DCR_EX	X	X	X	X

DCR_EX

Select the source of pumping clock

Table 23 : Pumping Clock Control

DCR_EX	Source of the pumping clock
0	Internal Oscillator Clock
1	External DOTCLK

MTP CONTROL (RB4h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	MTP_SEL	X	X	X	MTP_INIT	X	X	X	MTP_WRB	X	X	X	MTP_LOAD

MTP_LOAD

User can load MTP data into internal register with writing “1” to this register before reading.

MTP_WRB

User can write MTP data writing “0” to this register.

MTP_INIT

User can initialize MTP data writing “1” to this register and writing “0” to MTP_WRB register

MTP_SEL

User can use MTP data to control VCOMH.

Table 24 : VCOMH Control

MTP_SEL	VCOMH Control Data
0	VCM Register
1	MTP data

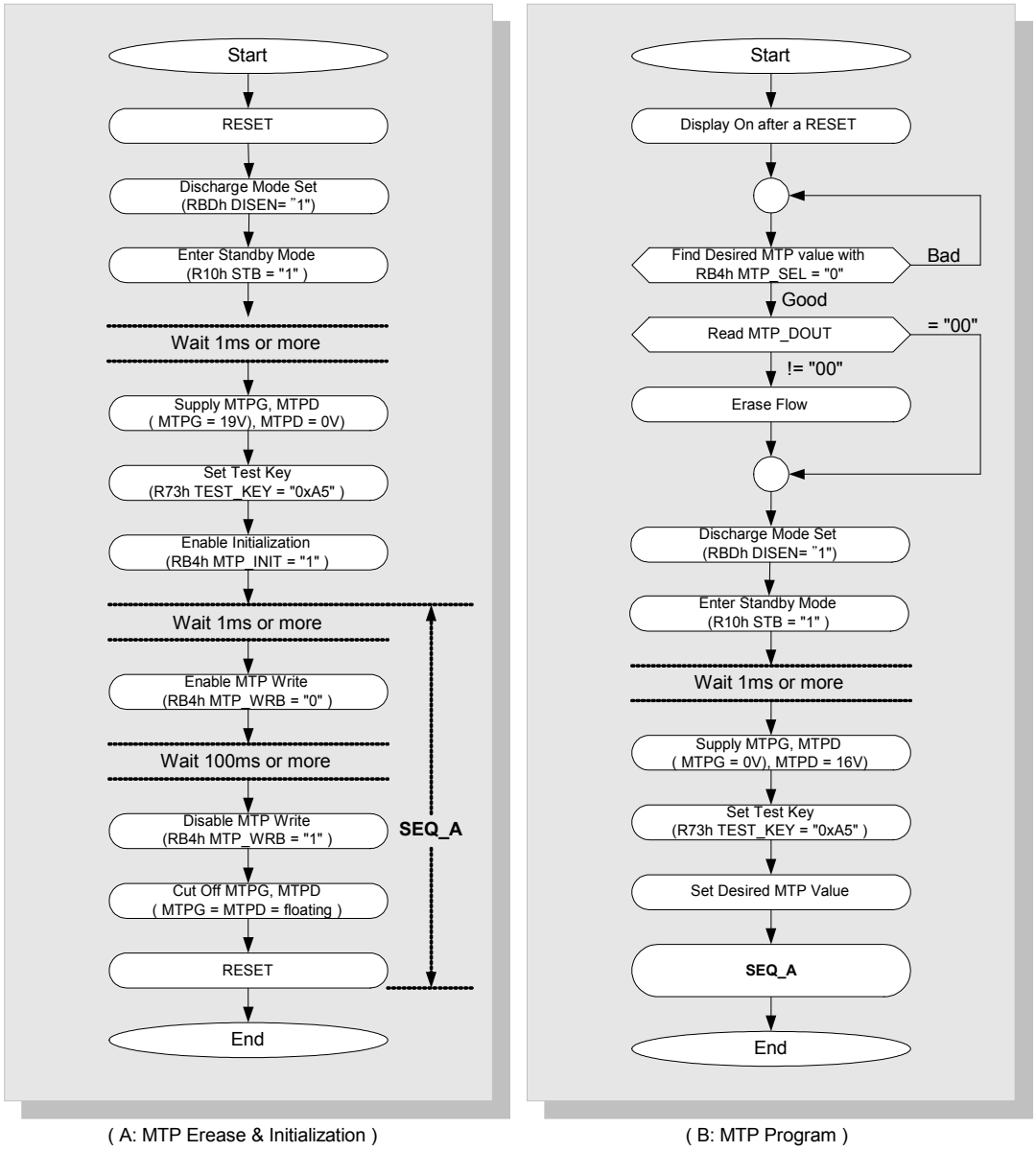


Figure 25 : MTP Initializae, Erase & Program Flow of S6D0144

MTP DATA READ (RBDh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R/W	1	X	X	X	X	X	X	X	DIS EN	X	MTP_DOUT[6:0]						

DISEN

Battery off detection discharge circuit and standby mode discharge circuit operation setting register.

Table 59 : Discharge Circuit Operation

DISEN	VGL/VCL discharge circuit operation
0	Discharge circuit operation stop
1	Discharge circuit operating

MTP_DOUT

MTP data read using MTP_READ reigister.

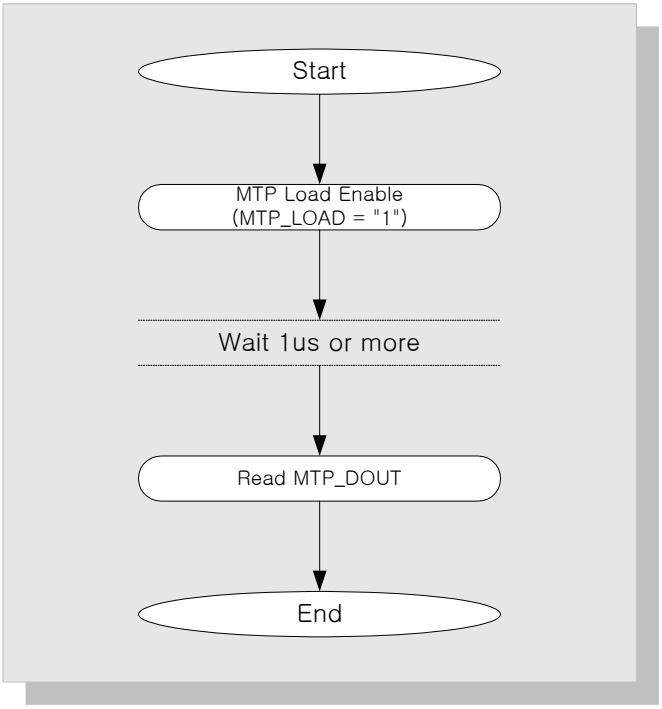


Figure 26 : MTP Read Flow of S6D0144

INTERFACE MODE SELECTION (RBEh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	IM_SEL	IM_3	X	X	X

IM_SEL

IM_SEL register selects interface mode.
Interface mode is selected by external pins(IM[3:0]) when the value of IM_SEL is 0 and interface mode is selected by internal register(IM_3) and external pins(IM[2:0]) when the value of IM_SEL is 1.
In SPI mode, the use of IM_SEL is prohibited.
The initial value of IM_SEL is 0.

Table 60 : Interface mode selection

IM_SEL	Interface mode
0	IM[3:0]
1	{IM_3, IM[2:0]}

IM_3

IM_3 is only applied to the interface mode if IM_SEL is set to 1.
The initial value of IM_3 is 0..

RESET FUNCTION

The S6D0144 is internally initialized by RESET input. The reset input must be held for at least 20us. Don't access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization

All Registers in S6D0144 are initialized when RESET is asserted.

GRAM Data Initialization

GRAM is not automatically initialized by RESET input so it must be initialized by software while display is off(D = 00).

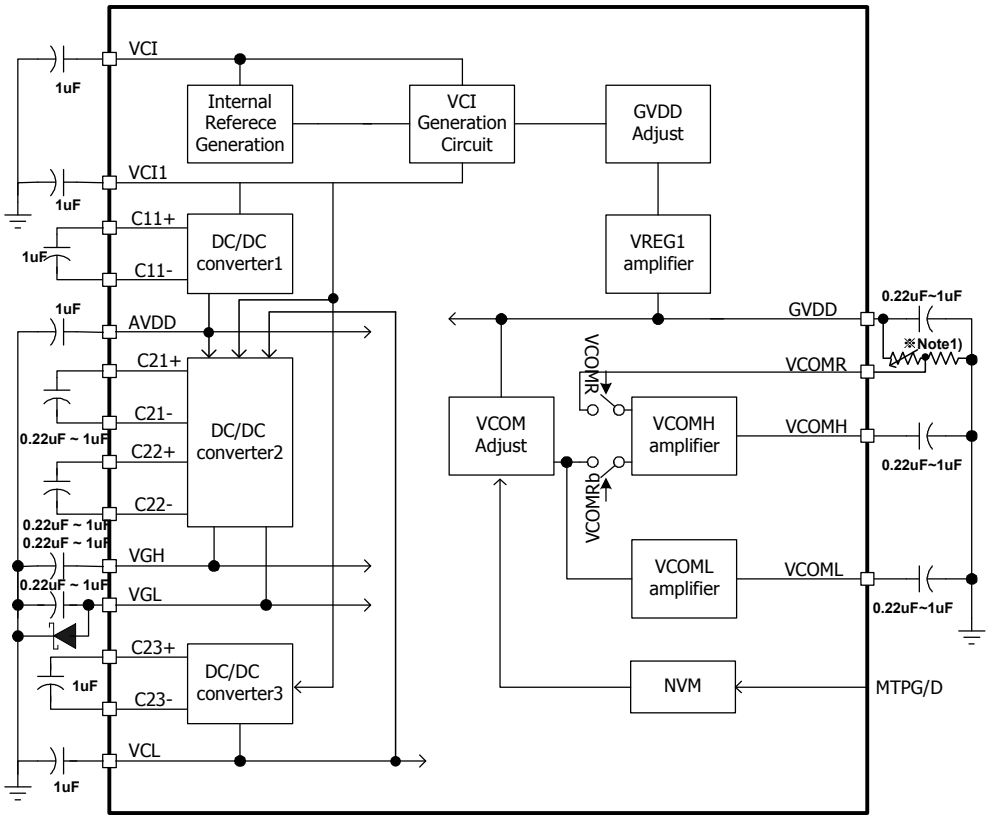
Output Pin Initialization

1. LCD driver output pins (Source output) : Output VSS level
   (Gate output) : Output VGH level

POWER CONTROL

POWER SUPPLY CIRCUIT

The following figure shows a configuration of the voltage generation circuit for S6D0144. The step-up circuits consist of step-up circuits 1 to 3. Step-up circuit1 doubles the voltage supplied to VCI1, and that voltage is X2, X2.5, X3 in step-up circuit2. Step-up circuit 3 reverses the VCI1 level with reference to VSS and generates the VCL level. These step-up circuits generate power supplies AVDD, GVDD, VGH, VGL, and VCOM. Reference voltages GVDD, VCOM, and VGL for the grayscale voltage are amplified in amplification circuits 1 and 2 from the internal-voltage adjustment circuit or the REGP or REGN voltage, and generate each level depending on that voltage. Connect VCOM to the TFT panel.

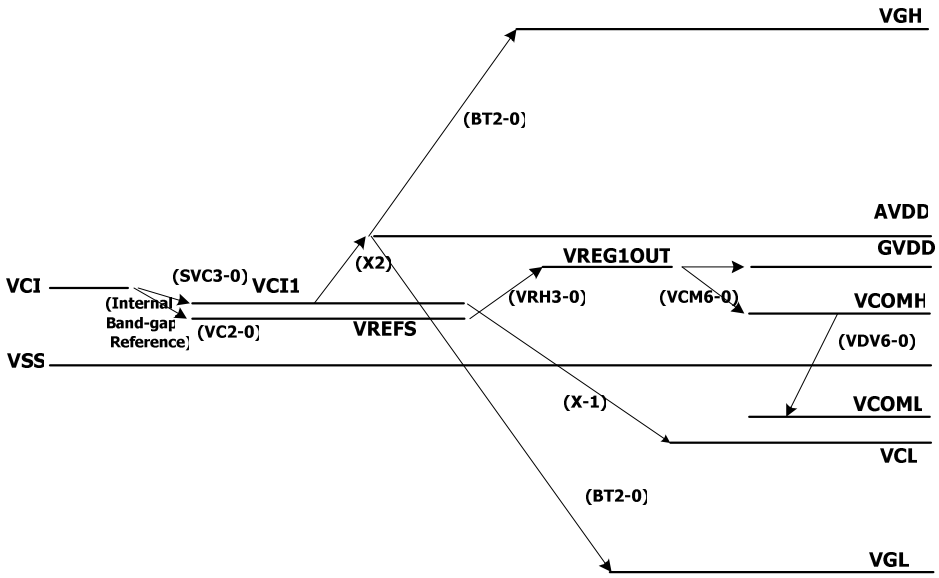


Note1) When VCOMH is externally adjusted, attach these registor. The total resistance should be higher than 100 kilohm.

Figure 27 : Configuration of the Internal Power-Supply Circuit

PATTERN DIAGRAMS FOR VOLTAGE SETTING

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.



Note1 : Adjust the conditions of AVDD-GVDD>0.5V, VCOML-VCL>0.5V, with loads because they differ depending on the display load to be driven.

Note2 : If VCI is smaller than internal bandgap reference output VCI1, VCI1 outputted level is VCI. (without Load)

Note3 : VREG1OUT is IC internal name

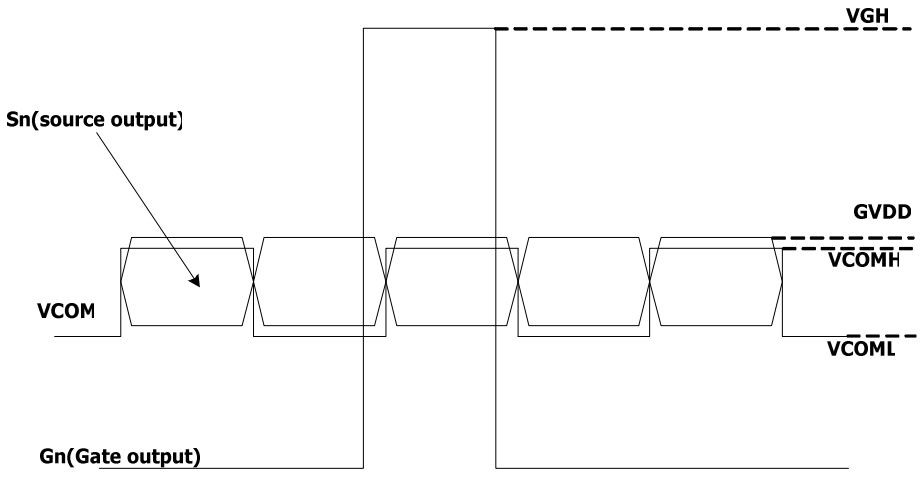


Figure 28 : Pattern diagram and an example of waveforms

SETUP FLOW OF POWER SUPPLY

Apply the power in a sequence as shown in the following figure. The stable time of the oscillation circuit, step-up circuit, and operational amplifier depend on the external resistor or capacitance.

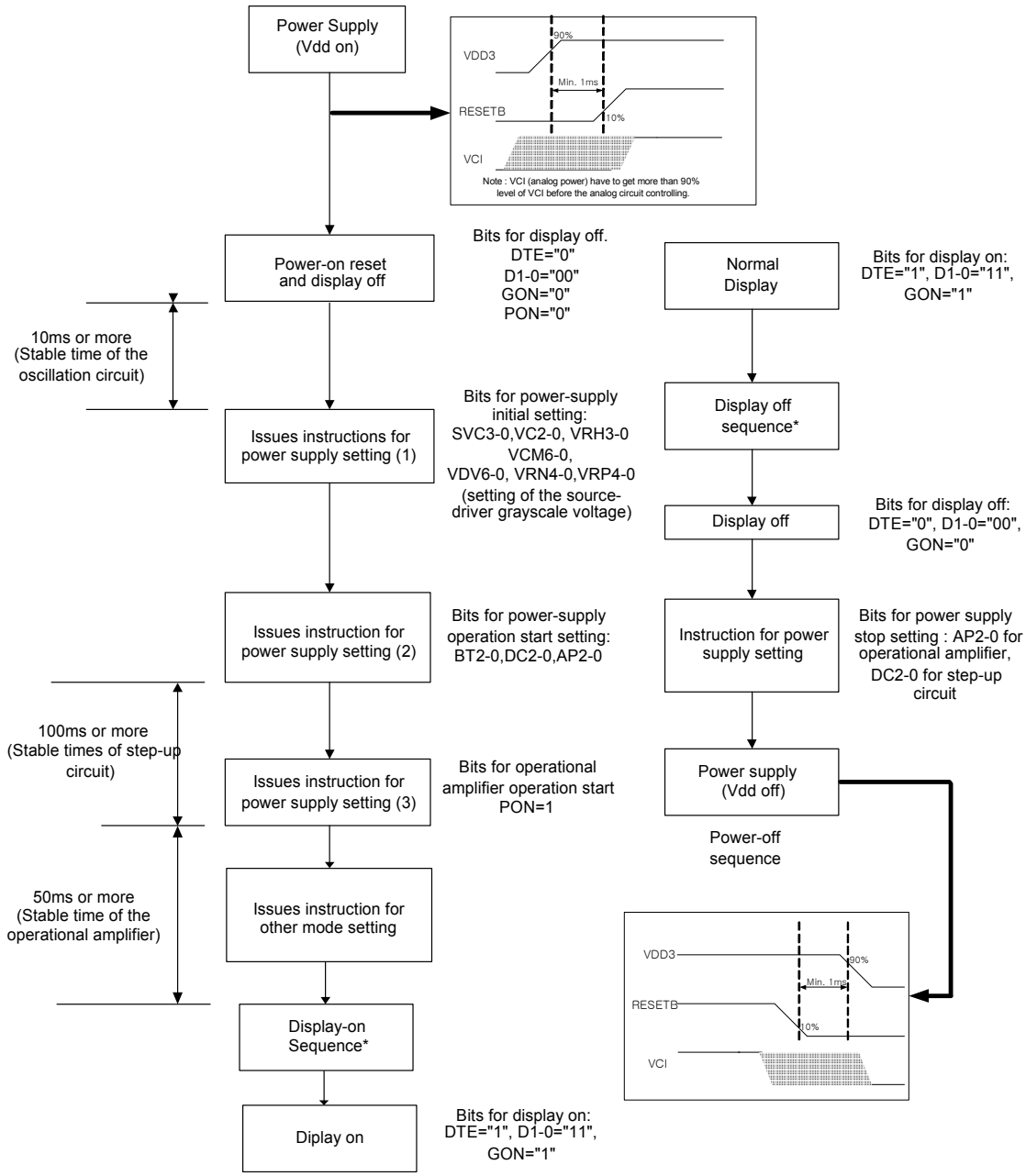


Figure 29 : Set up Flow of Power Supply

VOLTAGE REGULATION FUNCTION

The S6D0144 have internal voltage regulator. Voltage regulation function is controlled by DSTB signal.
If DSTB = “1”, voltage regulation is stopped. DSTB = “0” enables internal voltage regulation function.
By use of this function, internal logic circuit damage can be prohibited. Furthermore, power consumption also is obtained. Detailed function description and application setup is described in the following diagram.

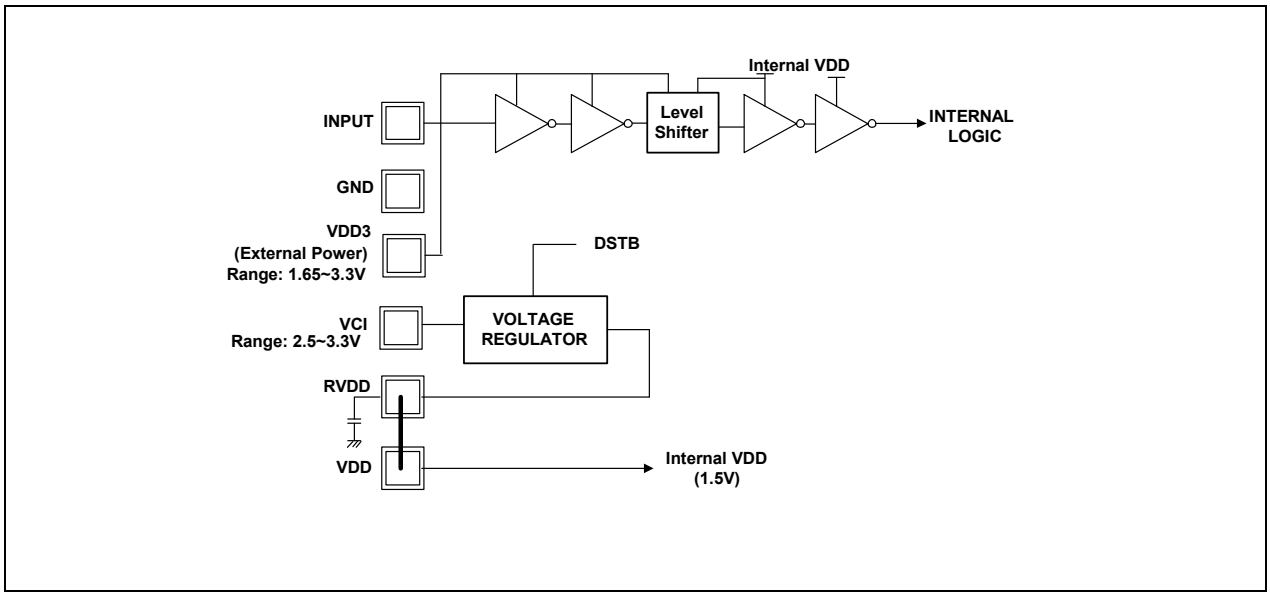


Figure 30 : Voltage regulation function

VCOM SETTING

The S6D0144 has 3 kind of VCOM amplitude adjusting method. It selects from external resistor setting, internal electronic volume setting, or MTP programmed setting.

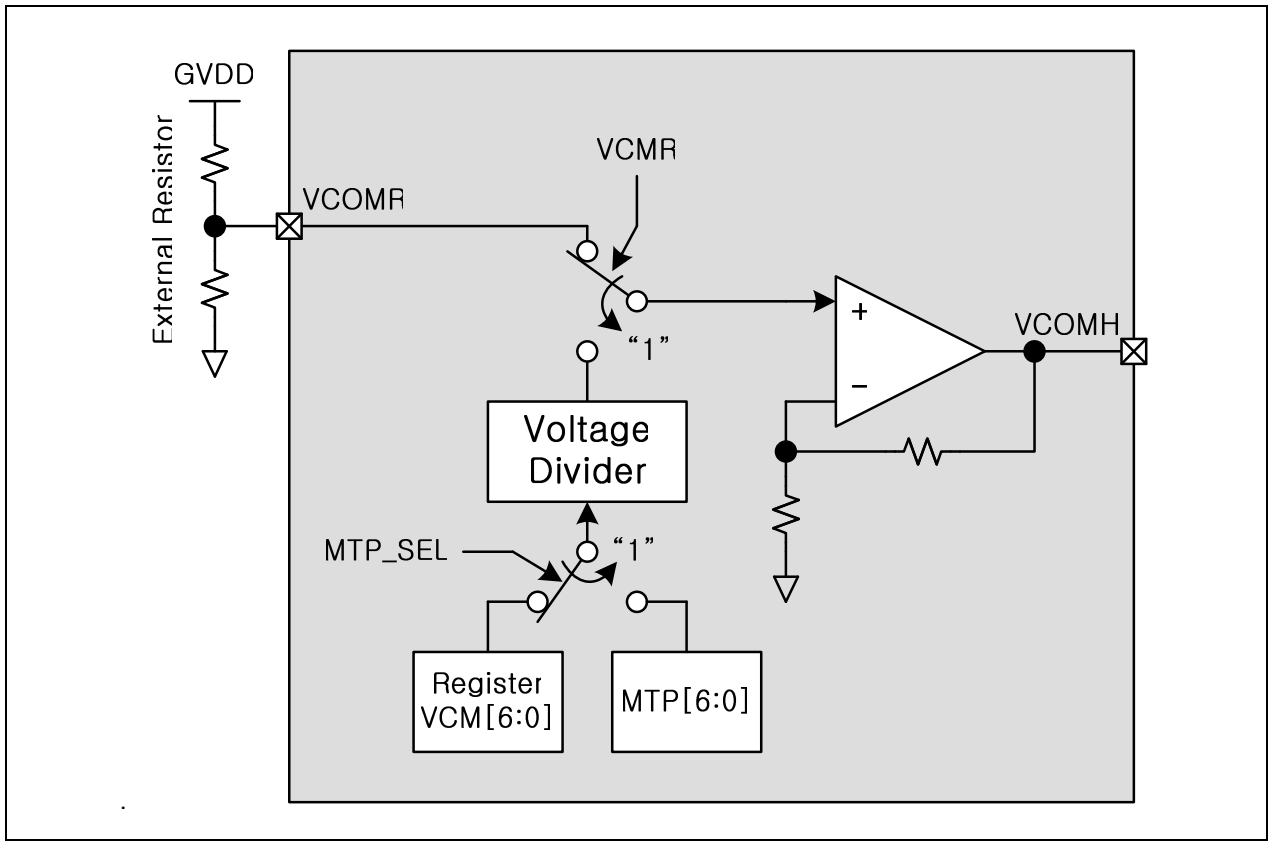


Figure 31 : VCOMH control function

INTERFACE SPECIFICATION

S6D0144 incorporates nine System Interfaces which are used to set instructions, and an RGB interface that is used to display motion pictures. Selecting one of these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

The External Clock Operation mode that uses RGB interface allows flicker-free screen update. In this mode, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for display operation. The data for display (DB[17:0]) is written according to the status of ENABLE in synchronization with VSYNC, HSYNC, and DOTCLK. In addition, using Window Address function enables rewriting only to the internal GRAM area to display motion pictures. Using this function also enables simultaneously display of motion picture and the GRAM data that was written earlier.

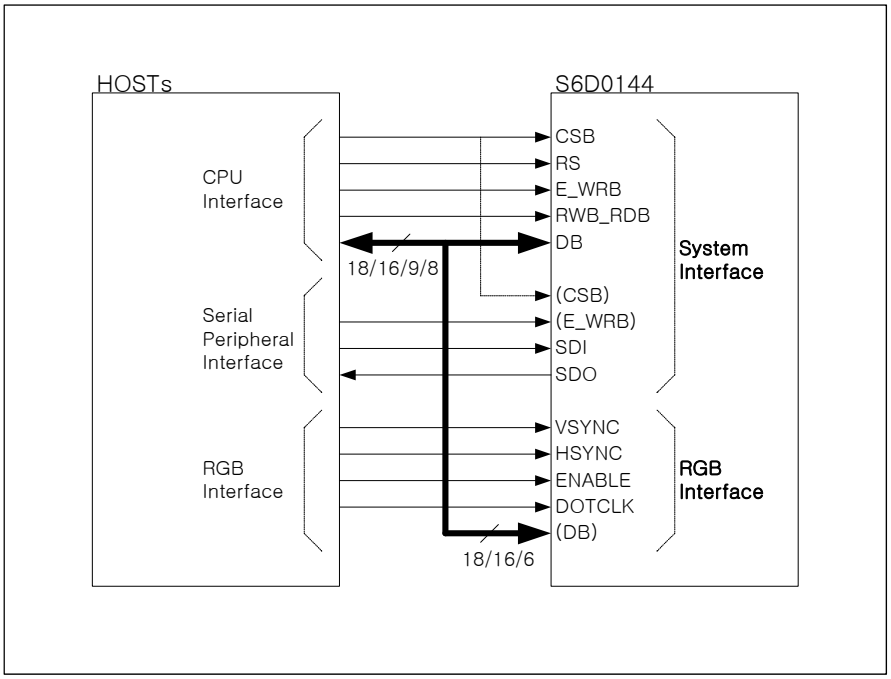


Figure 32 : System Interface and RGB Interface

SYSTEM INTERFACE

S6D0144 has nine System Interfaces as show below.

Table 61 : System Interfaces of S6D0144

No	Description
1	68x-System 18-bit bus interface
2	68x-System 16-bit bus interface
3	68x-System 9-bit bus interface
4	68x-System 8-bit bus interface
5	80x-System 18-bit bus interface
6	80x-System 16-bit bus interface
7	80x-System 9-bit bus interface
8	80x-System 8-bit bus interface
9	SPI (Serial Peripheral Interface)

In order to select one of them you should set IM[3:0] properly. For detail, see “PIN DESCRIPTION” described earlier.

68-18BIT CPU INTERFACE

Bit Assignment

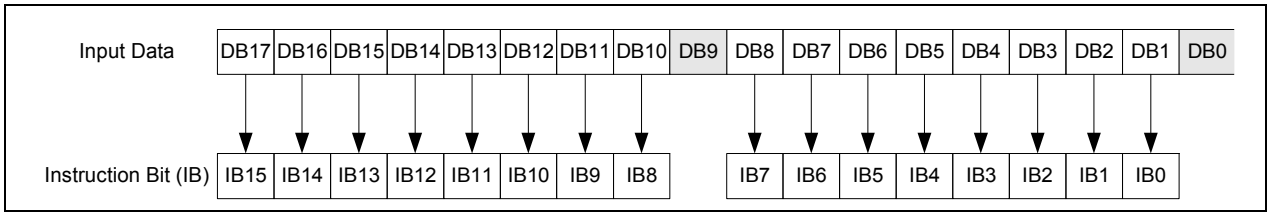


Figure 33 : Bit Assignment of Instructions on 68-18bit CPU Interface

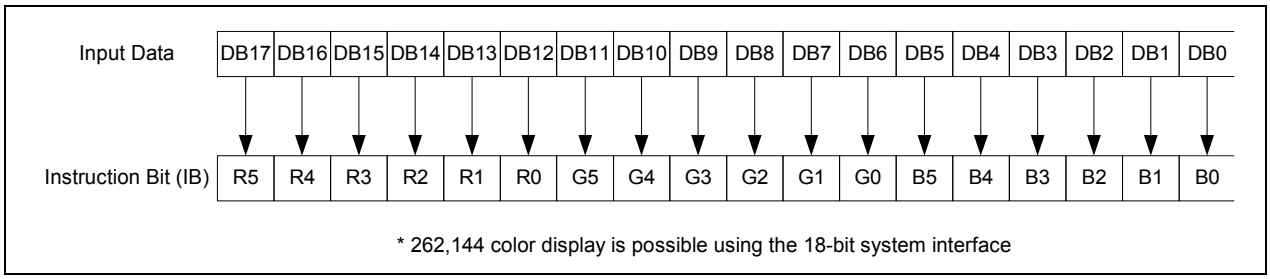


Figure 34 : Bit Assignment of GRAM Data on 68-18bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68 18-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

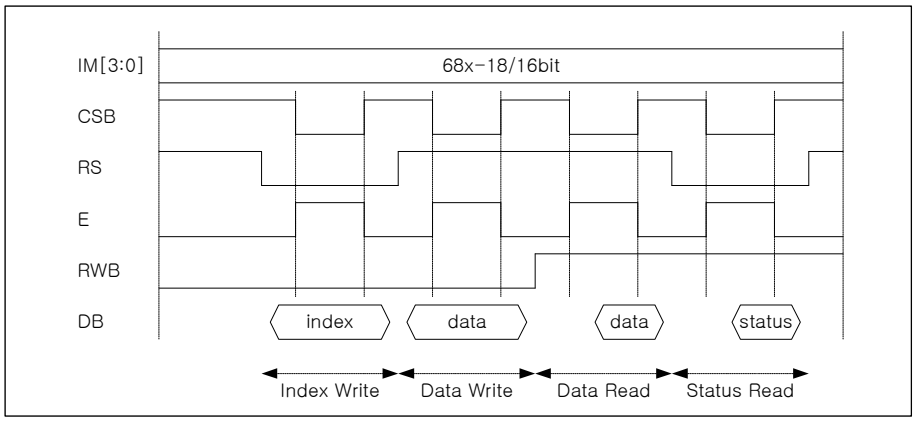


Figure 35 : Timing Diagram of 68-18bit CPU Interface

68-16BIT CPU INTERFACE

Bit Assignment

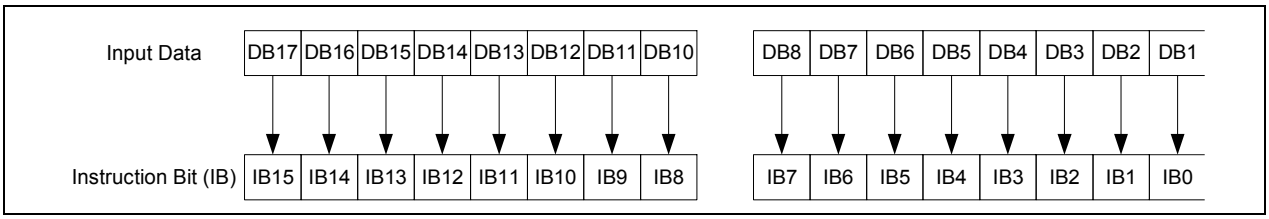


Figure 36 : Bit Assignment of Instructions on 68-16bit CPU Interface

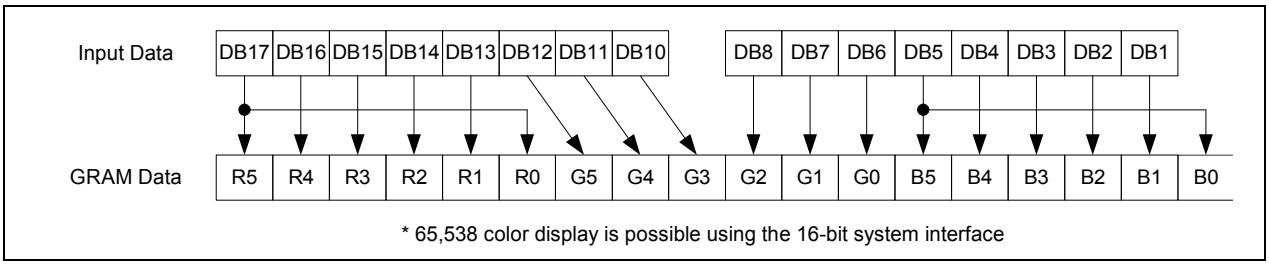


Figure 37 : Bit Assignment of GRAM Data on 68-16bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68-16bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

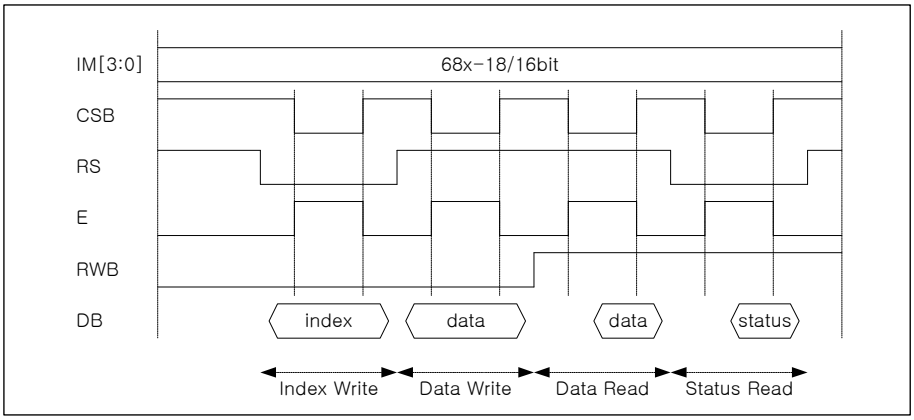


Figure 38 : Timing Diagram of 68-16bit CPU Interface

68-9BIT CPU INTERFACE

Bit Assignment

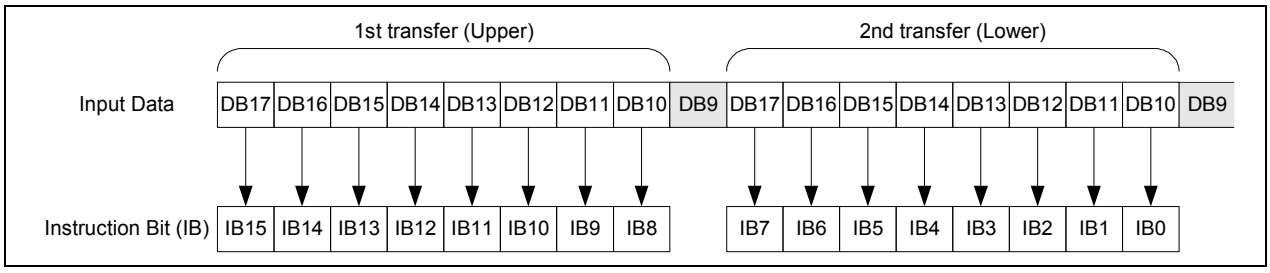


Figure 39 : Bit Assignment of Instructions on 68-9bit CPU Interface

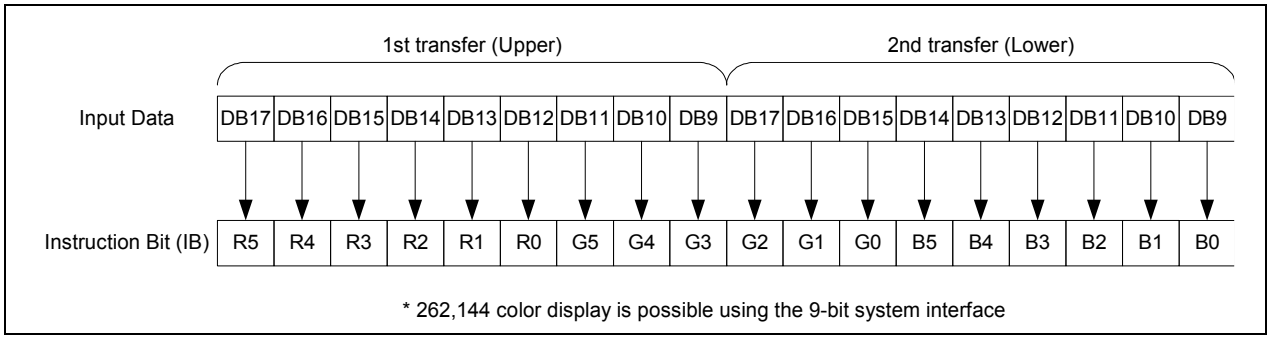


Figure 40 : Bit Assignment of GRAM Data on 68-9bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68-9bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

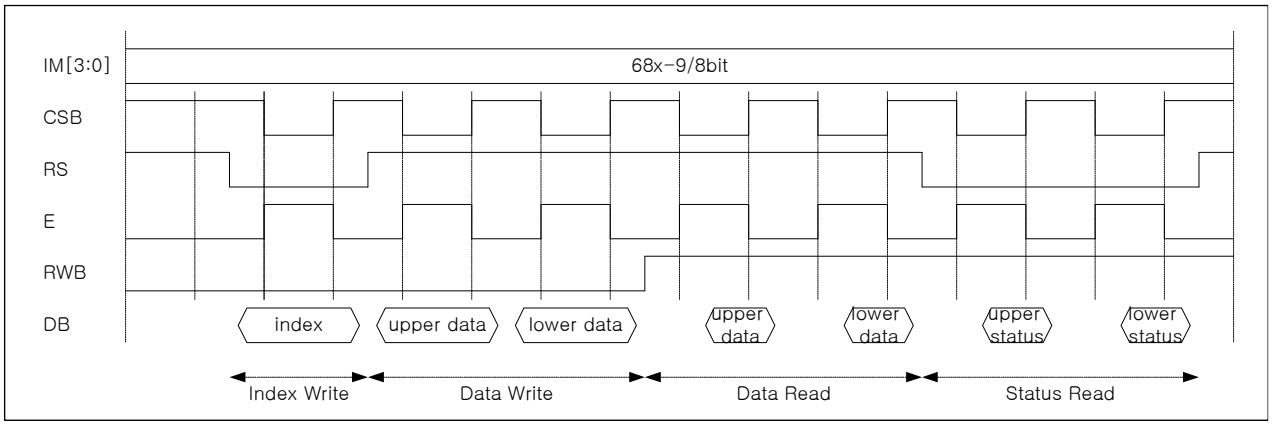


Figure 41 : Timing Diagram of 68-9bit CPU Interface

68-8BIT CPU INTERFACE

Bit Assignment

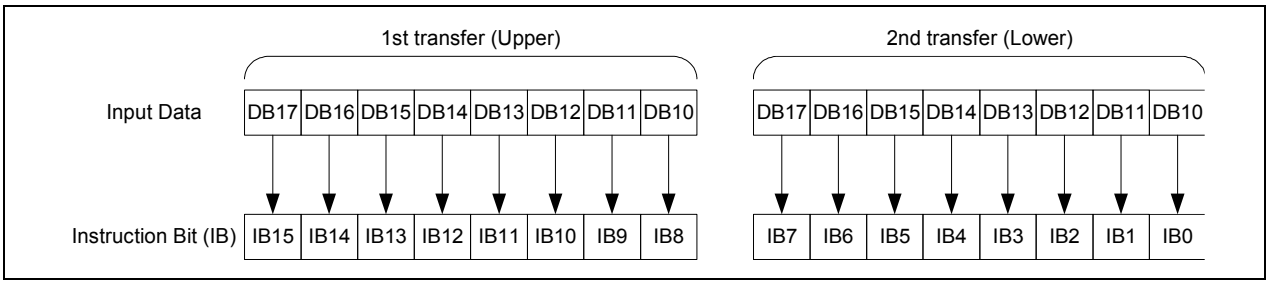


Figure 42 : Bit Assignment of Instructions on 68-8bit CPU Interface

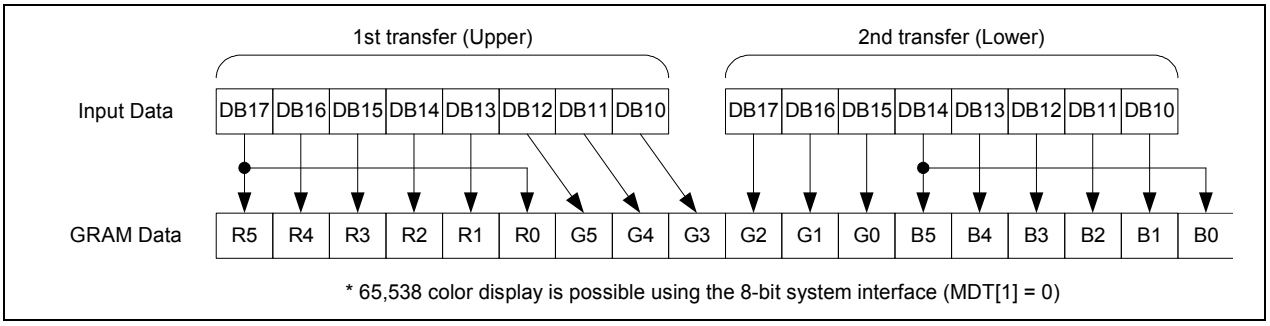


Figure 43 : Bit Assignment of GRAM Data on 68-8bit CPU Interface

Timing Diagram

There are 4 timing conditions for 68-8bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

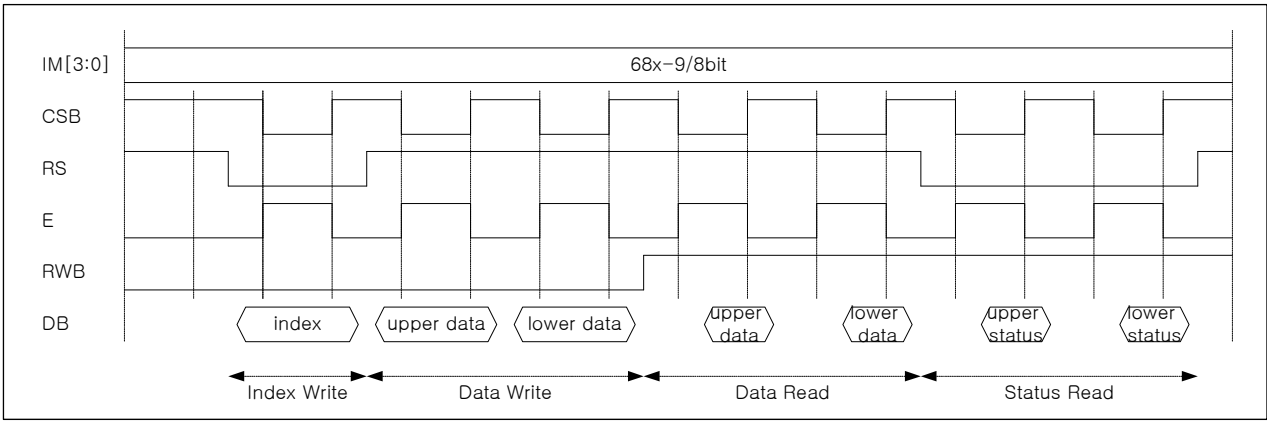


Figure 44 : Timing Diagram of 68-8bit CPU Interface

80-18BIT CPU INTERFACE

Bit Assignment

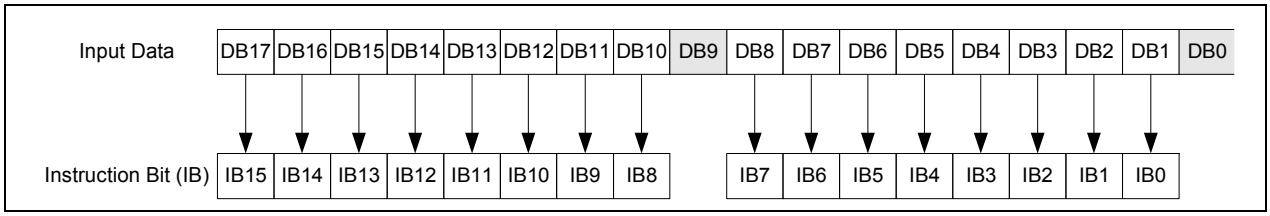


Figure 45 : Bit Assignment of Instructions on 80-18bit CPU Interface

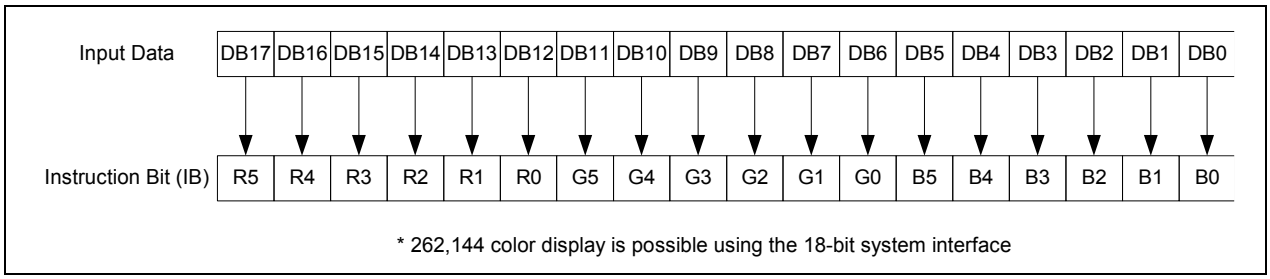


Figure 46 : Bit Assignment of GRAM Data on 80-18bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80 18-bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

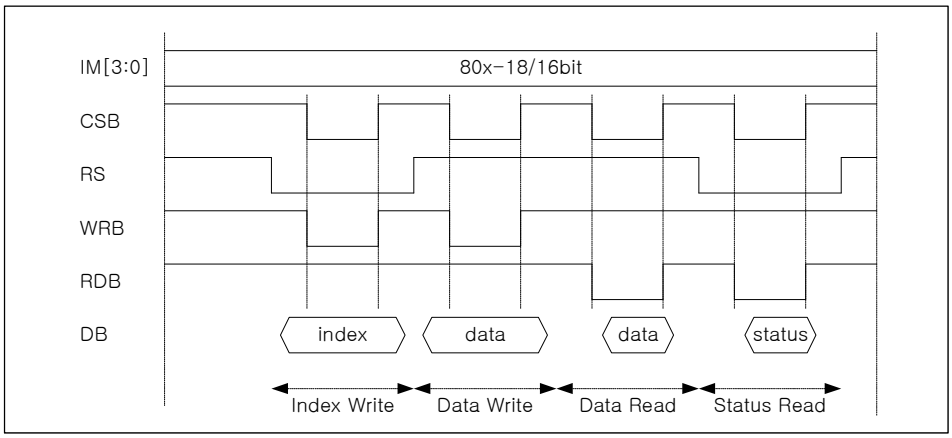


Figure 47 : Timing Diagram of 80-18bit CPU Interface

80-16BIT CPU INTERFACE

Bit Assignment

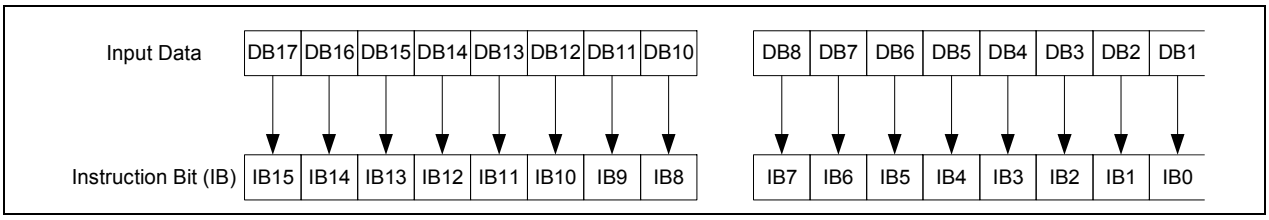


Figure 48 : Bit Assignment of Instructions on 80-16bit CPU Interface

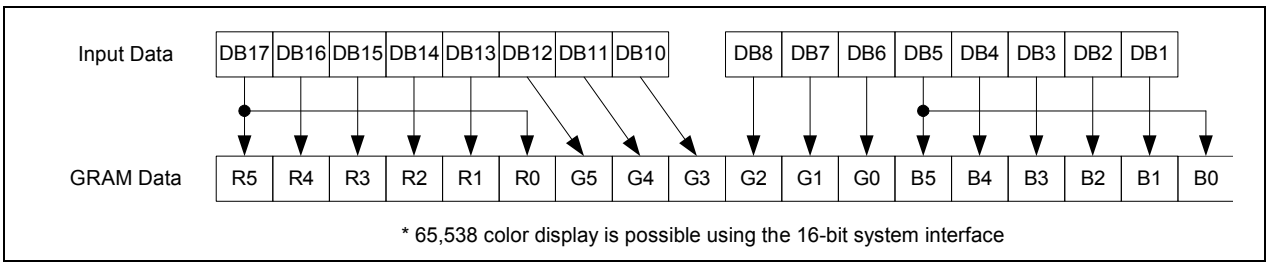


Figure 49 : Bit Assignment of GRAM Data on 80-16bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80-16bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.

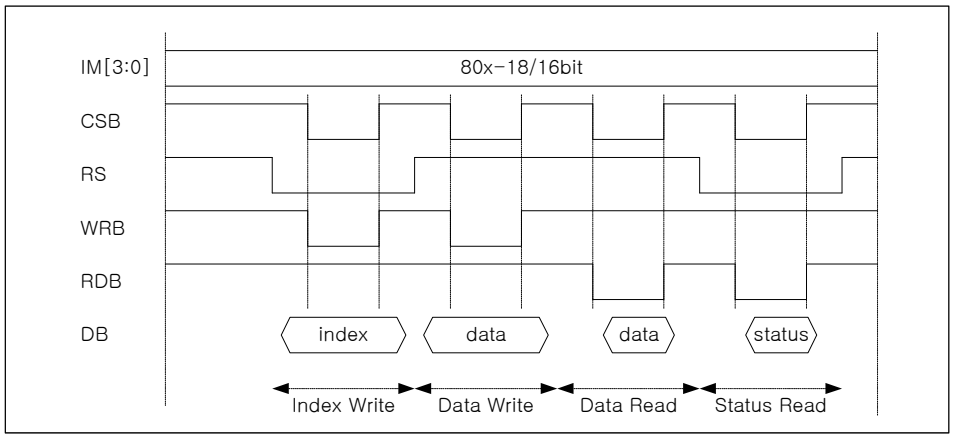


Figure 50 : Timing Diagram of 80-16bit CPU Interface

80-9BIT CPU INTERFACE

Bit Assignment

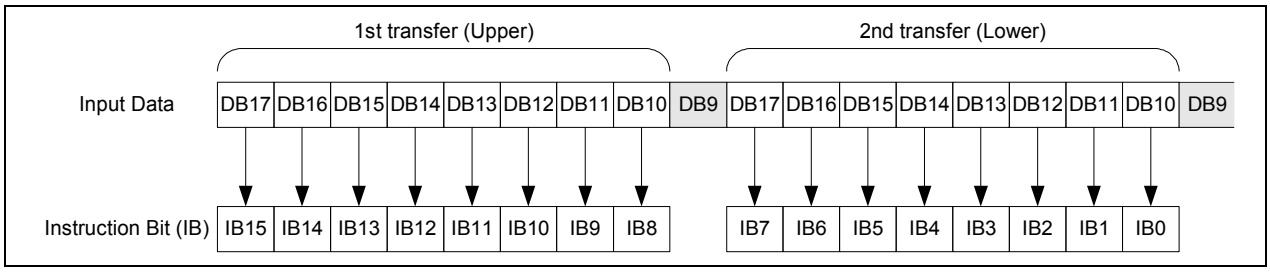


Figure 51 : Bit Assignment of Instructions on 80-9bit CPU Interface

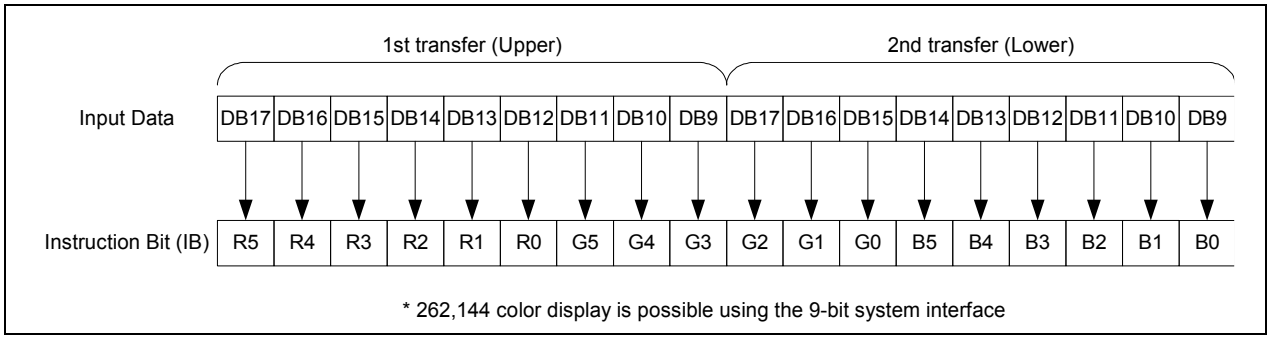


Figure 52 : Bit Assignment of GRAM Data on 80-9bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80-9bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

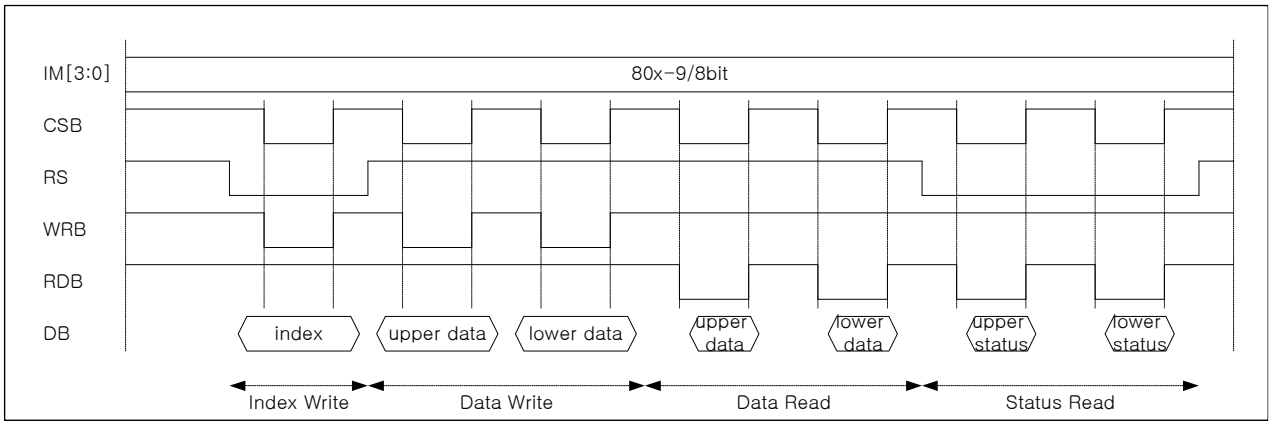


Figure 53 : Timing Diagram of 80-9bit CPU Interface

80-8BIT CPU INTERFACE

Bit Assignment

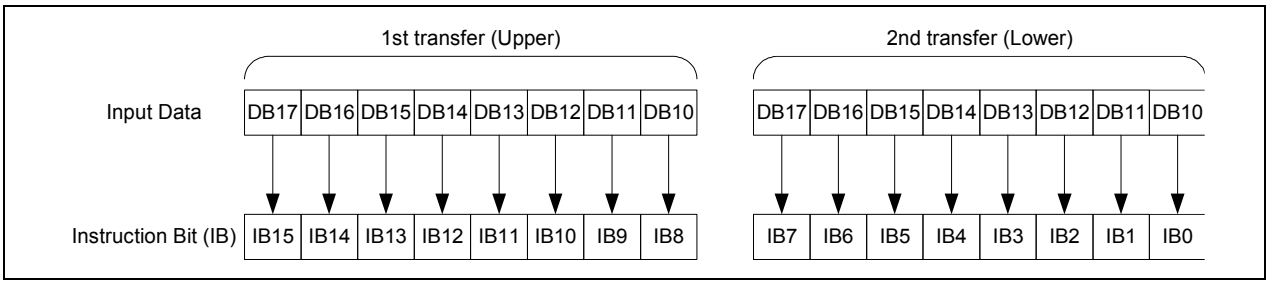


Figure 54 : Bit Assignment of Instructions on 80-8bit CPU Interface

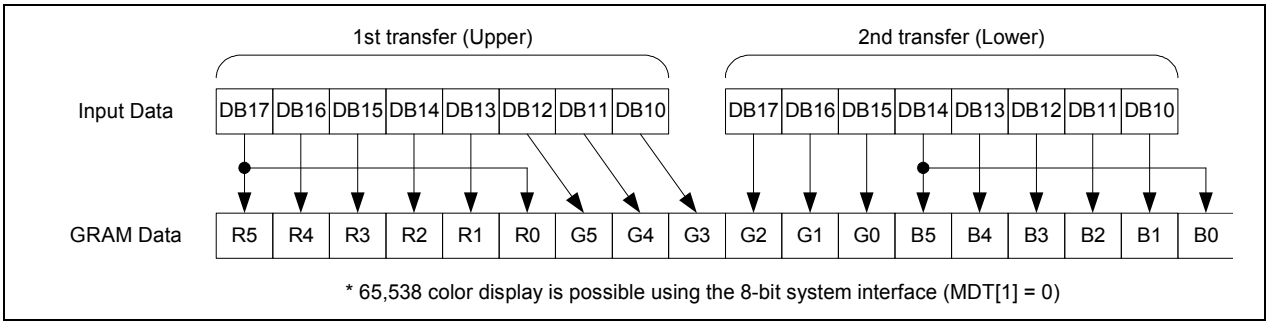


Figure 55 : Bit Assignment of GRAM Data on 80-8bit CPU Interface

Timing Diagram

There are 4 timing conditions for 80-8bit CPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.
In this mode, 16-bit instructions and GRAM data are divided into two half words and the transfer starts from the upper half word.

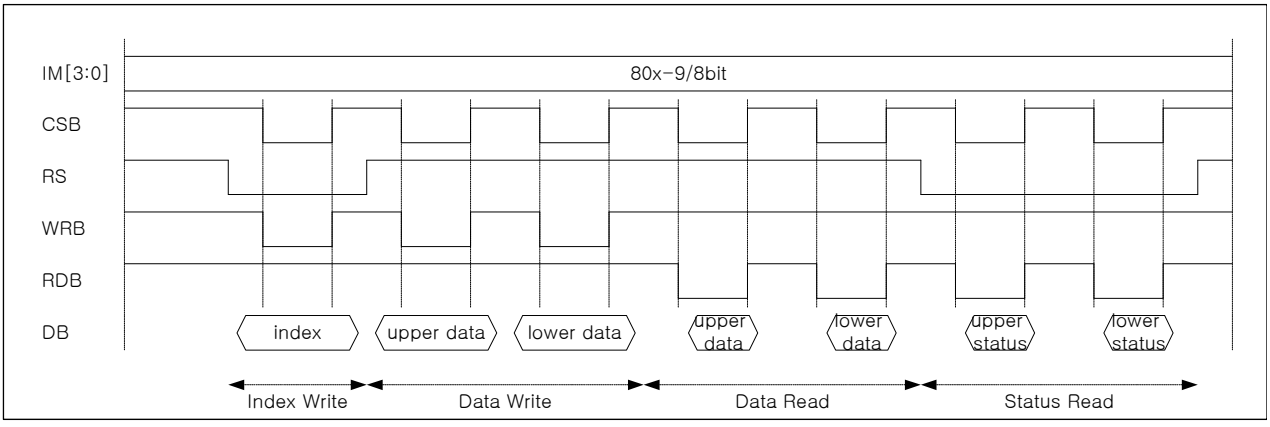


Figure 56 : Timing Diagram of 80-8bit CPU Interface

SERIAL PERIPHERAL INTERFACE

Setting IM[3:0] properly allows standard clock-synchronized serial data transfer (SPI ; Serial Peripheral Interface), using CSB (chip select), SCL (serial transfer clock), SDI (serial input data) and SDO (serial output data). For the serial interface, IM[0] is used as ID.

S6D0144 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

S6D0144 is selected when the 6-bit chip address in the start byte transferred by the transmitting device matches the 6-bit device identification code assigned to S6D0144. ID is the least significant bit of the device identification code. S6D0144, when selected, receives the subsequent data string.

Two different chip addresses must be assigned to a single S6D0144 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = “0”, data can be written to the index register or status can be read, and when RS = “1”, an instruction can be issued or data can be written to or read from GRAM. Read or write is determined according to the eighth bit of the start byte (R/WB bit). The data is written (receives) when the R/WB bit is “0”, and is read (transmits) when the R/WB bit is “1”.

After receiving the start byte, S6D0144 receives or transmits the subsequent data. The data is transferred with the MSB first. All S6D0144 instructions are 16 bits, so two bytes are received with the MSB first (DB15 to 0), and then the instruction is internally executed.

Five bytes of GRAM data read just after the start byte are invalid. S6D0144 starts to read correct GRAM data from the sixth byte. Likewise, it starts to read correct register/status from the second byte.

Table 62 : Start Byte Format

Transfer Bit	1st	2nd	3rd	4th	5th	6th	7th	8th
Start byte format	Device Identification code						RS	RWB
	0	1	1	1	0	ID		

[NOTE] The IM[0] pin is used as ID

Table 63 : RS and RWB Bit Function

RS bit	RWB bit	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

Bit Assignment

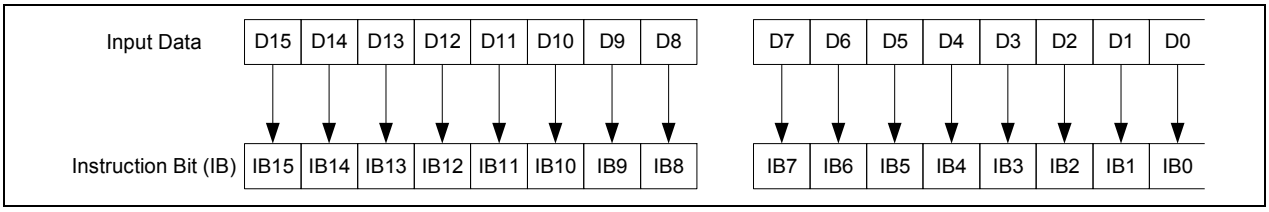


Figure 57 : Bit Assignment of Instructions on SPI

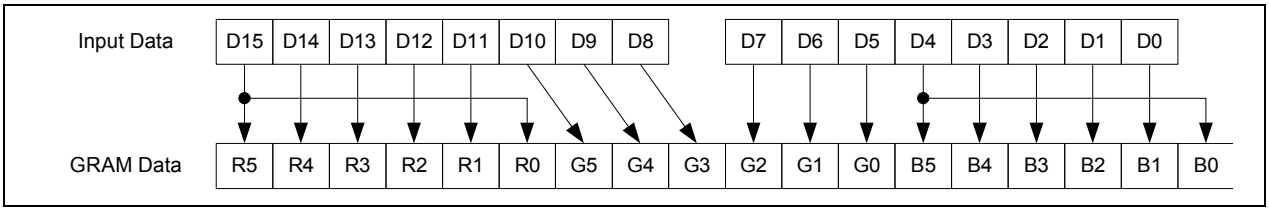


Figure 58 : Bit Assignment of GRAM Data on SPI

Timing Diagrams

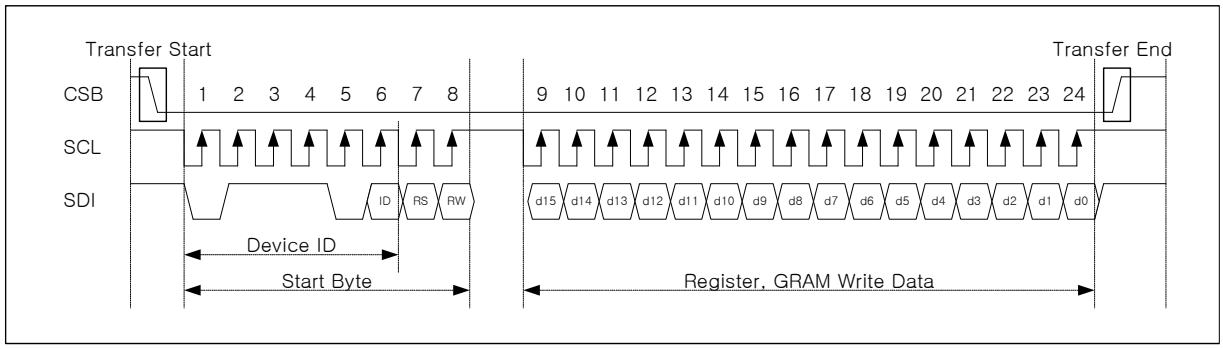


Figure 59 : Basic Timing Diagram of Data Transfer through SPI

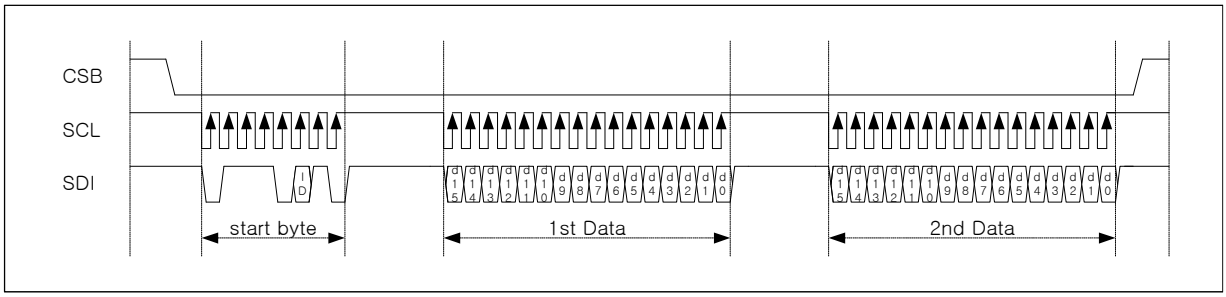


Figure 60 : Timing Diagram of Consecutive Data-Write through SPI

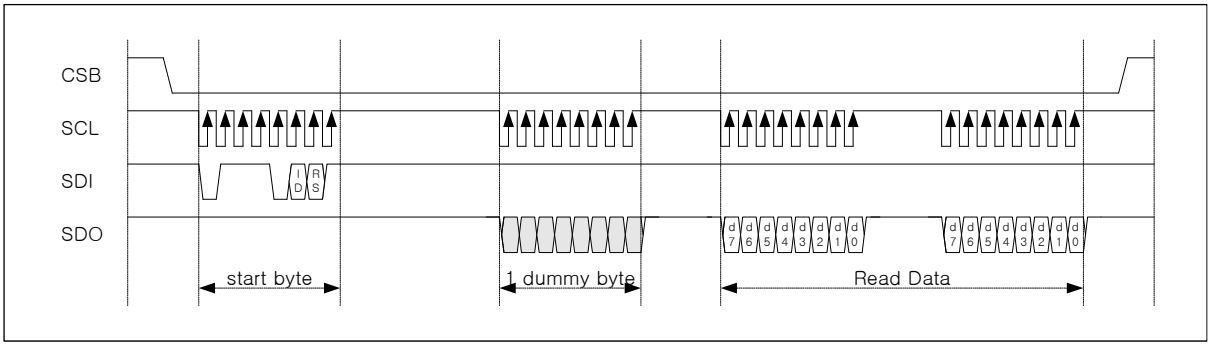


Figure 61 : Timing Diagram of Register / Status Read through SPI

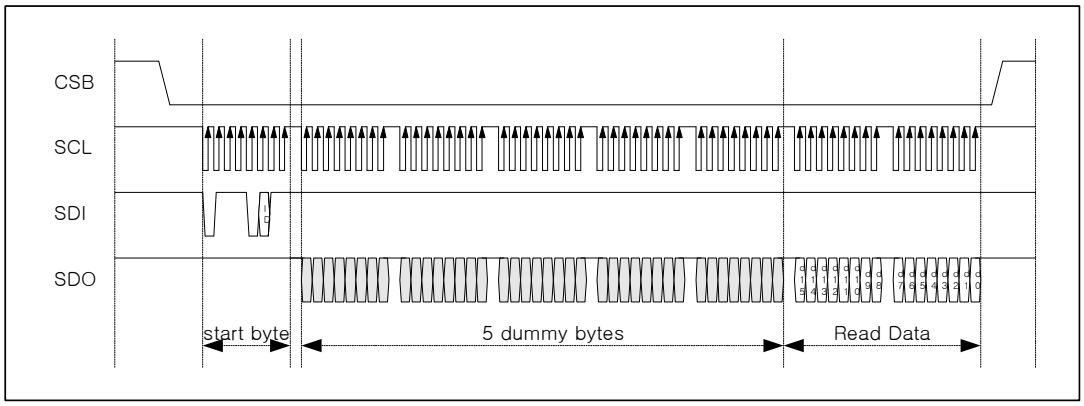


Figure 62 : Timing Diagram of GRAM-Data Read through SPI

RGB INTERFACE

MOTION PICTURE DISPLAY

S6D0144 incorporates RGB interface to display motion pictures and GRAM to store data for display.
To display motion pictures, S6D0144 has the following features.
- Only motion picture area can be transferred by the Window Address function.
- Only motion picture area to be rewritten can be transferred selectively.
- Reducing the amount of data transferred enables reduce the power consumption of the whole system.
- Still picture area, such as an icon, can be updated while displaying motion pictures combining with the system interface (for details, refer to “GRAM ACCESS VIA RGB INTERFACE AND SPI” described later).

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK.
Window Address Function enables transfer only the screen to be updated and reduce the power consumption.

In the period between the completion of displaying one frame data and the next VSYNC signal, the display status will remain in front porch period.

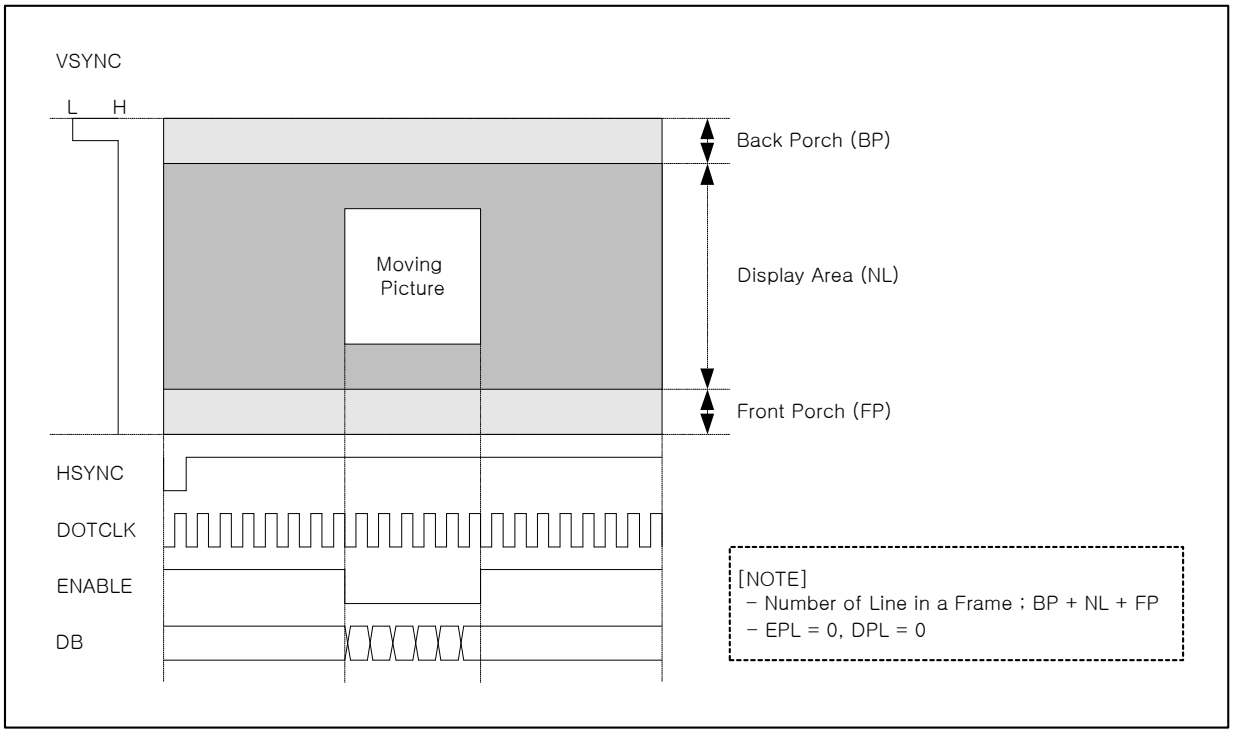


Figure 63 : RGB Interface

[NOTE] For RGB interface, VSYNC, HSYNC, DOTCLK should be supplied at much higher resolution than that of panel.

There are three timing conditions for RGB Interface that is determined according to RIM and each condition is described below.

18BIT RGB INTERFACE

Bit Assignment

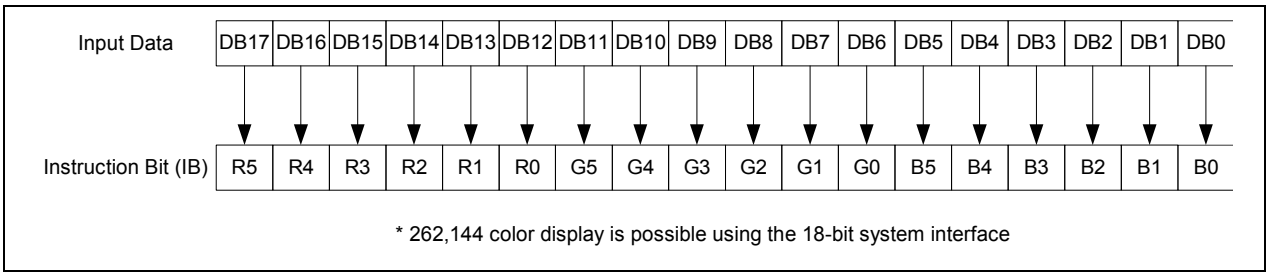


Figure 64 : Bit Assignment of GRAM Data on 18bit RGB Interface

Timing Diagram

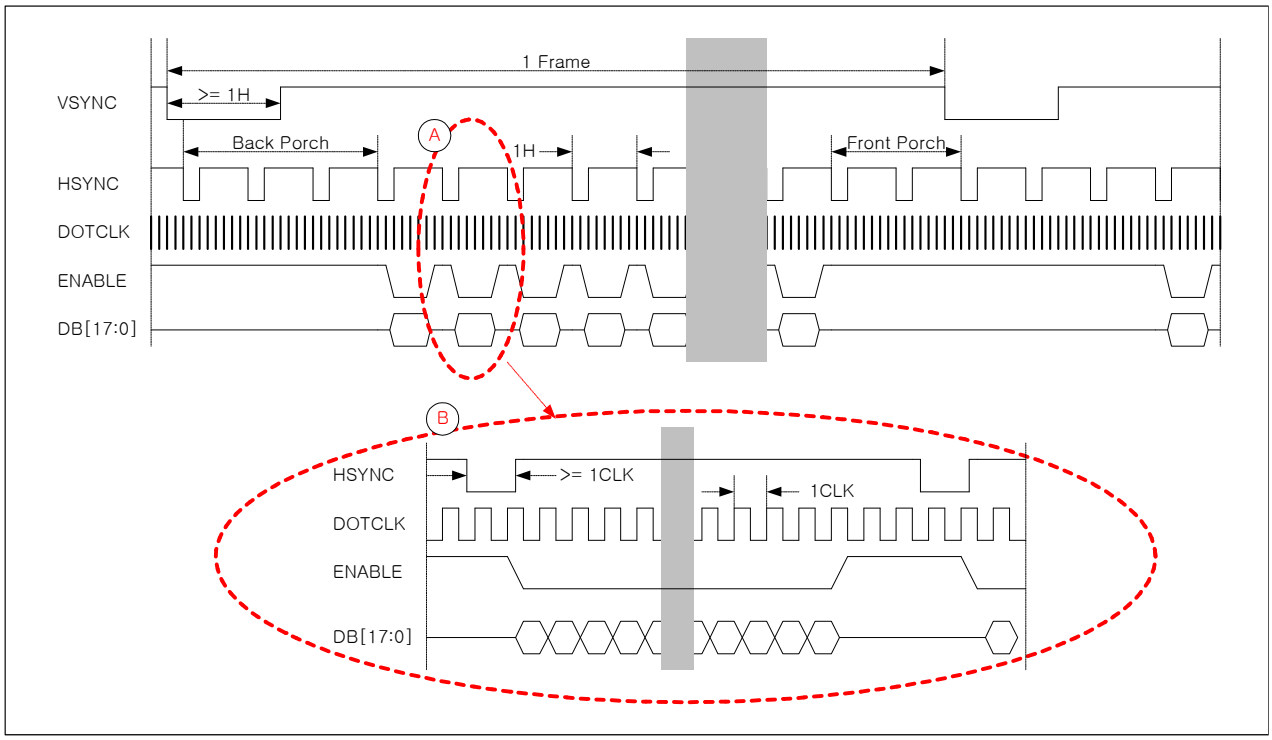


Figure 65 : Timing Diagram of 18/16bit RGB Interface

16BIT RGB INTERFACE

Bit Assignment

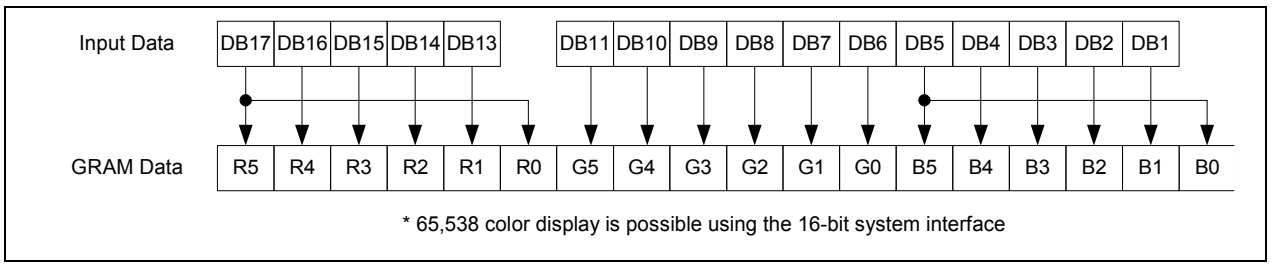


Figure 66 : Bit Assignment of GRAM Data on 16bit RGB Interface

Timing Diagram

There are two timing conditions for RGB Interface that is determined according to RIM.

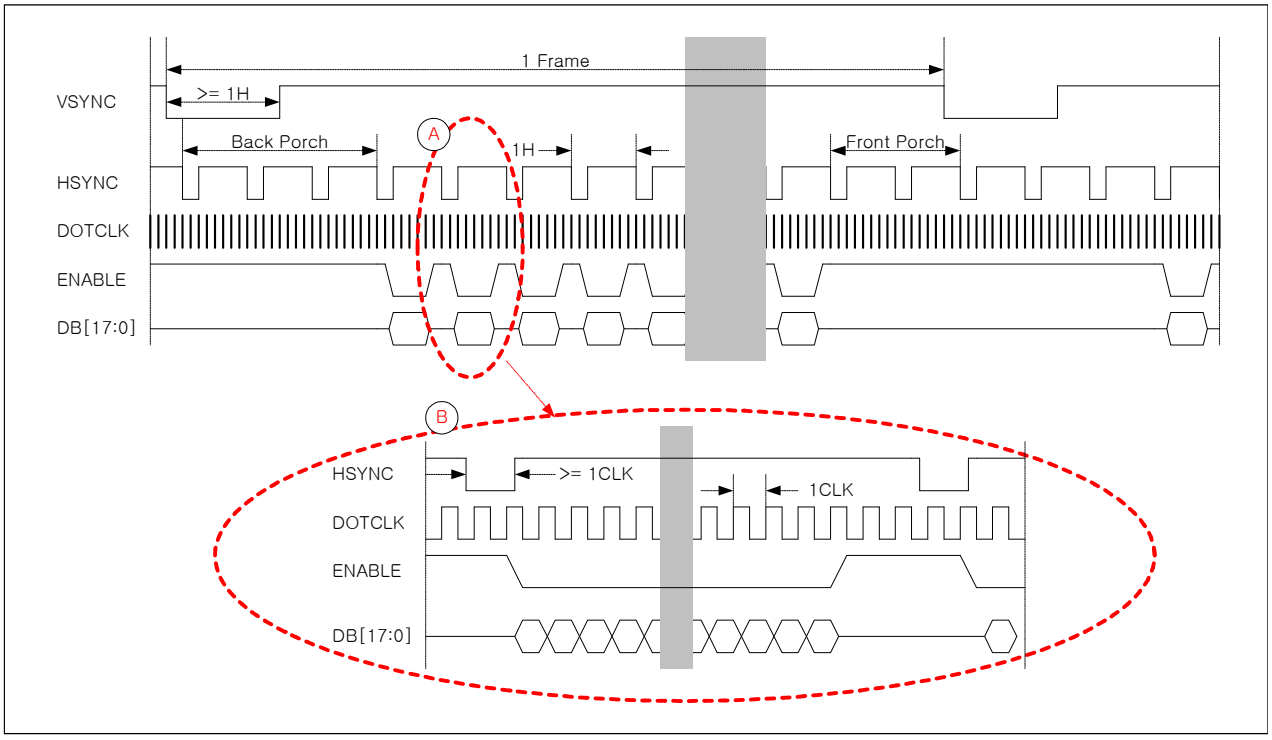


Figure 67 : Timing Diagram of 18/16bit RGB Interface

6BIT RGB INTERFACE

In order to transfer data on 6bit RGB Interface there should be three transfers.

Bit Assignment

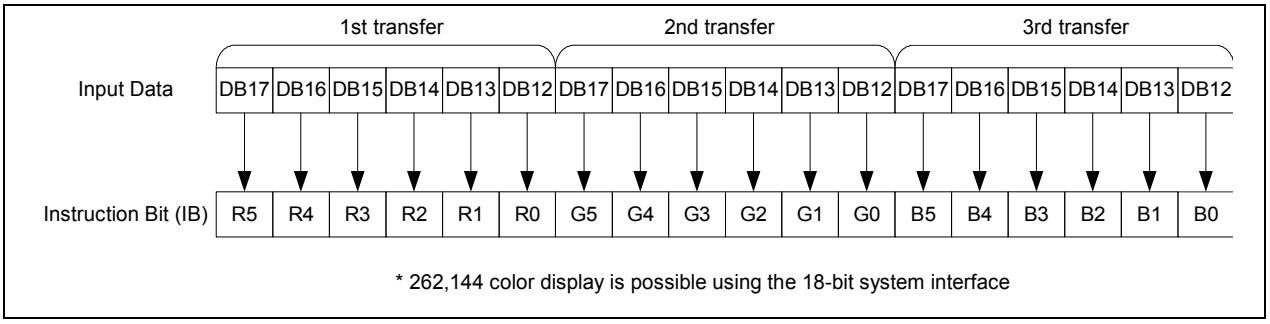


Figure 68 : Bit Assignment of GRAM Data on 6bit RGB Interface

Timing Diagram

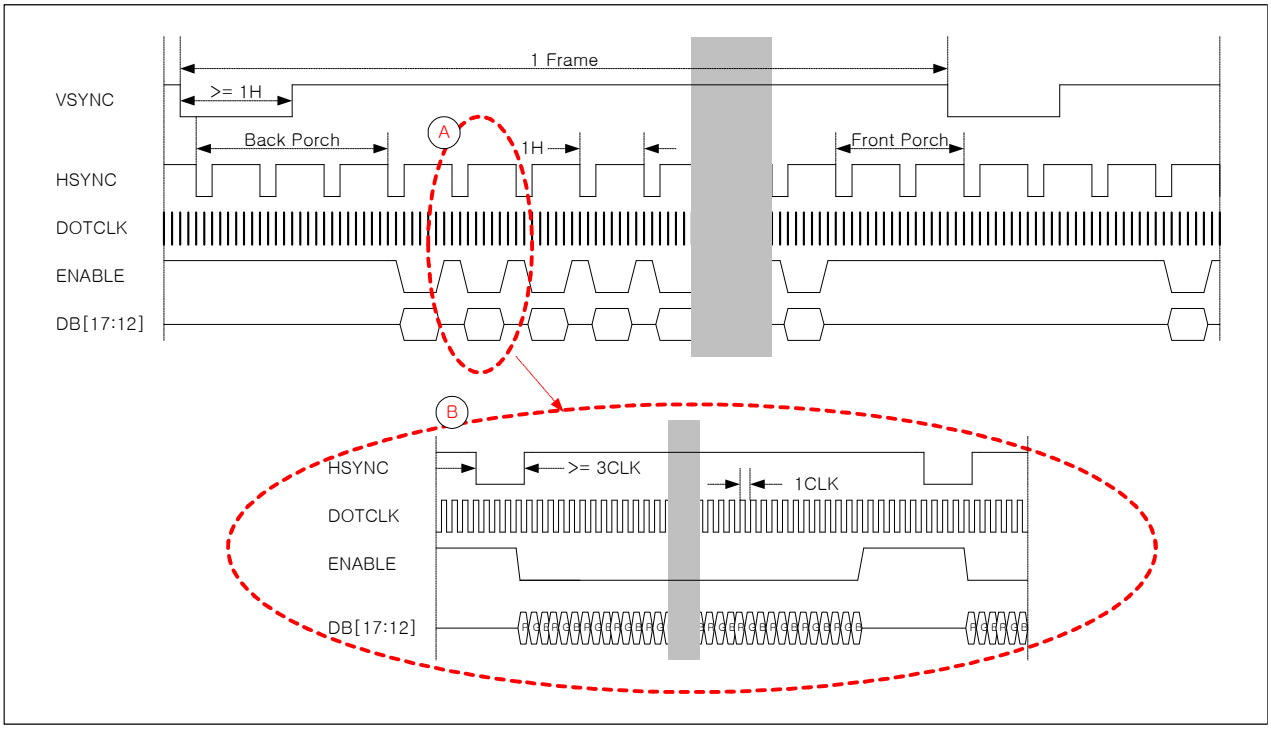


Figure 69 : Timing Diagram of 6bit RGB Interface

[NOTES] 1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.
2. VSYNC, HSYNC, ENABLE, DOTCLK, and DB[17:12] should be transferred in units of three clocks.

Transfer Synchronization

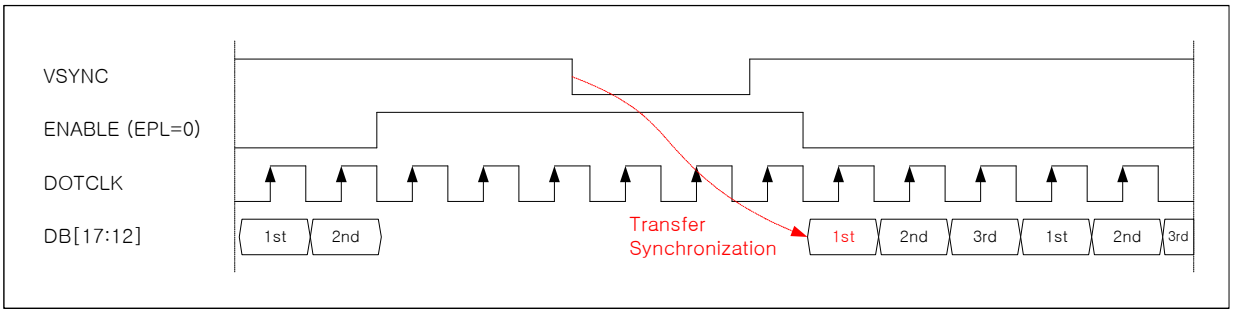


Figure 70 : Transfer Synchronization Function in 6-bit RGB Interface mode

NOTE: The figure above shows Transfer Synchronization function for 6bit RGB Interface. S6D0144 has a transfer counter internally to count 1st, 2nd and 3rd data transfer of 6bit RGB Interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected at every VSYNC signal assertion. In this method, when data is consecutively transferred in for displaying motion pictures, the effect of transfer mismatch will be reduced and recovered by normal operation.

NOTE: The internal display is operated in units of three DOTCLKs. When DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame are not displayed correctly.

INTERFACE SWAPPING FOR MEMORY ACCESS

DISPLAY MODES AND GRAM ACCESS CONTROL

Display mode and RAM Access is controlled as shown below. For each display status, display mode control and RAM Access control are combined properly.

Table 64 : DISPLAY MODE & RAM ACCESS CONTROL

Display Status	GRAM Access (RM)	Display Mode (DM)
1. Still Picture Display	System Interface (RM = 0)	Internal Clock Operation (DM[1:0] = 00)
2. Motion Picture Display	RGB Interface (RM = 1)	External Clock Operation (DM[1:0] = 01)
3. Rewrite Still Picture while Motion Picture is being displayed	System Interface (RM = 0)	External Clock Operation (DM[1:0] = 01)

[NOTE 1] Only system interface can set Instruction register.
[NOTE 2] When the RGB Interface is being operated do not change the RGB Interface mode (RIM).

Internal Clock Operation mode with System Interface (1)

Every operation in Internal Clock Operation mode is done in synchronization with the internal clock which is generated by internal OSC. The signals input through RGB interface are all meaningless. Access to internal GRAM is done via system interface.

External Clock Operation mode with RGB Interface (2)

In External Clock Operation mode, frame sync signal (VSYNC), line sync signal (HSYNC) and DOTCLK are used for display operation. Display data is transferred in the unit of pixel through DB bus and saved to GRAM.

External Clock Operation mode with System Interface (3)

Write GRAM data via system interface even in External Clock Operation mode. There should not be any data transmission on RGB interface in this case. To restart data transmission on RGB interface, set RM to “1”, set memory address properly and write index of 22h for GRAM write operation.

With the combination of Window Address function, motion picture and still picture may be saved in separated GRAM regions respectively. In this case motion picture and still picture are displayed simultaneously.

GRAM ACCESS VIA RGB INTERFACE AND SPI

All the data for display is written to the internal GRAM in S6D0144 when RGB interface is in use. In this method, data, including motion picture and screen update frame, can only be transferred via RGB interface.

With Window Address function, power consumption can be reduced and high-speed access can be achieved while motion pictures are being displayed. Data for display that is not in the motion picture area or the screen update frame can be written via System Interface.

GRAM can be accessed via SPI even when RGB interface is in use. To do that ENABLE should be inactive state to stop data writing via RGB interface, because the write operation to GRAM is always performed in synchronization with DOTCLK while ENABLE is active state. Then you may write any data through SPI. After this access to GRAM via SPI, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, data writing is not guaranteed.

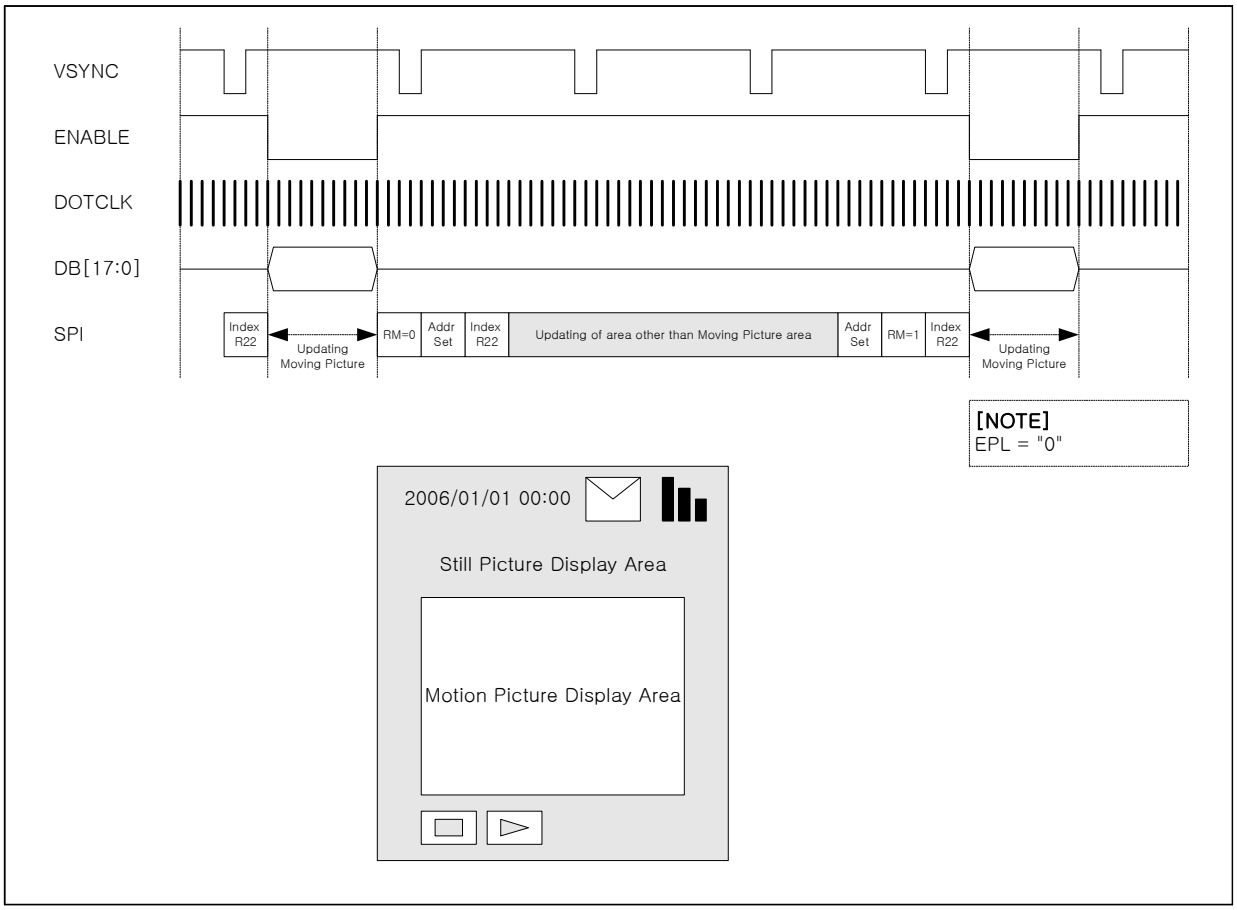


Figure 71 : GRAM Access through RGB Interface and SPI

TRANSITION SEQUENCES BETWEEN DISPLAY MODES

Transitions between Internal Clock Operation mode and External Clock Operation mode should follow the mode transition sequence shown below.

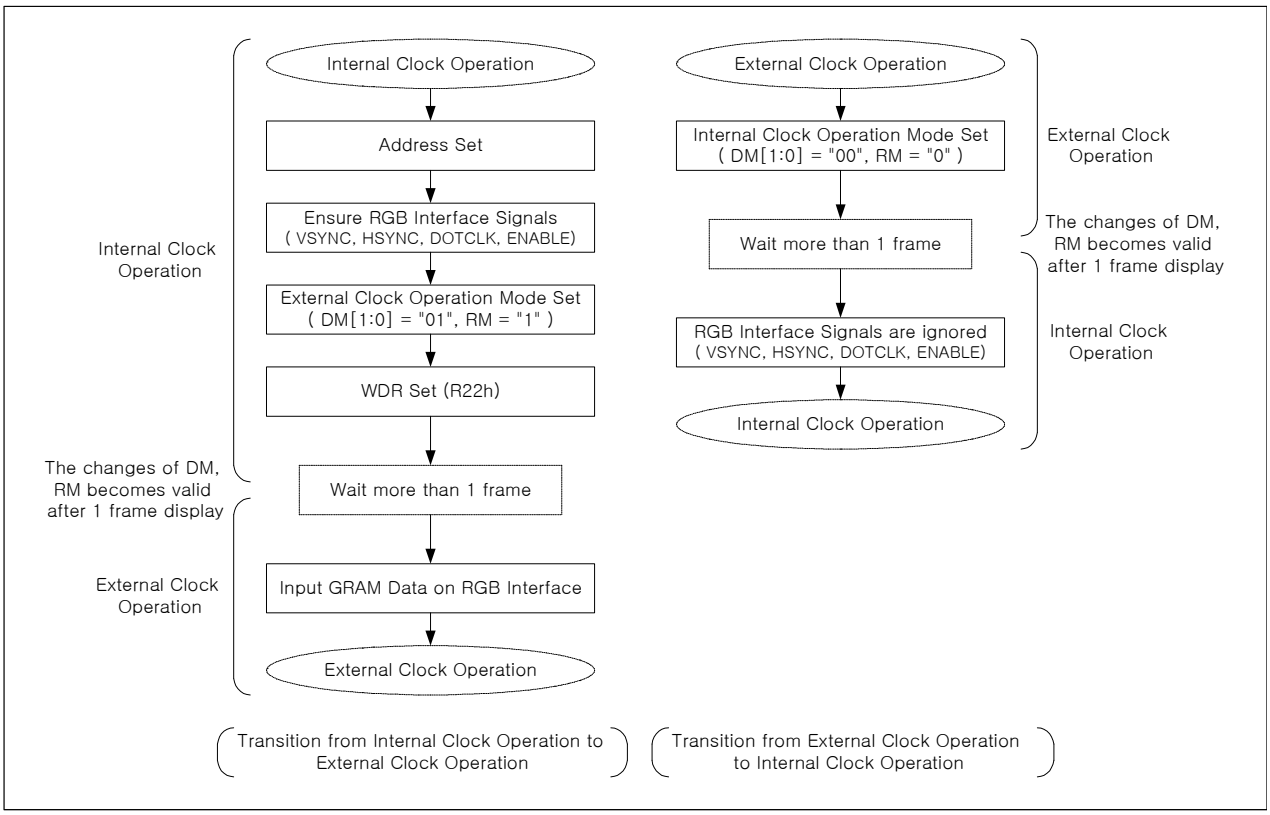


Figure 72 : Transition between Internal Clock Operation Mode and External Clock Operation Mode

PANEL CONTROL INTERFACE

INTERCONNECTION BETWEEN PANEL AND S6D0144

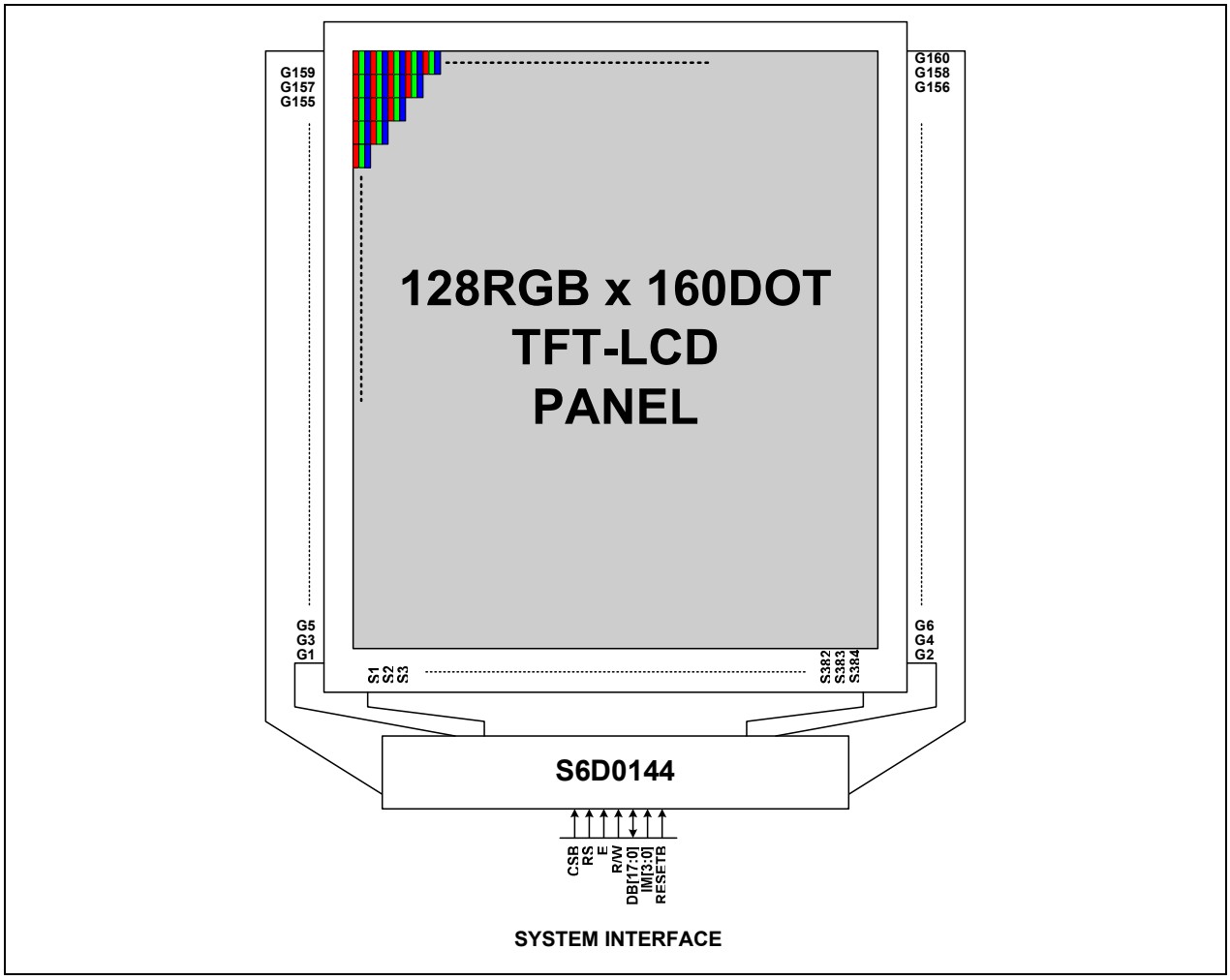


Figure 73 : System structure

TIMING DIAGRAMS

Frame Inversion & Line Inversion

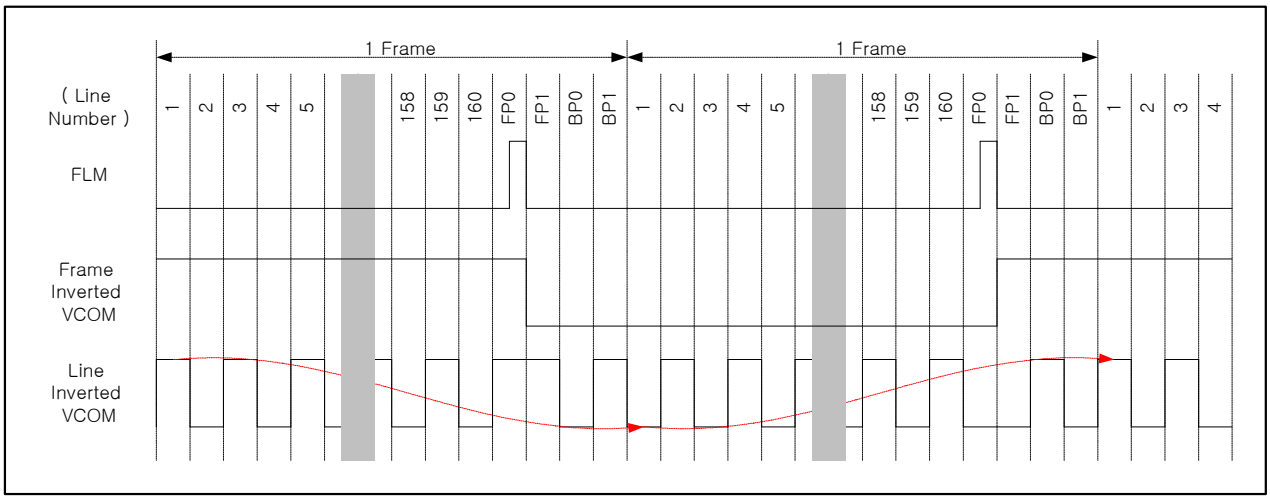
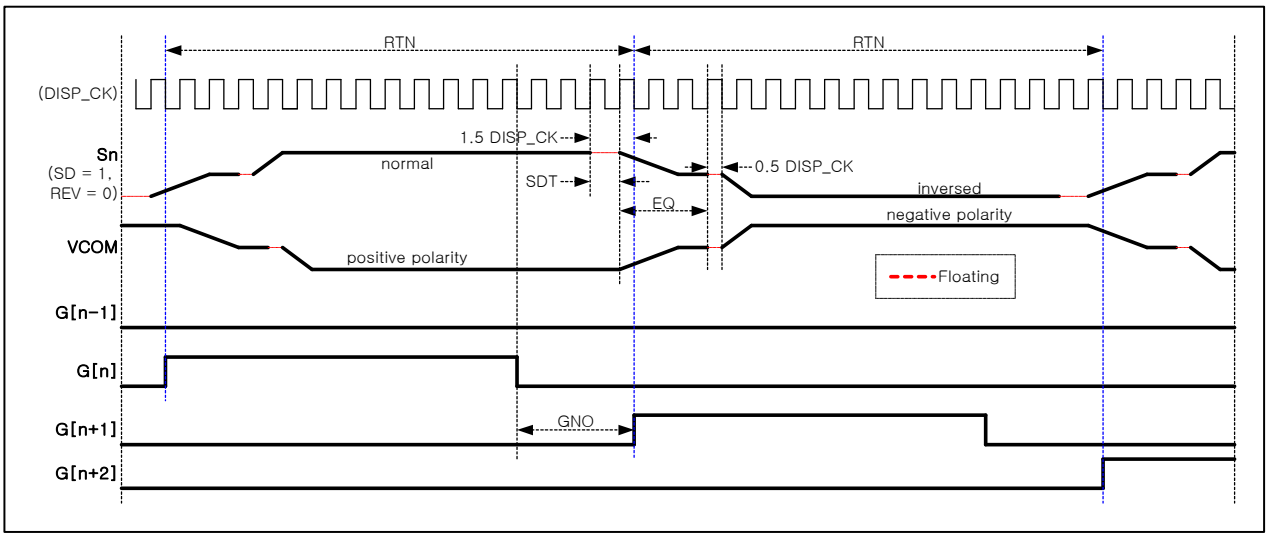


Figure 74 : VCOM waveforms and LCD inversion (BP = 2, FP = 2)

Source Output & Gate Clock



[NOTE] DISP_CK : OSCK_CK divided by DIV[1:0](DM = 2'b00) or DOTCLK divided by 8(DM = 2'b01 and RIM[1] = 1'b1)

Figure 75 : Source Output & Gate Clock Timing (EQ = 2'b11, GNO = 2'b01, DIV = 2'b00)

Interlaced Scanning Function

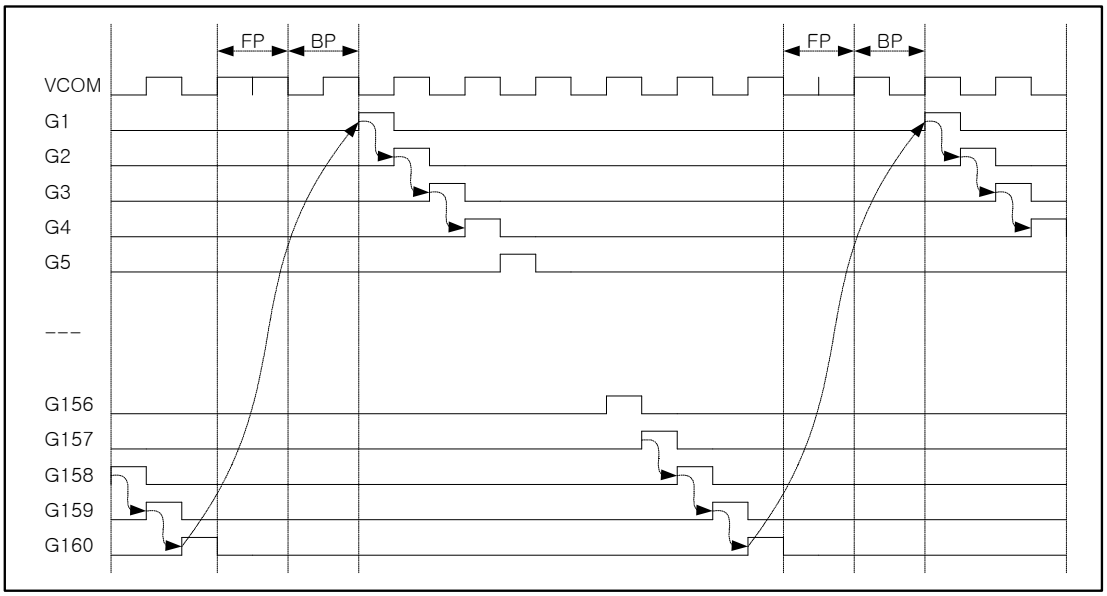


Figure 76 : normal scanning method (Line Inversion)

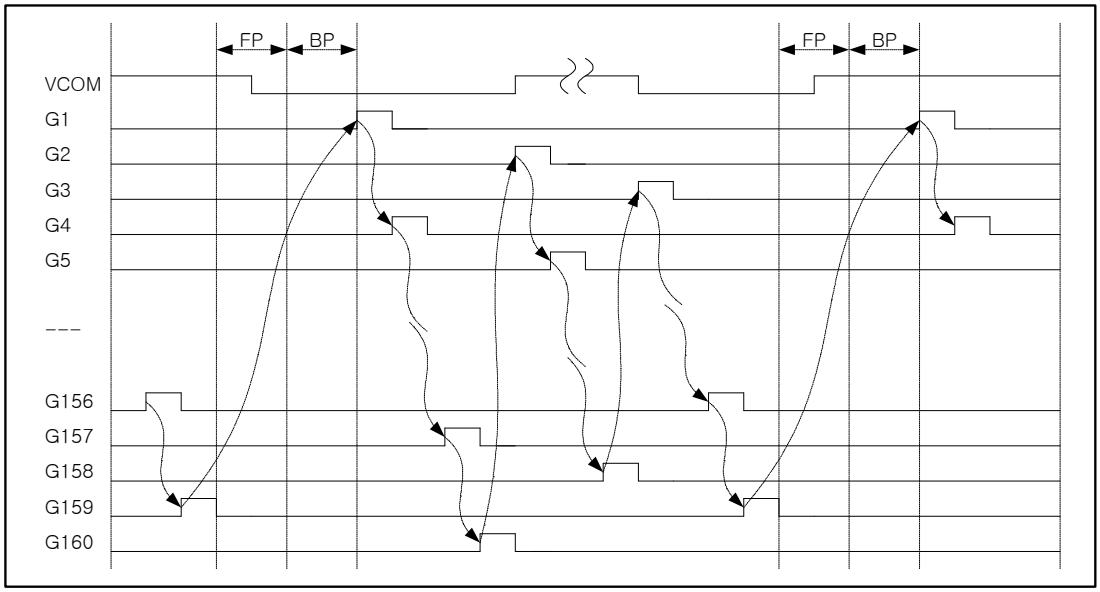


Figure 77 : 3-field interlaced scanning method

GAMMA ADJUSTMENT FUNCTION

The S6D0144 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels. Furthermore, since the gradient adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

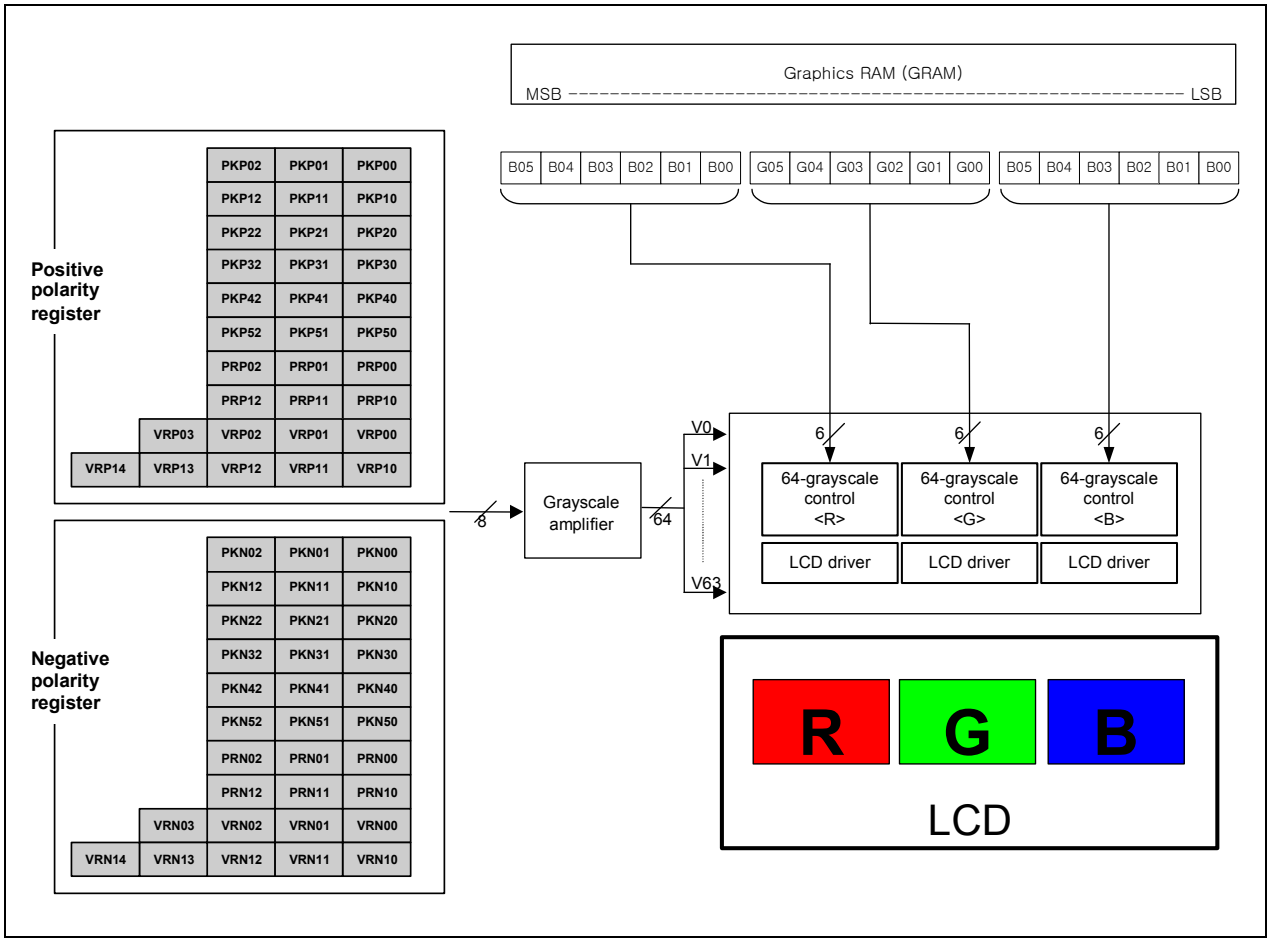


Figure 78 : Grayscale control

STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of the grayscale amplifier is shown as below. Determine 8-level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Each level is split by the internal ladder resistance and level between V0 to V63 is generated.

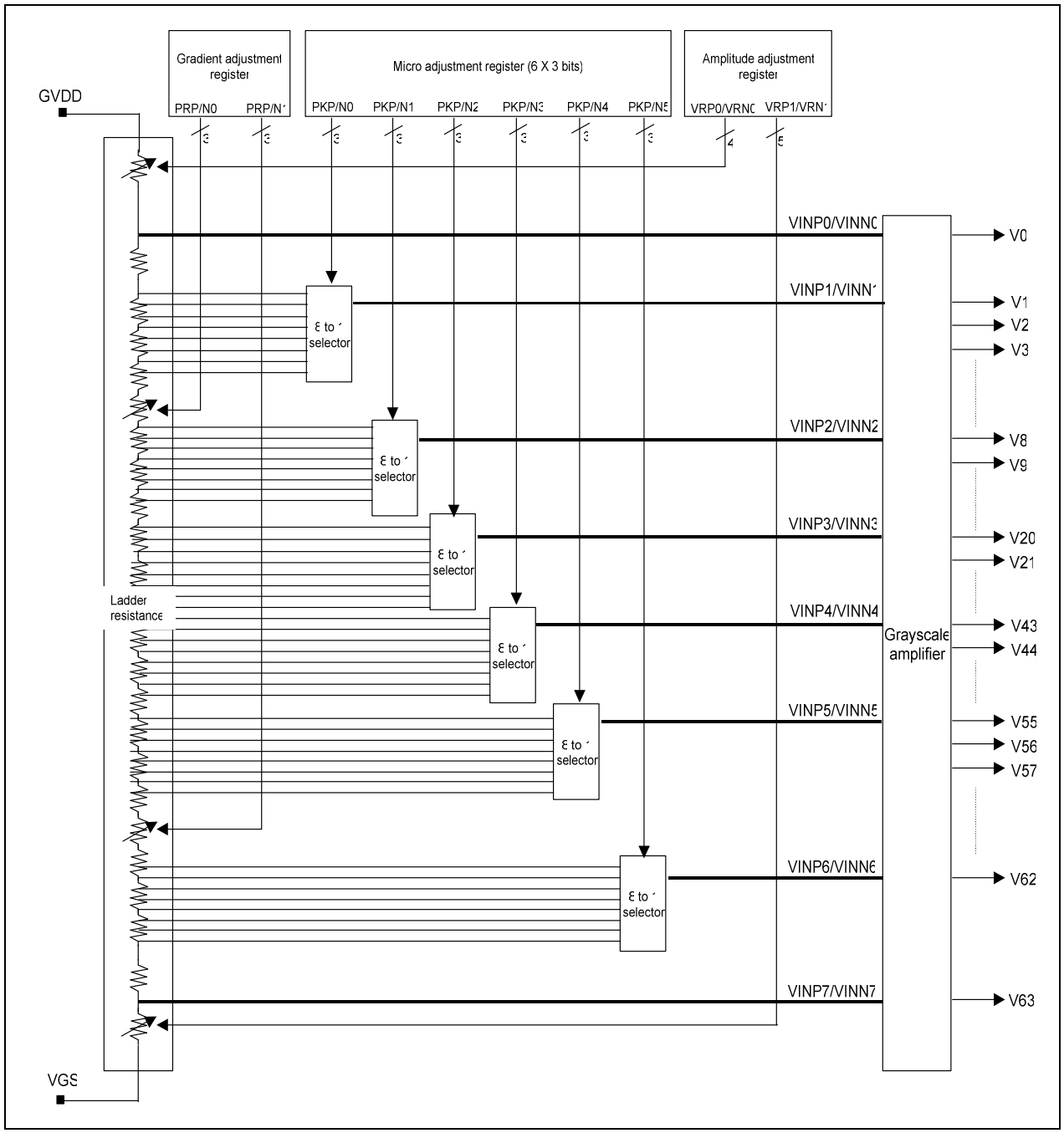


Figure 79 : Structure of grayscale amplifier

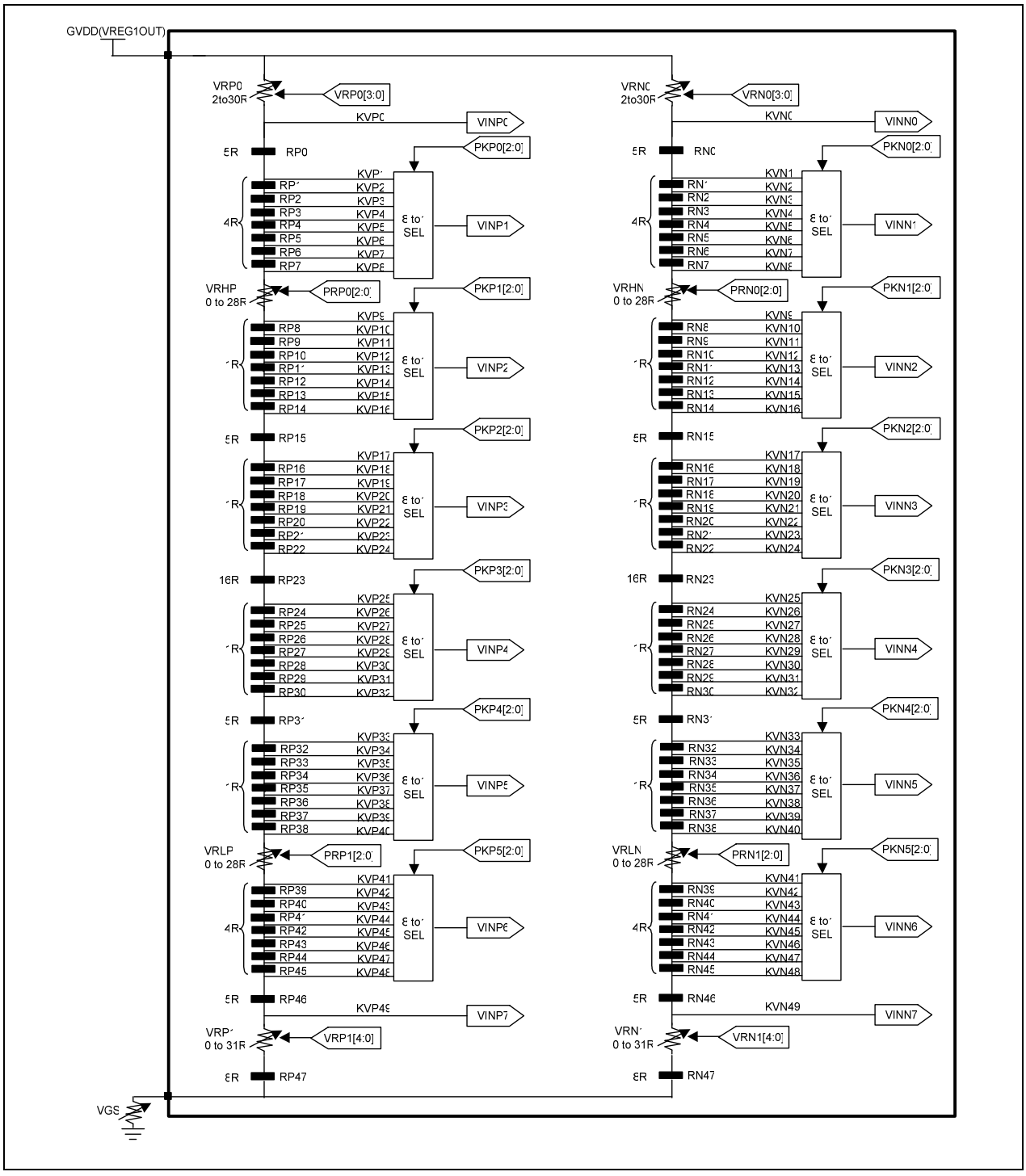


Figure 80 : Structure of Ladder / 8 to 1 selector

GAMMA ADJUSTMENT REGISTER

This block has the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 3 types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (Average <R><G><B> is common.) The following figure indicates the operation of each adjusting register.

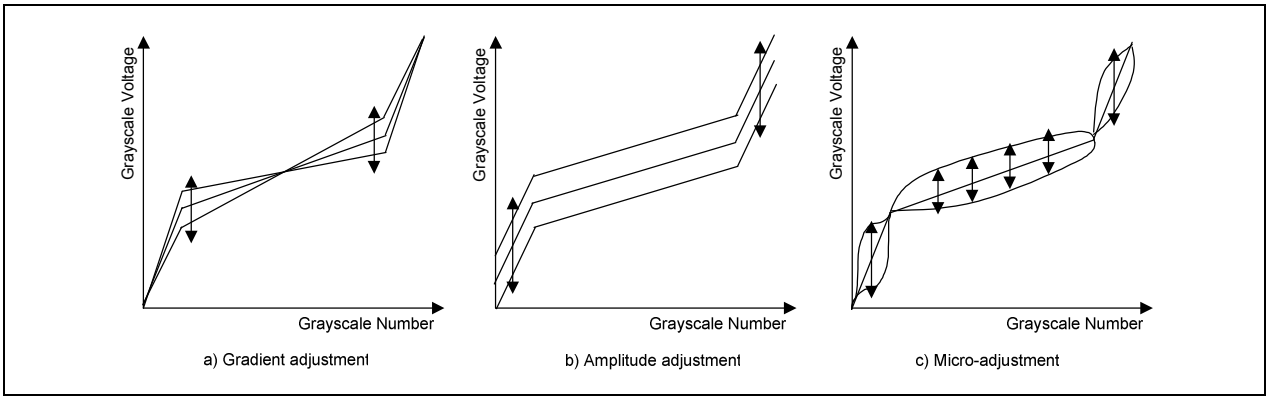


Figure 81 : The operation of adjusting register

a) Gradient adjustment resistor

The gradient adjustment resistors are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N) / VRLP (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

b) Amplitude adjustment resistor

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at upper side of the ladder resistor and it controls the variable resistor (VRP(N)1) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor.

Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

c) Micro adjustment resistor

The micro adjustment resistor is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Table 65 : Gamma correction registers

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Micro-adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP2[2:0]	PKN2[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

LADDER RESISTOR / 8-to-1 SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. The variable and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length from one panel to another.

VARIABLE RESISTOR

There are 2 types of the variable resistors that are for the gradient adjustment (VRHP (N) / VRLP (N)) and for the amplitude adjustment (VRP(N)0 / VRP(N)1). The resistance value is set by the gradient adjusting resistor and the amplitude adjustment resistor as below.

Table 66 : Gradient Adjustment

Register value PRP(N) [2:0]	Resistance value VRHP(N)/VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 67 : Amplitude Adjustment(1)

Register value VRP(N)0 [3:0]	Resistance value VRP(N)0
0000	0R
0001	2R
0010	4R
. . .	. . .
1101	26R
1110	28R
1111	30R

Table 68 : Amplitude Adjustment(2)

Register value VRP(N)1 [4:0] , VR1C=0	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
. . .	. . .
11101	29R
11110	30R
11111	31R

Table 69 : Amplitude Adjustment(3)

Register value VRP(N)1 [4:0] , VR1C=1	Resistance value VRP(N)1
00000	0R
00001	2R
00010	4R
. . .	. . .
01101	26R
01110	28R
01111	30R
10000	Setting disabled
. . .	. . .
11101	Setting disabled
11110	Setting disabled
11111	Setting disabled

8-to-1 SELECTOR

In the 8 to 1 selector, the voltage level must be selected given by the ladder resistance and the micro-adjusting register. And output the voltage the six types of the reference voltage, the VIN1- to VIN6.
Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Table 70 : Relationship between Micro-adjustment Register and Selected Voltage

Register value PKP(N) [2:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

Table 71 : Gamma Adjusting Voltage Formula (Positive polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	GVDD - ΔV *VRP0 / SUMRP	-	VINP0
KVP1	GVDD - ΔV * (VRP0 + 5R) / SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	GVDD - ΔV * (VRP0 + 9R) / SUMRP	PKP0[2:0] = “001”	
KVP3	GVDD - ΔV * (VRP0 + 13R) / SUMRP	PKP0[2:0] = “010”	
KVP4	GVDD - ΔV * (VRP0 + 17R) / SUMRP	PKP0[2:0] = “011”	
KVP5	GVDD - ΔV * (VRP0 + 21R) / SUMRP	PKP0[2:0] = “100”	
KVP6	GVDD - ΔV * (VRP0 + 25R) / SUMRP	PKP0[2:0] = “101”	
KVP7	GVDD - ΔV * (VRP0 + 29R) / SUMRP	PKP0[2:0] = “110”	
KVP8	GVDD - ΔV * (VRP0 + 33R) / SUMRP	PKP0[2:0] = “111”	
KVP9	GVDD - ΔV * (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	GVDD - ΔV * (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = “001”	
KVP11	GVDD - ΔV * (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = “010”	
KVP12	GVDD - ΔV * (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = “011”	
KVP13	GVDD - ΔV * (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = “100”	
KVP14	GVDD - ΔV * (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = “101”	
KVP15	GVDD - ΔV * (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = “110”	
KVP16	GVDD - ΔV * (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = “111”	
KVP17	GVDD - ΔV * (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	GVDD - ΔV * (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = “001”	
KVP19	GVDD - ΔV * (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = “010”	
KVP20	GVDD - ΔV * (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = “011”	
KVP21	GVDD - ΔV * (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = “100”	
KVP22	GVDD - ΔV * (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = “101”	
KVP23	GVDD - ΔV * (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = “110”	
KVP24	GVDD - ΔV * (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = “111”	
KVP25	GVDD - ΔV * (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	GVDD - ΔV * (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = “001”	
KVP27	GVDD - ΔV * (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = “010”	
KVP28	GVDD - ΔV * (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = “011”	
KVP29	GVDD - ΔV * (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = “100”	
KVP30	GVDD - ΔV * (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = “101”	
KVP31	GVDD - ΔV * (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = “110”	
KVP32	GVDD - ΔV * (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = “111”	
KVP33	GVDD - ΔV * (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	GVDD - ΔV * (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = “001”	
KVP35	GVDD - ΔV * (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = “010”	
KVP36	GVDD - ΔV * (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = “011”	
KVP37	GVDD - ΔV * (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = “100”	
KVP38	GVDD - ΔV * (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = “101”	
KVP39	GVDD - ΔV * (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = “110”	
KVP40	GVDD - ΔV * (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = “111”	
KVP41	GVDD - ΔV * (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	GVDD - ΔV * (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “001”	
KVP43	GVDD - ΔV * (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “010”	
KVP44	GVDD - ΔV * (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “011”	
KVP45	GVDD - ΔV * (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “100”	
KVP46	GVDD - ΔV * (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “101”	
KVP47	GVDD - ΔV * (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “110”	
KVP48	GVDD - ΔV * (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “111”	
KVP49	GVDD - ΔV * (VRP0 + 120R + VRHP + VRLP) / SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0+VRP1
ΔV: Potential difference between GVDD-VGS

Table 72 : Gamma Voltage Formula (Positive Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V20-(V20-V43)*(12/23)
V1	VINP1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINP2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINP4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINP3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINP5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINP6
V31	V20-(V20-V43)*(11/23)	V63	VINP7

[NOTE] Keep the following conditions.
AVDD – V0 > 0.5V
AVDD – V8 > 1.1V

Table 73 : Gamma Adjusting Voltage Formula (Negative polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	GVDD - ΔV *VRN0 / SUMRN	-	VINN0
KVN1	GVDD - ΔV * (VRN0 + 5R) / SUMRN	PKP0[2:0] = “000”	VINN1
KVN2	GVDD - ΔV * (VRN0 + 9R) / SUMRN	PKP0[2:0] = “001”	
KVN3	GVDD - ΔV * (VRN0 + 13R) / SUMRN	PKP0[2:0] = “010”	
KVN4	GVDD - ΔV * (VRN0 + 17R) / SUMRN	PKP0[2:0] = “011”	
KVN5	GVDD - ΔV * (VRN0 + 21R) / SUMRN	PKP0[2:0] = “100”	
KVN6	GVDD - ΔV * (VRN0 + 25R) / SUMRN	PKP0[2:0] = “101”	
KVN7	GVDD - ΔV * (VRN0 + 29R) / SUMRN	PKP0[2:0] = “110”	
KVN8	GVDD - ΔV * (VRN0 + 33R) / SUMRN	PKP0[2:0] = “111”	
KVN9	GVDD - ΔV * (VRN0 + 33R + VRHN) / SUMRN	PKP1[2:0] = “000”	VINN2
KVN10	GVDD - ΔV * (VRN0 + 34R + VRHN) / SUMRN	PKP1[2:0] = “001”	
KVN11	GVDD - ΔV * (VRN0 + 35R + VRHN) / SUMRN	PKP1[2:0] = “010”	
KVN12	GVDD - ΔV * (VRN0 + 36R + VRHN) / SUMRN	PKP1[2:0] = “011”	
KVN13	GVDD - ΔV * (VRN0 + 37R + VRHN) / SUMRN	PKP1[2:0] = “100”	
KVN14	GVDD - ΔV * (VRN0 + 38R + VRHN) / SUMRN	PKP1[2:0] = “101”	
KVN15	GVDD - ΔV * (VRN0 + 39R + VRHN) / SUMRN	PKP1[2:0] = “110”	
KVN16	GVDD - ΔV * (VRN0 + 40R + VRHN) / SUMRN	PKP1[2:0] = “111”	
KVN17	GVDD - ΔV * (VRN0 + 45R + VRHN) / SUMRN	PKP2[2:0] = “000”	VINN3
KVN18	GVDD - ΔV * (VRN0 + 46R + VRHN) / SUMRN	PKP2[2:0] = “001”	
KVN19	GVDD - ΔV * (VRN0 + 47R + VRHN) / SUMRN	PKP2[2:0] = “010”	
KVN20	GVDD - ΔV * (VRN0 + 48R + VRHN) / SUMRN	PKP2[2:0] = “011”	
KVN21	GVDD - ΔV * (VRN0 + 49R + VRHN) / SUMRN	PKP2[2:0] = “100”	
KVN22	GVDD - ΔV * (VRN0 + 50R + VRHN) / SUMRN	PKP2[2:0] = “101”	
KVN23	GVDD - ΔV * (VRN0 + 51R + VRHN) / SUMRN	PKP2[2:0] = “110”	
KVN24	GVDD - ΔV * (VRN0 + 52R + VRHN) / SUMRN	PKP2[2:0] = “111”	
KVN25	GVDD - ΔV * (VRN0 + 68R + VRHN) / SUMRN	PKP3[2:0] = “000”	VINN4
KVN26	GVDD - ΔV * (VRN0 + 69R + VRHN) / SUMRN	PKP3[2:0] = “001”	
KVN27	GVDD - ΔV * (VRN0 + 70R + VRHN) / SUMRN	PKP3[2:0] = “010”	
KVN28	GVDD - ΔV * (VRN0 + 71R + VRHN) / SUMRN	PKP3[2:0] = “011”	
KVN29	GVDD - ΔV * (VRN0 + 72R + VRHN) / SUMRN	PKP3[2:0] = “100”	
KVN30	GVDD - ΔV * (VRN0 + 73R + VRHN) / SUMRN	PKP3[2:0] = “101”	
KVN31	GVDD - ΔV * (VRN0 + 74R + VRHN) / SUMRN	PKP3[2:0] = “110”	
KVN32	GVDD - ΔV * (VRN0 + 75R + VRHN) / SUMRN	PKP3[2:0] = “111”	
KVN33	GVDD - ΔV * (VRN0 + 80R + VRHN) / SUMRN	PKP4[2:0] = “000”	VINN5
KVN34	GVDD - ΔV * (VRN0 + 81R + VRHN) / SUMRN	PKP4[2:0] = “001”	
KVN35	GVDD - ΔV * (VRN0 + 82R + VRHN) / SUMRN	PKP4[2:0] = “010”	
KVN36	GVDD - ΔV * (VRN0 + 83R + VRHN) / SUMRN	PKP4[2:0] = “011”	
KVN37	GVDD - ΔV * (VRN0 + 84R + VRHN) / SUMRN	PKP4[2:0] = “100”	
KVN38	GVDD - ΔV * (VRN0 + 85R + VRHN) / SUMRN	PKP4[2:0] = “101”	
KVN39	GVDD - ΔV * (VRN0 + 86R + VRHN) / SUMRN	PKP4[2:0] = “110”	
KVN40	GVDD - ΔV * (VRN0 + 87R + VRHN) / SUMRN	PKP4[2:0] = “111”	
KVN41	GVDD - ΔV * (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “000”	VINN6
KVN42	GVDD - ΔV * (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “001”	
KVN43	GVDD - ΔV * (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “010”	
KVN44	GVDD - ΔV * (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “011”	
KVN45	GVDD - ΔV * (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “100”	
KVN46	GVDD - ΔV * (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “101”	
KVN47	GVDD - ΔV * (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “110”	
KVN48	GVDD - ΔV * (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKP5[2:0] = “111”	
KVN49	GVDD - ΔV * (VRN0 + 120R + VRHN + VRLN) / SUMRN	-	VINN7

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0+VRN1
ΔV: Potential difference between GVDD-VGS

Table 74 : Gamma Voltage Formula (Negative Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V20-(V20-V43)*(12/23)
V1	VINN1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINN2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINN4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINN3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINN5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINN6
V31	V20-(V20-V43)*(11/23)	V63	VINN7

[NOTE] Keep the following conditions.
AVDD – V0 > 0.5V
AVDD – V8 > 1.1V

OUTPUT LEVEL AS THE FUNCTION OF GRAM DATA

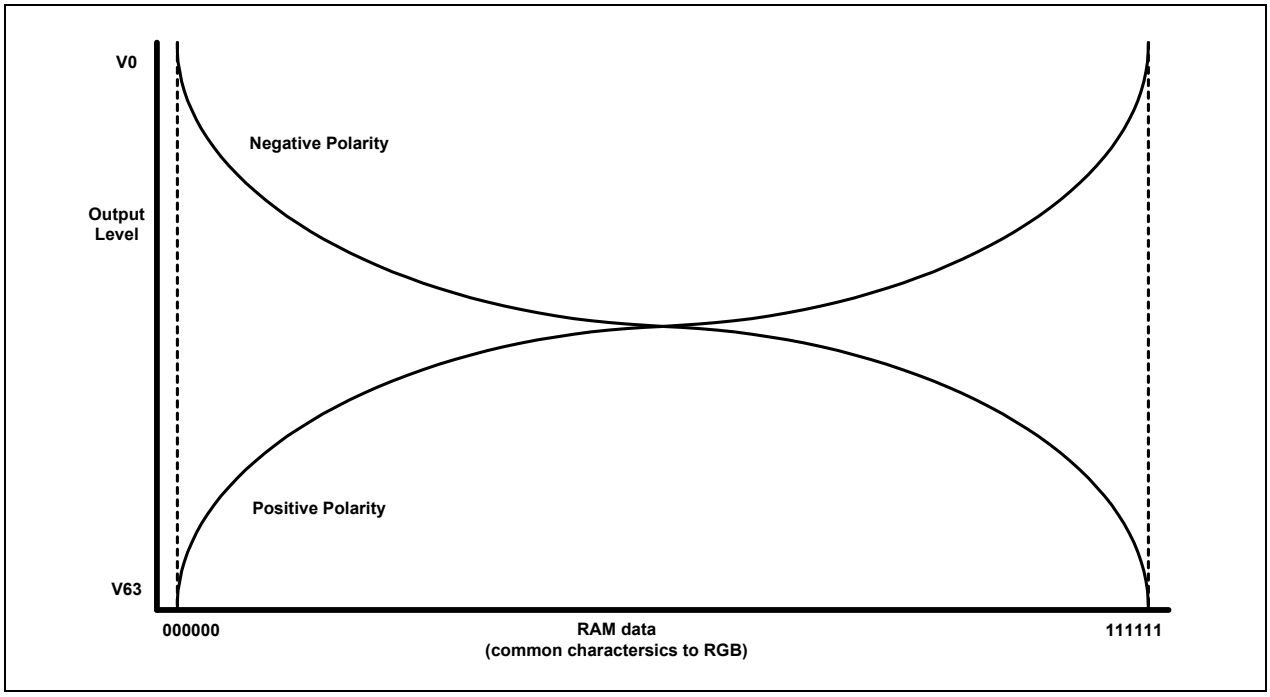
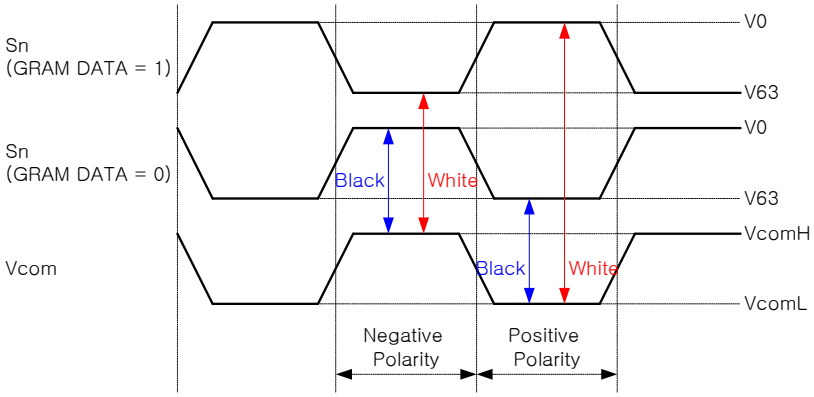
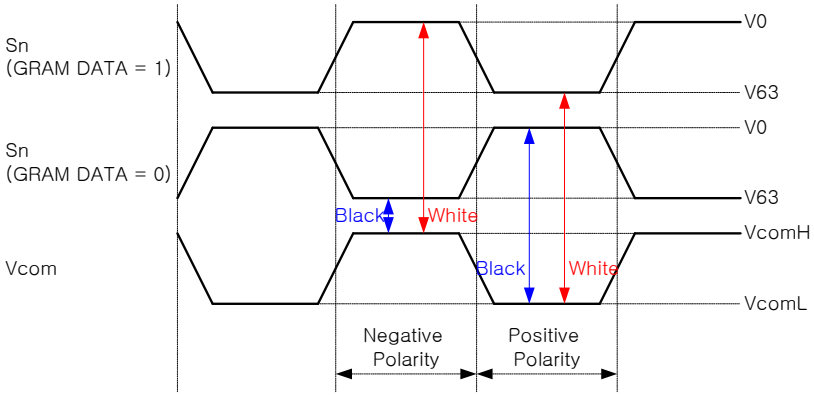


Figure 82 : Relationship between RAM data and output voltage



(a) For Normally Black Panel (REV = 0)



(b) For Normally White Panel (REV = 1)

Figure 83 : Relationship between source output and Vcom

THE 8-COLOR DISPLAY MODE

The S6D0144 incorporates 8-color display mode. During the 8-color mode all the gray scale levels (V1~V62) are halt. So that it attempts to lower power consumption.
During the 8-color mode, the Gamma micro adjustment register, PKP and PKN are invalid. Since V1-V62 is stopped, the RGB data in the GRAM should be set to 000000 or 111111 before set the mode.

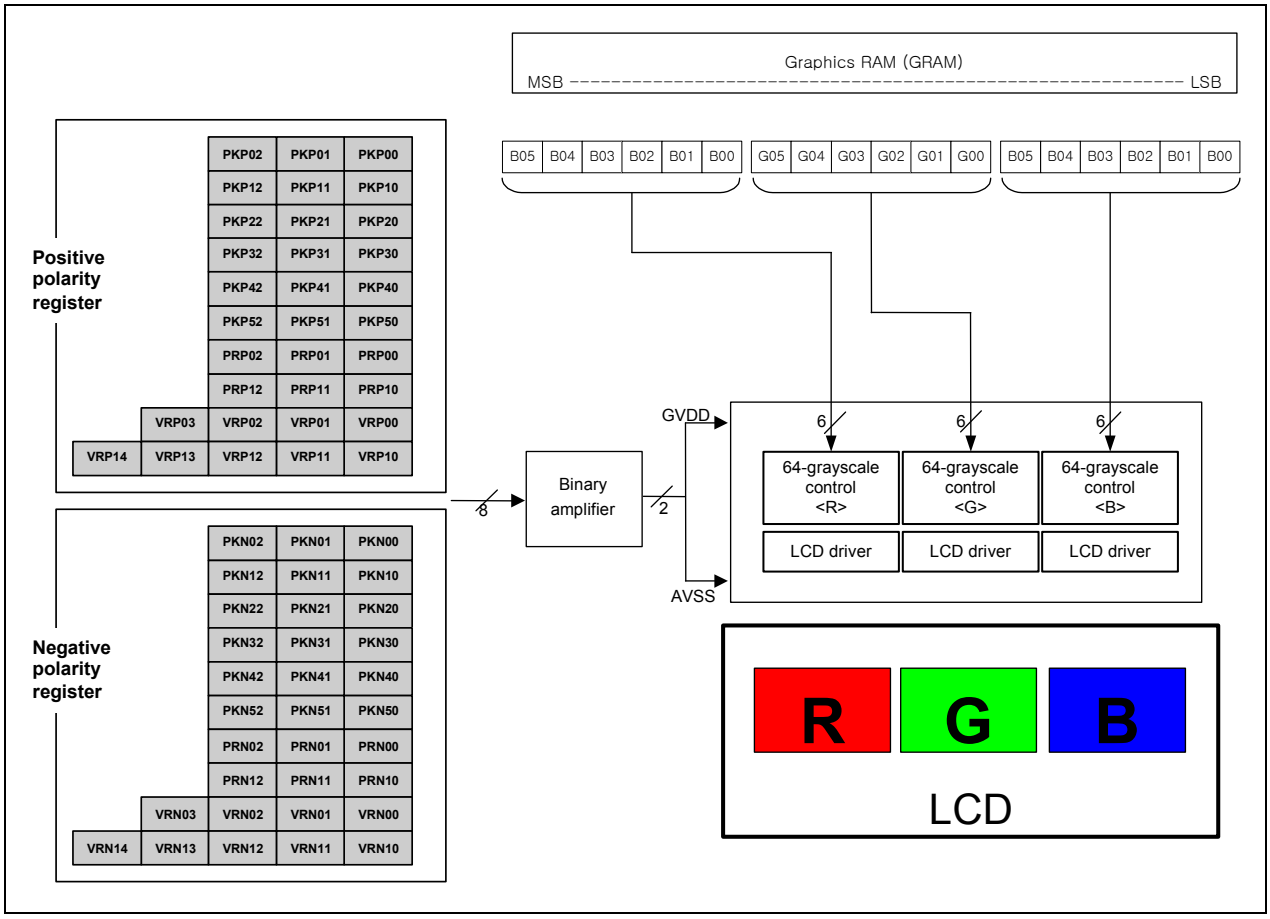


Figure 84 : 8-color display control

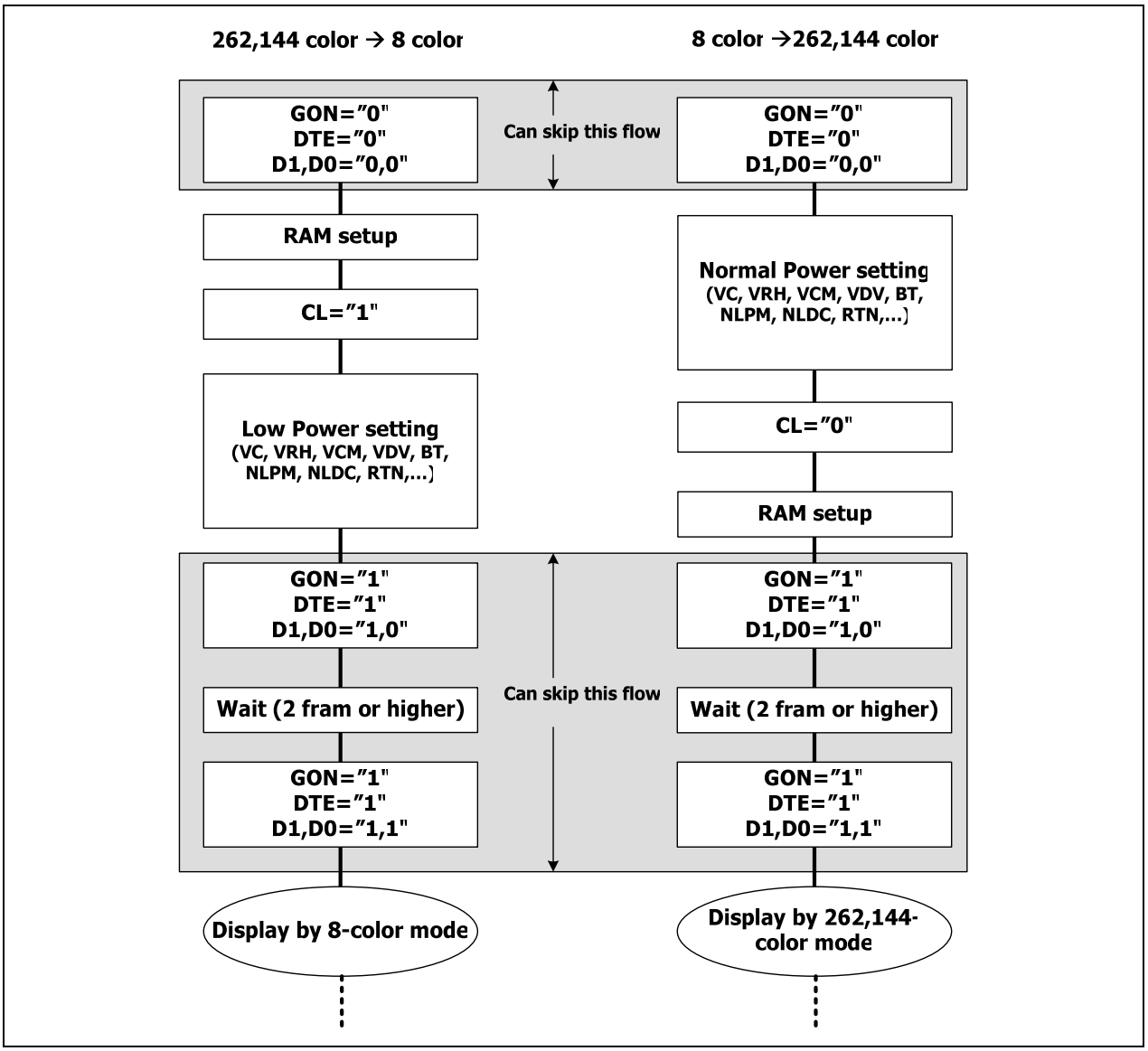


Figure 85 : Set up procedure for the 8-color mode

INSTRUCTION SET UP FLOW

DISPLAY ON / OFF SEQUENCE

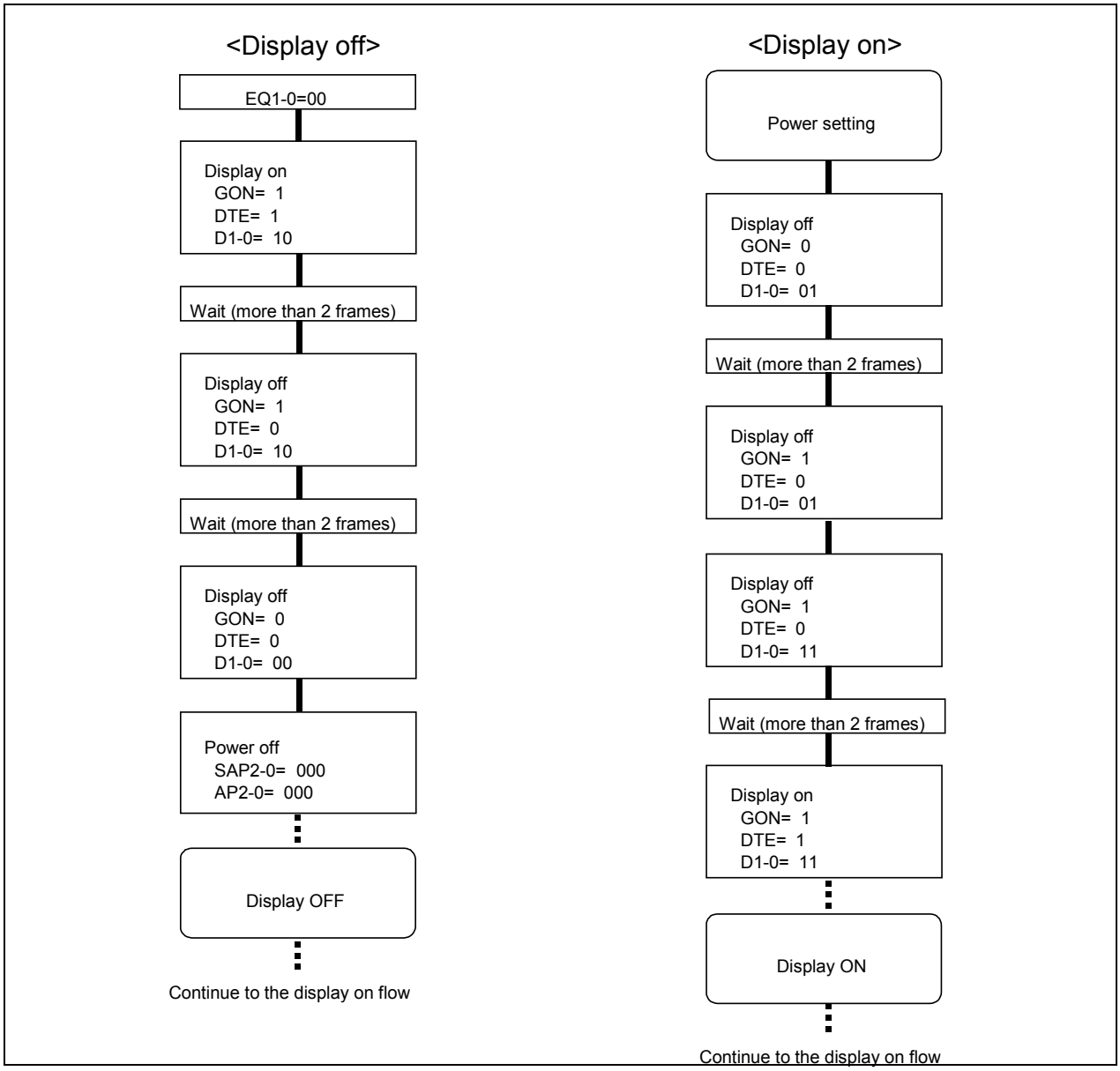


Figure 86 : DISPLAY ON / OFF SEQUENCE

D-STAND-BY / STAND-BY / SLEEP SEQUENCE

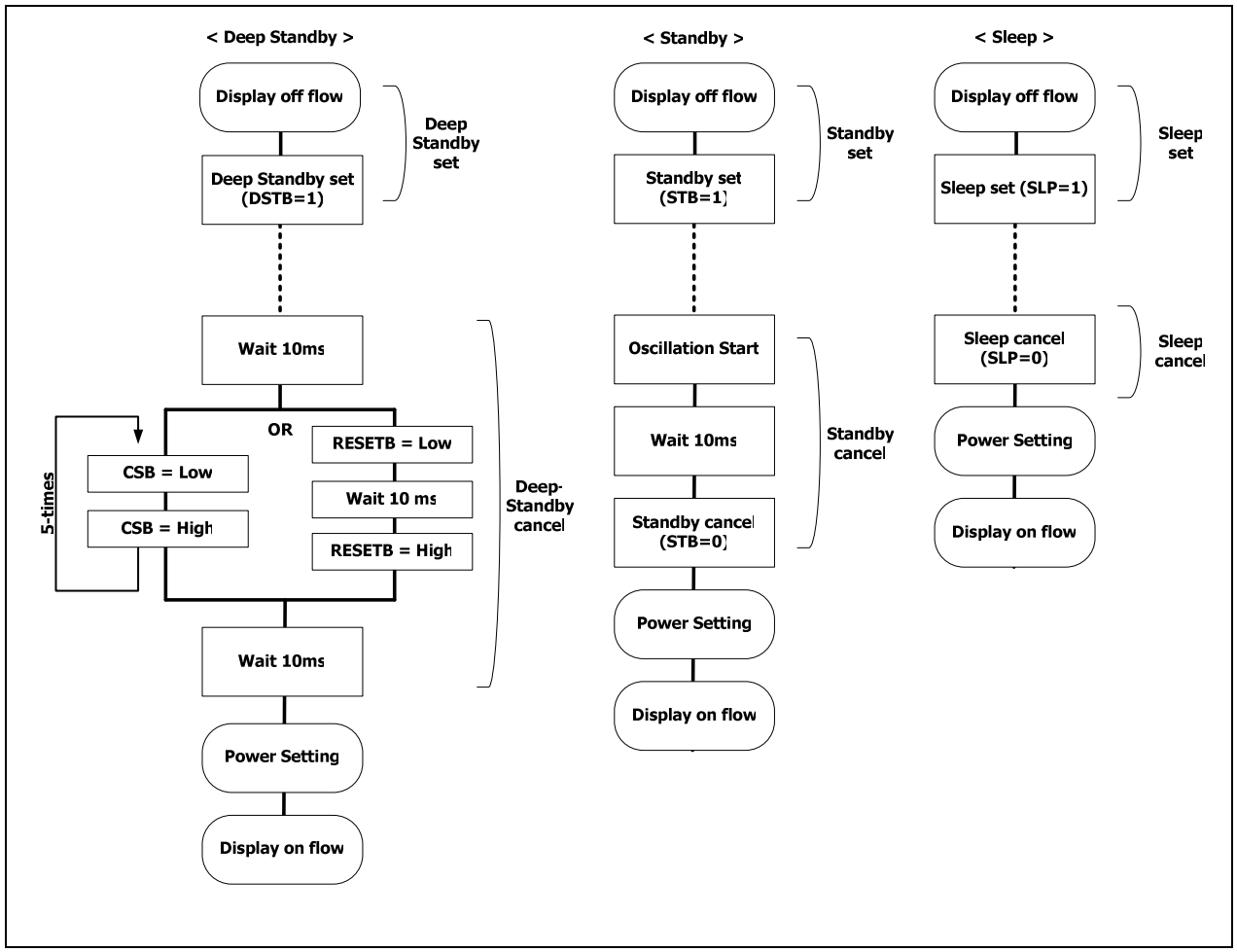


Figure 87 : D-STAND-BY/STAND-BY / SLEEP SEQUENCE

OSCILLATION CIRCUIT

The S6D0144 can provide R-C oscillation. S6D0144 internal oscillator does not need to attach the external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the oscillator frequency control register setting. Since R-C oscillation stops during the standby mode, power consumption can be reduced.

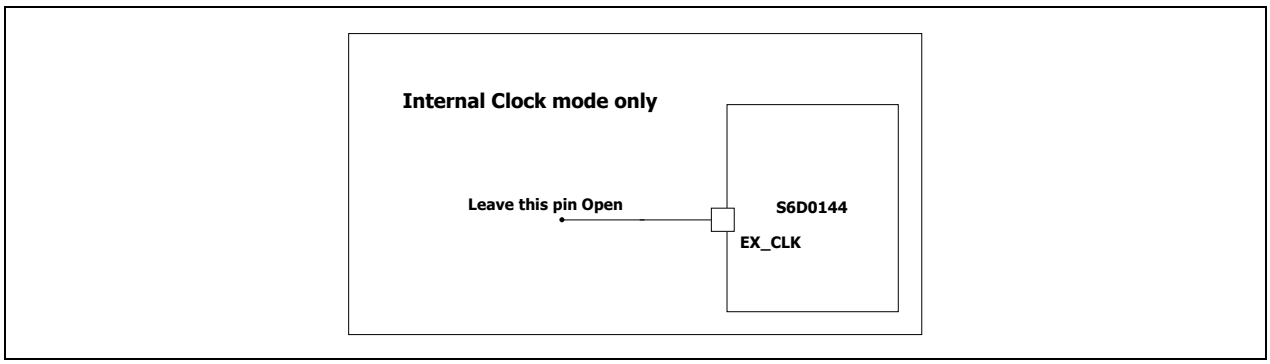


Figure 88 : Oscillation Circuit

APPLICATION CIRCUIT

The following figure indicates a schematic diagram of application circuit for S6D0144.

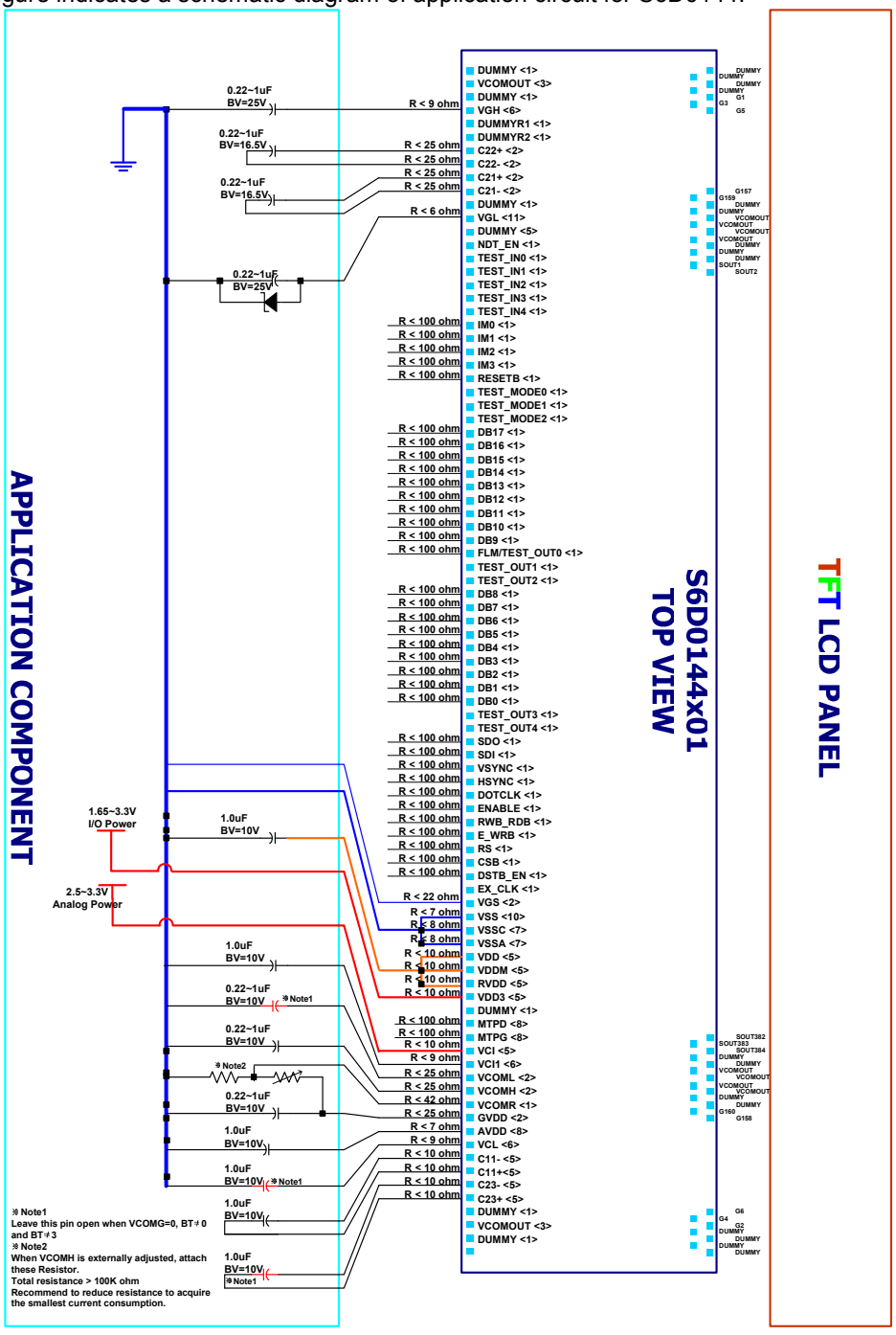


Figure 89 : Application Circuit

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 75 : Absolute Maximum Rating

(VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage for logic block	VDD - VSS	-0.3 ~ 3.3	V
Supply voltage for I/O block	VDD3 - VSS	-0.3 ~ 5.0	
Supply voltage for step-up circuit	VCI - VSS	-0.3 ~ 5.0	V
LCD Supply Voltage range	AVDD – VSS	-0.3 ~ 6.5	V
	VGH - VSS	-0.3 ~ 22.0	
	VSS – VGL	-0.3 ~ 22.0	
	VSS - VCL	-0.3 ~ 5.0	
	|VGH – VGL|	-0.3 ~ 33	
Input Voltage range	Vin	- 0.3 to VDD3 +0.3	V
Maximum rewritable time of MTP	t_{mtp}	1000	times
Operating temperature	T_{opr}	-40 ~ +85	°C
Storage temperature	T_{stg}	-55 ~ +110	°C

[NOTE] Absolute maximum rating is the limit value beyond which the IC may be broken. They do not assure operations
Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.
Absolute maximum rating is guaranteed when our company's package used.

Caution

Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

DC CHARACTERISTICS

Table 76 : DC Characteristics

(VSS = 0V, T_A = -40°C ~ 85°C)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Operating voltage	VDD		1.40		1.60	V	*1
	VDD3		1.65		3.3	V	*1
LCD driving voltage	VGH		+7		16.5	V	
	VGL		-13.5		-7	V	
	AVDD		3.5		5.5	V	
Input high voltage	V_{IH}		0.8VDD3		VDD3	V	*2
Input low voltage	V_{IL}		0		0.2VDD3	V	*2
Output high voltage	V_{OH}	I_{OH} = -1.0mA	0.8VDD3		VDD3	V	*3
Output low voltage	V_{OL}	I_{OL} = 10mA	0.0		0.2VDD3	V	*3
Input leakage current	I_{IL}	VIN = VSS or VDD3	-1.0		1.0	μA	*2
Output leakage current	I_{OL}	VIN = VSS or VDD3	-3.0		3.0	μA	*2
Operating frequency	fosc	VDD3=2.8V	T.B.D.	240	T.B.D.	kHz	*4
Internal reference power supply voltage	VCI		2.5	-	3.3	V	
1st step-up output efficiency	AVDD	ILOAD=1.0mA, VCI=2.8V BT=000	90	95		%	
2nd step-up output efficiency	VGH	ILOAD=0.2mA, VCI=2.8V BT=000	90	95		%	
3rd step-up output efficiency	VGL	ILOAD=0.1mA, VCI=2.8V BT=000	90	95		%	
4th step-up output efficiency	VCL	ILOAD=0.2mA, VCI=2.8V BT=000	90	95		%	

[NOTE]
1. VSS= 0V
2. Applied pins; IM, CSB, E_WRB, RWB_RDB, RS, DB, DSTB_EN, RESETB.
3. Applied pins; DB
4. Target frame frequency = 60 Hz, Display line = 160, Back porch = 3, Front porch = 5
5. Internal RTN[4:0] register = “11000”, Internal DIV[1:0] register = “00”

Table 77 : DC Characteristics for LCD driver outputs

(AVDD=5.0V, VSS = 0V, T_A = -40°C ~ 85°C)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
LCD gate driver output on resistance	Ron	VGH–VGL=30.0V, VGH=16.5V, VGL=-13.5V, Vgo=VGH - 0.5V		-	2.5	kΩ	
Output voltage deviation (Mean value)	ΔVo	4.2V ≤ Vso		±20	±55	mV	
		0.8V < Vso < 4.2V		±10	±30	mV	
		Vso ≤ 0.8V		±20	±55	mV	
LCD source driver output voltage range	Vso	-	0.1	-	AVDD-0.1	V	
LCD source driver delay (Cload=18pF,Rload=11Khom)	t_{SD1}	AVDD = 5.0V SAP = "010"	-	-	80	µs	
	t_{SD2}	AVDD = 5.0V SAP = "011"	-	-	50	µs	
	t_{SD3}	AVDD = 5.0V SAP = "100"	-	-	40	µs	
	t_{SD4}	AVDD = 5.0V SAP = "101"	-	-	30	µs	
Standby mode current	I_{stby_VDD3}	Standby mode, VDD3=2.8V, VDD=1.5V VCI=2.8V	-	-	TBD	µA	
	I_{stby_VDD}				TBD	µA	
	I_{stby_VCI}				TBD	µA	
Deep standby mode current	I_{dstby_VDD3}	Deep standby mode, VDD3=2.8V, VDD=0V VCI=2.8V	-	-	TBD	µA	
	I_{dstby_VDD}				TBD	µA	
	I_{dstby_VCI}				TBD	µA	
Current consumption during normal operation	IVDD	No load, VDD3=2.8, VDD=1.5V, VCI=2.8V			100	µA	
	IVCI				3	mA	
Current consumption during setting MTP	I_{MTPG}	MTPG=19V		0.6	TBD	mA	*1
	I_{MTPD}	MTPD=16V		0.6	TBD	mA	*1

[NOTE] 1. Simulation result., with common power condition VDD3=2.8, VDD=1.5V, VCI=2.8V

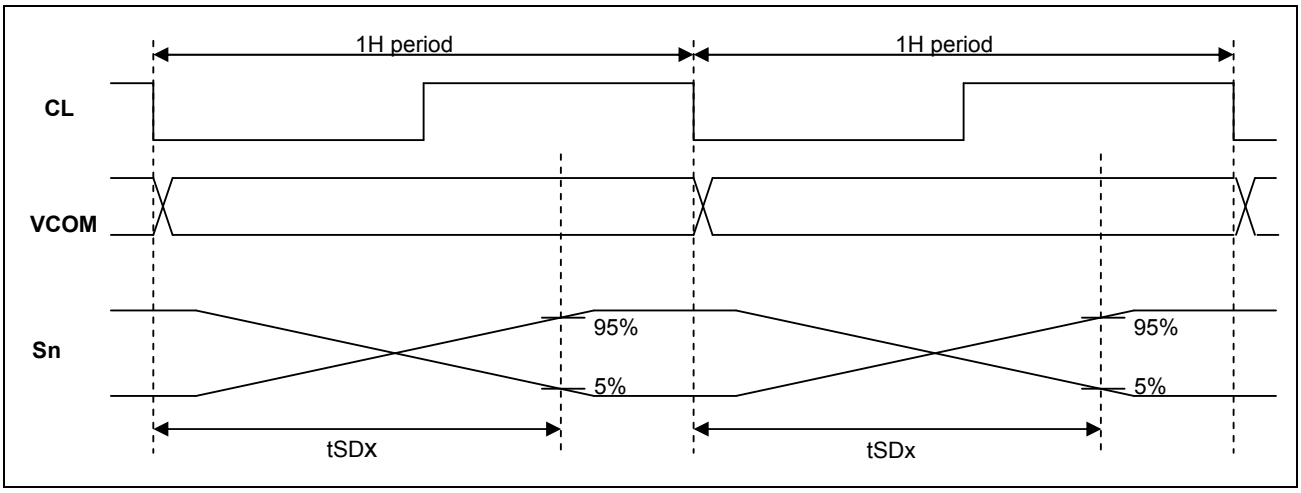
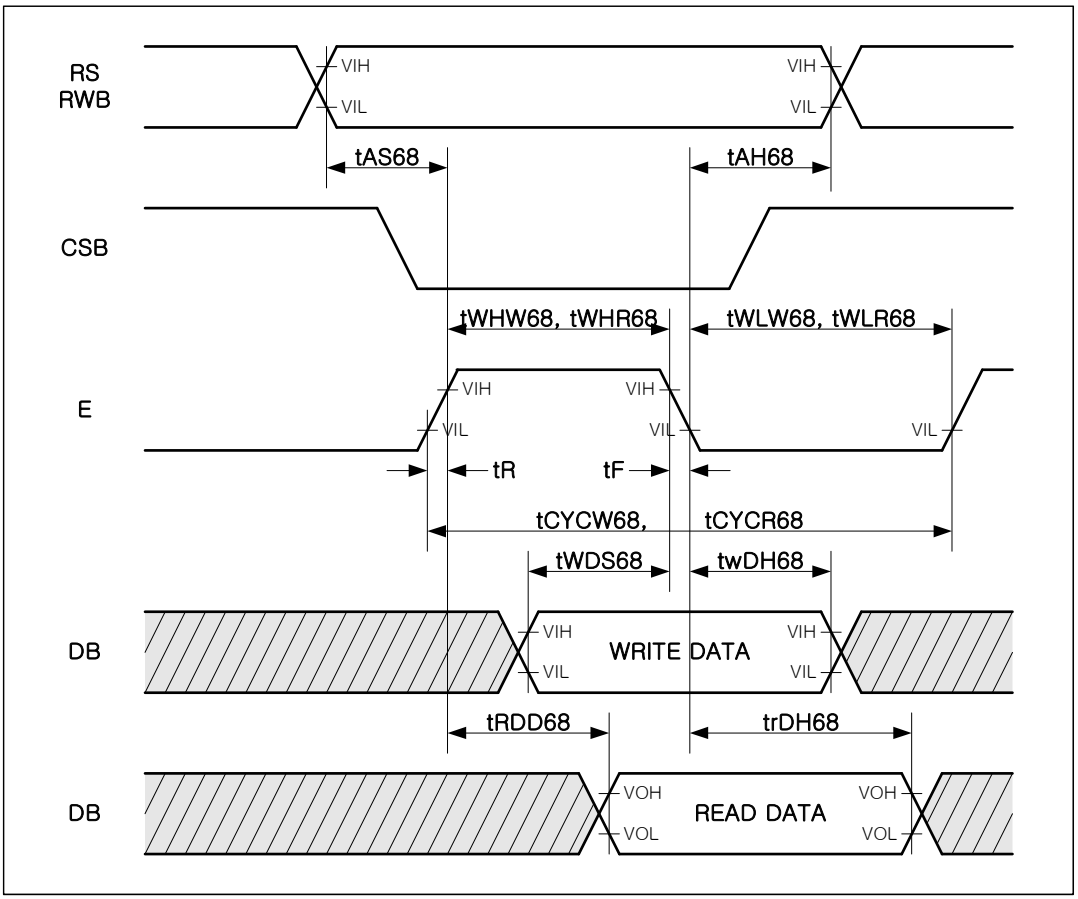


Figure 90 : DC characteristics

AC CHARACTERISTICS

68-SYSTEM 18/16/9/8BIT INTERFACE

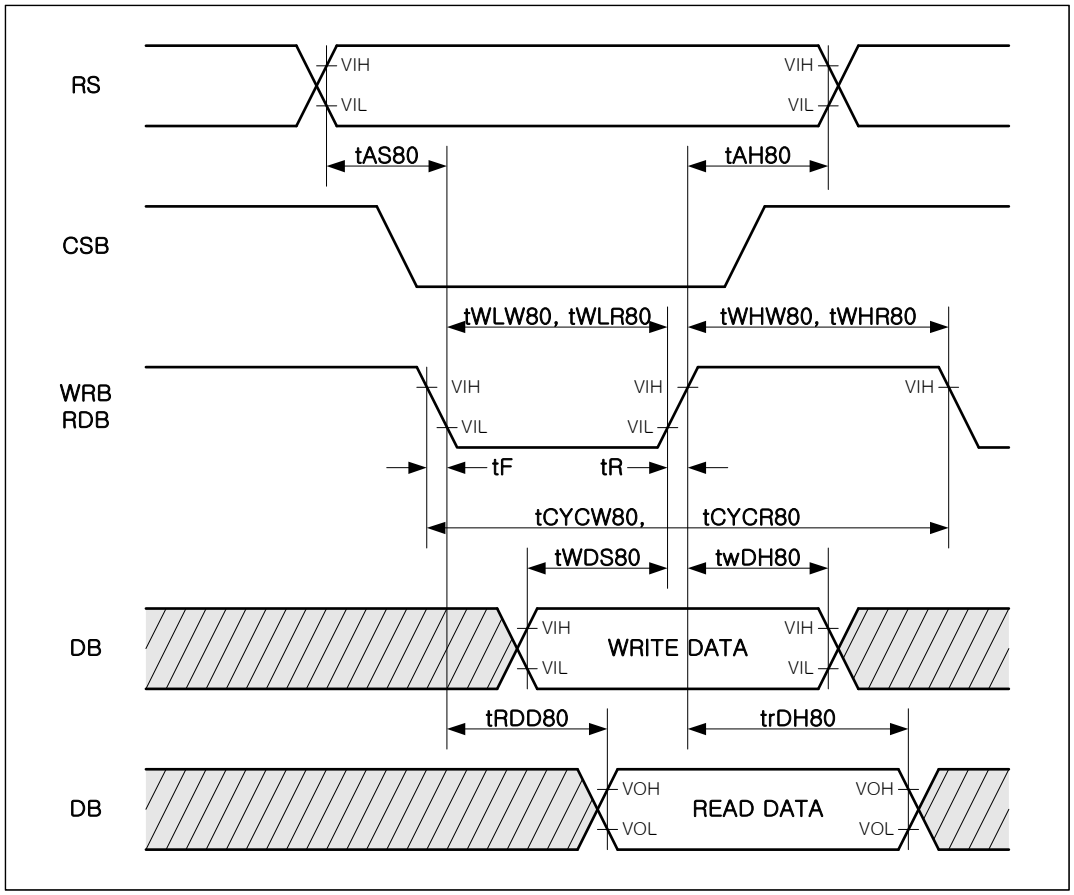


[NOTE] tWLW68 and tWLR68 are determined by the overlap period of low CSB and high E.

Parameter	Description	Min	Max	Unit
tCYCW68	Cycle time (Write)	100	-	ns
tCYCR68	Cycle time (Read)	500	-	ns
tR, tF	Pulse rise / fall time	-	25	ns
tWLW68	Pulse Width Low (Write)	40	-	ns
tWLR68	Pulse Width Low (Read)	250	-	ns
tWHW68	Pulse Width High (Write)	40	-	ns
tWHR68	Pulse Width High (Read)	200	-	ns
tAS68	RS, RWB to CSB, E setup time	0	-	ns
tAH68	RS, RWB to CSB, E hold time	0	-	ns
tWDS68	Write data setup time	60	-	ns
tWDH68	Write data hold time	2	-	ns
tRDD68	Read data delay time	-	200	ns
tRDH68	Read data hold time	5	-	ns

Figure 91 : AC characteristics of 68-system interface

80-SYSTEM 18/16/9/8BIT INTERFACE

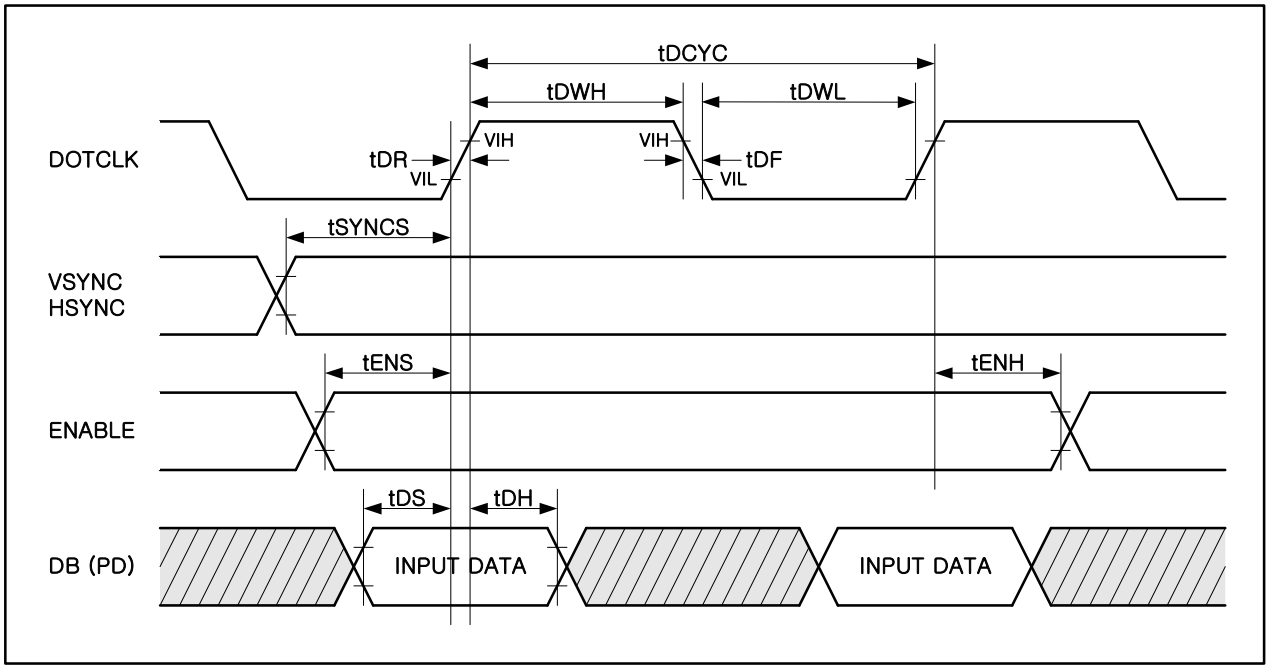


[NOTE] tWLW80 and tWLR80 are determined by the overlap period of low CSB and low WRB or low CSB and low RDB

Parameter	Description	Min	Max	Unit
tCYCW80	Cycle time (Write)	100	-	ns
tCYCR80	Cycle time (Read)	500	-	ns
tR, tF	Pulse rise / fall time	-	25	ns
tWLW80	Pulse Width Low (Write)	40	-	ns
tWLR80	Pulse Width Low (Read)	250	-	ns
tWHW80	Pulse Width High (Write)	40	-	ns
tWHR80	Pulse Width High (Read)	200	-	ns
tAS80	RS to CSB, WRB (or RDB) setup time	0	-	ns
tAH80	RS to CSB, WRB (or RDB) hold time	0	-	ns
tWDS80	Write data setup time	60	-	ns
tWDH80	Write data hold time	2	-	ns
tRDD80	Read data delay time	-	200	ns
tRDH80	Read data hold time	5	-	ns

Figure 92 : AC characteristics or 80-system interface

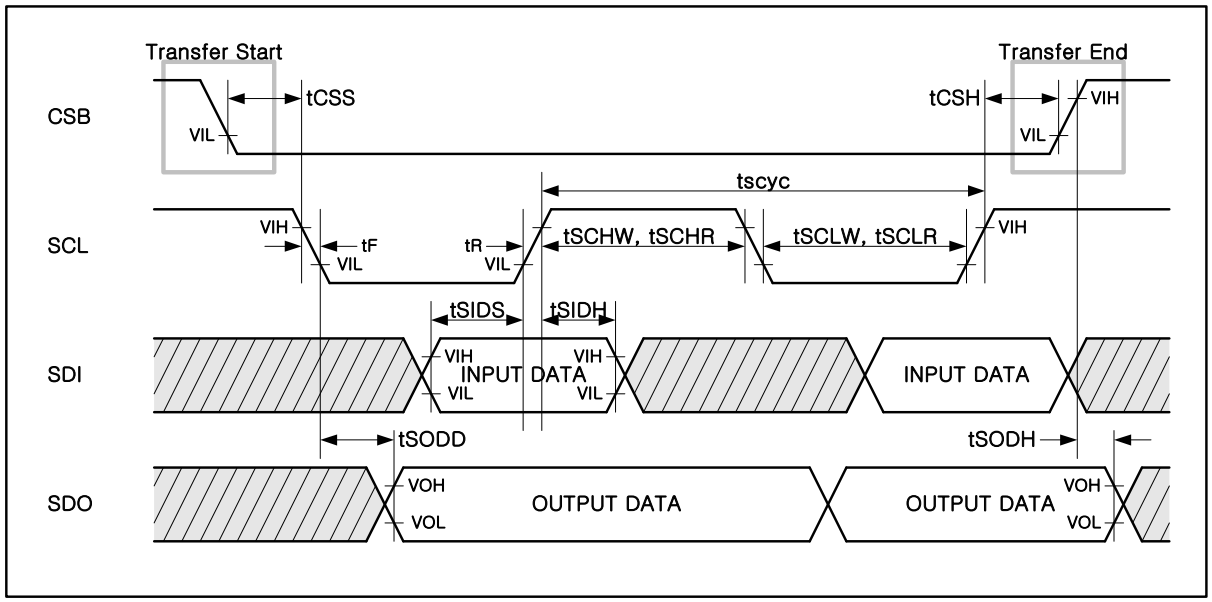
RGB INTERFACE



Parameter	Description	Min	Max	Unit
tDCYC	DOTCLK period	80	-	ns
tDWL	DOTCLK pulse width low	40	-	ns
tDWH	DOTCLK pulse width high	40	-	ns
tDR / tDF	DOTCLK rising / falling time	-	25	ns
tSYNCS	VSYNC, HSYNC setup	0	-	ns
tENS	ENABLE setup	30	-	ns
tENH	ENABLE hold	20	-	ns
tDS	Input Data setup	30	-	ns
tDH	Input Data hold	20	-	ns

Figure 93 : AC Characteristics of RGB Interface

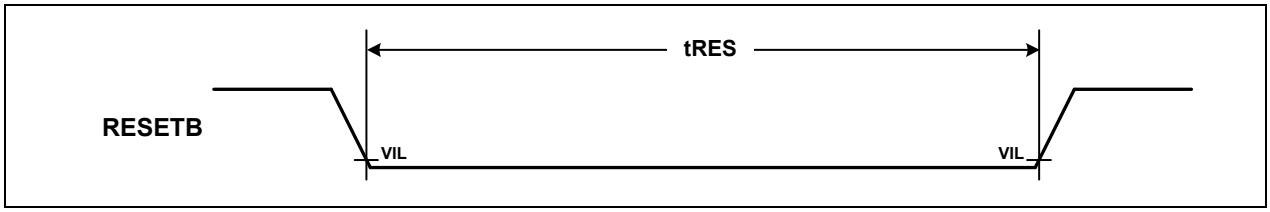
SERIAL PERIPHERAL INTERFACE



Parameter	Description	Min	Max	Unit
tscyc (write)	Serial clock write cycle time	100	-	ns
tscyc (read)	Serial clock read cycle time	500	-	ns
t_R, t_F	Serial clock rise / fall time	-	20	ns
t_{SCHW}	Pulse width high for write	40	-	ns
t_{SCHR}	Pulse width high for read	230	-	ns
t_{SCLW}	Pulse width low for write	60	-	ns
t_{SCLR}	Pulse width low for read	230	-	ns
t_{CSS}	Chip Select setup time	20	-	ns
t_{CSH}	Chip Select hold time	60	-	ns
t_{SIDS}	Serial input data setup time	40	-	ns
t_{SIDH}	Serial input data hold time	30	-	ns
t_{SODD}	Serial output data delay time	-	130	ns
t_{SODH}	Serial output data hold time	5	-	ns

Figure 94 : AC Characteristics of Serial Peripheral Interface

RESETB



[NOTE] Reset low pulse width shorter than 7us do not make reset. It means undesired short pulse such as glitch, bouncing noise or electrostatic discharge do not cause irregular system reset. Please refer to the table below.

Parameter	Description	Min	Max	Unit
tRES	Reset low pulse width	20	-	us

Figure 95 : AC characteristics (RESET timing)

Table 78 : Reset Operation Regarding tRES Pulse Width

tRES Pulse	Action
Shorter than 7 us	No reset
Longer than 20 us	Reset
Between 7 us and 20 us	Not determined

User may or may not use RESETB pin. In order to use it, user should satisfy the conditions described in the above tables. But when not wants to use RESETB, user may float it because internally generated POR (Power-On-Reset) is used. The RESETB is pulled-up internally.

FIGURES

TABLES

REVISION HYSTORY

S6D0144 Specification Revision History			
Version	**Content**	**Author**	**Date**
0.0	Original	J.S. Kang	September 8, 2005
0.1	1. MDT function added. 2. PAD specification modified. 3. NL register description added. 4. Non-inversion mode added. 5. RIM description modified. 6. PREGB function deleted. 7. Register VR1C[R11h] added. 8. Register SVC added. 9. Register EXCLK_EN deleted. 10. Register RADJ bit width reduced.	J.S. Kang	September 26, 2005
0.2	1. VCM, VDV, VCOMG register modified. 2. Pad center coordinates added. 3. Pin description modified. - VSSO deleted. - AVSS → VSSA - VSSA → VSSC - IOVCCDUM → Deleted - IOGNDDUM → Deleted - TEST_MODE → TEST_MODE2-0 - TEST_OUT → TEST_OUT4-0 - RVDD pin description modified. - Pin TEST_IN4-0 added.	H.J. Kim	October 07, 2005
0.3	1. PAD configuration added. 2. PAD center coordinate added. 3. Pin description modified. - SDI pin description - SDO pin description - TEST_OUT4-1 pin description - TEST_MODE2-0 pin description - TEST_IN4-0 pin description - MTPD/MTPG pin description - PregB(DSTB_EN) pin description 4. PAD name changed. - TEST_OUT0 → FLM/TEST_OUT0 - DUMMY → EX_CLK - PregB → DSTB_EN - MVDD → VDDM 5. Application circuit Preliminary version added. 6. Table 53 “RADJ and Internal oscillator oscillation frequency” revised. 7. VRP0/VRN0 bit width changed. (Instruction table error) 8. R12h SVC register field changed. / description modified 9. R12h VCIREX_EN → Deleted 10. Register for MTP function (R73h, RB3h, RB4h, RBDh) added. 11. R02h FL register description modified. 12. R07h PT register decription modified. 13. Deep Stand-by IN/OUT sequence added.	H.J. Kim	October 26, 2005

0.4	1. Output Bump size changed - 20x105 um^2 → 21x105 um^2 2. Pin name corrected. - Pin configuration : VSSO → VSS - PAD Coordinates : VSSO → VSS - Application circuit : VSSO → VSS 3. PAD configuration " Top View description" added. 4. R70h, R71h "Note" added. 5. COG align mark Coordinate added. 6. Pattern diagram changed - VREG1OUT "Note" added - VREGP → VREFS - SVC3-0 added 7. Set up flow of Power Supply - SVC3-0 added 8. Oscillation circuit pin name changed OSC_MON → EX_CLK	H.J. Kim	October 27, 2005
0.5	1. MTP Flow diagrams are added. 2. BP, FP Timing diagrams are added. 3. R01h NL register description modified. - NL = 5'b10011 → NL=5'b10100 4. R42h SE1 register description modified. - SS1[7:0] ≤ SE1[7:0] ≤"13F"h → SS1[7:0] ≤ SE1[7:0] ≤"9F"h 5. Timing Diagram FIG 75 modified - VCOM toggle timing inserted. 6. Interlace Scanning Function FIG 77, FIG 78 modified. 7. Absolue maximum rating added. - MTP maximum rewritable time added. 8. DC characteristic added. - MTP current specification added. - RON measurement condition modified. 9. R12h SVC table revised. - SVC[3-0]="1100"~"1111" setting disable. 10. PAD name changed. - TEST_MODE2 → TEST_MODE 11. Application circuit modified. - Increasing readability 12. VCOM setting section added. 13. EX_CLK pin description modified. - Operation clock range added.	J.S. Kang	November 9, 2005

0.6	1. Figures of GS, SM are modified. 2. Graphic Operation Table (Table 36) is removed. 3. GRAM Data Alignment in 22h Description is removed. 4. Notation of equality is changed("==" ➔ "=") 5. Panel IF Timing Parameters using DOTCLK are removed. 6. PT Description is modified 7. Direction of TEST_MODE, NDT_EN is described. 8. INDEX width is expaned (7bits ➔ 8bits) 9. Relationship between DCCLK and DISP_CK is described. 10. Panel IF Timing Diagrams(Figure75, 77, 78) are modified. 11. Timing Diagram of BP, FP (Figure13) is modified. 12. RESET Initial Values are described. 13. VCOM Amplitude Control Table is modified. 14. Set-up Flow of Power Supply figure is modified. 15. Pattern Diagram And An Example Of Waveforms figure is moidfied. 16. Deep Stand-by IN/OUT sequence is modified. 17. DC Characteristics for LCD driver outputs Table is modified. - SAP=001 setting is removed. 18. RWB_RDB, E_WRB pin coordinates are changed. - PAD Center Coordinate Table is modified. - Application Circuit Figure is modified. - PAD Configuration Figure is modified. 19. Application Circuit is modified. - VCOMR external resistance is reduced. 20. MTPG, MTPD(21p) - Voltage range modified. 21. DC characteristic - MTPG, MTPD voltage condition added. - SAP=010 60us → 80us. 22. SAP - SAP=001 removed. 23. R13h PON description is revised. 24. R69h NLDC description is revised. 25. Voltage Regulation Function (Figure31) modified.	J.S Kang	December 12, 2005
0.7	1.P27 Gamma control Gamma control register → Gamma control 2. P48 VR1C bit IB14 → IB15 3. P56 PRP5[2:0]~PRP2[2:0], PRN5[2:0]~PRN2[2:0] removed 4. P114 100000 → 10000 5. P116 SUMRN removed 6. P118 SUMRP removed 7. P117 table changed 8. P75 Interface mode selection function. - RBEh register set is added. 9. P106 Figure75 is modified - NO → GNO 10. P54 table is inserted - R22H → R22h 11. P31 Figure6 is modified. 12. P27 Table17 is modifed.	C.W Park	January 6, 2006

NOTICE

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.