PI74AVC+16836

2.5V 20-Bit Universal Bus Driver with 3-State Outputs

Features

- PI74AVC+16836 is designed for low-voltage operation, V_{CC} = 1.65V to 3.6V
- True ±24mA Balanced Drive @ 3.3V
- I_{OFF} supports partial power-down operation
- 3.6V I/O Tolerant inputs and outputs
- Meets PC133 SDRAM Registered DIMM Specifications
- All outputs contain a patented DDC (Dynamic Drive Control) circuit that reduces noise without degrading propagation delay
- Industrial operation: –40°C to +85°C
- Packaging (Pb-free & Green available):
  – 56-pin 240-mil wide plastic TSSOP (A)

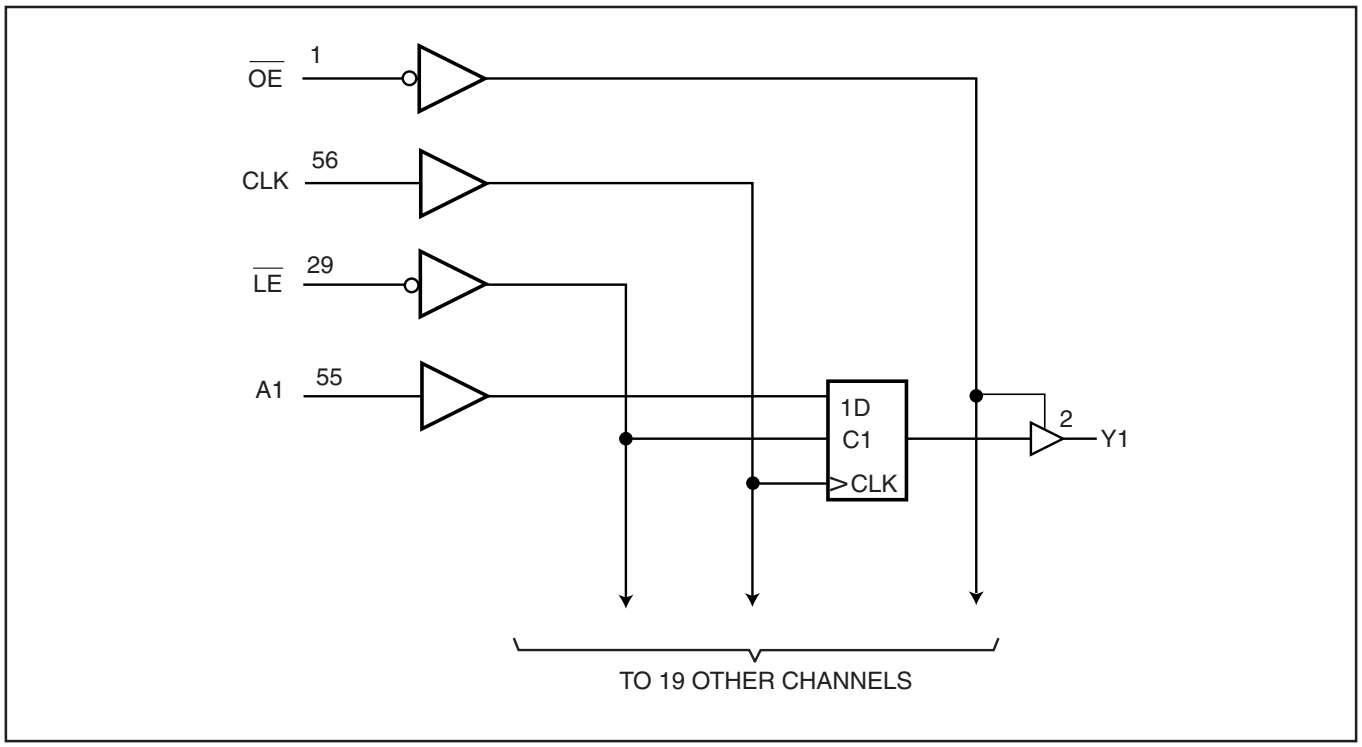
Description

Pericom Semiconductor's 20-bit PI74AVC+16836 universal bus driver is designed for 1.65V to 3.6V V_{CC} operation.

Data flow from A to Y is controlled by the Output Enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable ($\overline{LE}$) input is LOW. When $\overline{LE}$ is HIGH, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is HIGH, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state, but all the inputs are enabled and data is capable of being stored in the register.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Block Diagram



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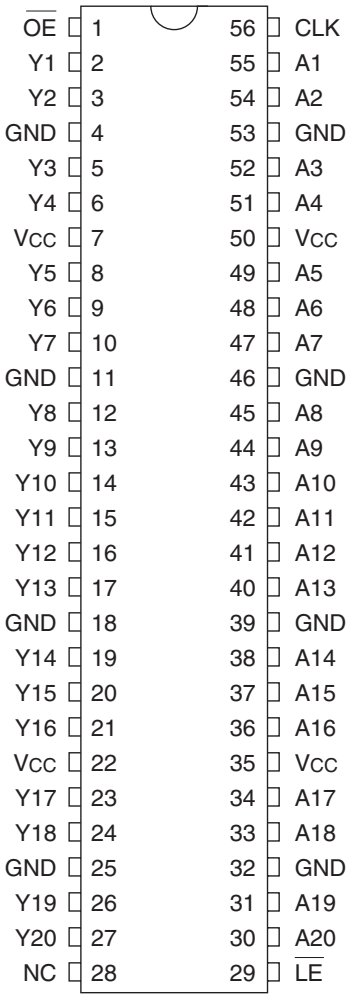
Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{LE}$	Latch Enable (Active LOW)
CLK	Clock Input
A	Data Input
Y	Data Output
GND	Ground
Vcc	Power

Pin Configuration



Truth Table(1)

Inputs				Outputs
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Yo(2)

Notes:

1. H = High Signal Level
   L = Low Signal Level
   Z = High Impedance
   ↑ = Transition LOW-to-HIGH
   X = Irrelevant
2. Output level before the indicated steady-state input conditions were established.

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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply voltage range, V_{CC} ..... –0.5V to +4.6V
Input voltage range, V_I ..... –0.5V to +4.6V
Voltage range applied to any output in the high-impedance or power-off state, V_O[1] ..... –0.5V to +4.6V
Voltage range applied to any output in the high or low state, V_O[1,2] ..... –0.5V to V_{CC} +0.5V
Input clamp current, I_{IK} (V_I <0) ..... –50mA
Output clamp current, I_{OK} (V_O <0) ..... –50mA
Continuous output current, I_O ..... ±50mA
Continuous current through each V_{CC} or GND ..... ±100mA
Package thermal impedance, θ_{JA}[3]: ..... 64°C/W
Storage Temperature range, T_{stg} ..... –65°C to 150°C

Notes:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1. Input & output negative-voltage ratings may be exceeded if the input and output curent rating are observed.
2. Output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions[1]

		Min.	Max.	Units
V_{CC} Supply Voltage	Operating	1.65	3.6	V
	Data retention only	1.2		
V_{IH} High-level Input Voltage	V_{CC} = 1.2V	V_{CC}		
	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}		
	V_{CC} = 2.3V to 2.7V	1.7		
	V_{CC} = 3V to 3.6V	2		
V_{IL} Low-level Input Voltage	V_{CC} = 1.2V		Gnd	
	V_{CC} = 1.65V to 1.95V		0.35 x V_{CC}	
	V_{CC} = 2.3V to 2.7V		0.7	
	V_{CC} = 3V to 3.6V		0.8	
V_I Input Voltage		0	3.6	
V_O Output Voltage	Active State	0	V_{CC}	
	3-State	0	3.6	
I_{OH} High-level output current	V_{CC} = 1.65V to 1.95V		–6	mA
	V_{CC} = 2.3V to 2.7V		–12	
	V_{CC} = 3V to 3.6V		–24	
I_{OL} Low-level output current	V_{CC} = 1.65V to 1.95V		6	
	V_{CC} = 2.3V to 2.7V		12	
	V_{CC} = 3V to 3.6V		24	
$\Delta t/\Delta v$ Input transition rise or fall rate	V_{CC} = 1.65V to 3.6V		5	ns/V
T_A Operating free-air temperature		–40	85	°C

Notes:
1. All unused inputs must be held at V_{CC} or GND to ensure proper device operation.

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DC Electrical Characteristics (Over the Operating Range, T_A = –40°C +85°C)

Parameters		Test Conditions[1]		V_{CC}	Min.	Max.	Units
V_{OH}		I_{OH} = –100µA		1.65V to 3.6V	V_{CC} –0.2V		V
		I_{OH} = –6mA	V_{IH} = 1.07V	1.65V	1.2		
		I_{OH} = –12mA	V_{IH} = 1.7V	2.3V	1.75		
		I_{OH} = –24mA	V_{IH} = 2V	3V	2.0		
V_{OL}		I_{OL} = 100µA		1.65V to 3.6V		0.2	
		I_{OL} = 6mA	V_{IH} = 0.57V	1.65V		0.45	
		I_{OL} = 12mA	V_{IH} = 0.7V	2.3V		0.55	
		I_{OL} = 24mA	V_{IH} = 0.8V	3V		0.8	
I_I		V_I = V_{CC} or GND		3.6V		±2.5	µA
I_{OFF}		V_I or V_O = 3.6V		0		±10	
I_{OZ}		V_I = V_{CC} or GND		3.6V		±10	
I_{CC}		V_O = V_{CC} or GND	I_O = 0	3.6V		40	
C_I	Control Inputs	V_I = V_{CC} or GND		2.5V		4	pF
				3.3V		4	
	Data Inputs			2.5V		6	
				3.3V		6	
C_O	Outputs	V_O = V_{CC} or GND		2.5V		8	
				3.3V		8	

Notes:
1. Typical values are measured at T_A = 25°C.

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

			V_{CC} = 1.2V	V_{CC} = 1.5V ±0.1V		V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
			Typical	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{clock}	Clock Frequency						150		150		150	MHz
t_w Pulse Duration	$\overline{LE}$ Low					3.3		3.3		3.3		ns
	CLK High or Low					3.3		3.3		3.3		
t_{su} Setup Time	Data before CLK↑		2.2	1.6		1.4		1.0		1.0		
	Data before $\overline{LE}$↑	CLK High	1.7	1.6		1.2		1.2		1.0		
		CLK Low	1.2	1.0		1.4		1.2		1.0		
t_h Hold Time	Data after CLK↑		1.0	1.0		1.0		0.8		0.6		
	Data after $\overline{LE}$↑	CLK High or Low	1.0	1.0		1.0		0.8		0.6		

Switching Characteristics

(Over recommended operating free-air temperature range, unless otherwise noted, see Figures 1 thru 4)

Parameters	From (Input)	To (Output)	V_{CC} = 1.2V	V_{CC} = 1.5V ±0.1V		V_{CC} = 1.8V ±0.15V		V_{CC} = 2.5V ±0.2V		V_{CC} = 3.3V ±0.3V		Units
			Typical	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{max}						150		150		150		MHz
t_{pd}	A	Y	5.4		4.0	1.0	4.5	0.8	3.0	0.7	2.4	ns
	$\overline{LE}$		6.8		4.6	1.0	4.5	0.8	3.3	0.7	2.5	
	CLK		7.8		5.0	1.0	4.5	0.8	3.3	0.7	2.5	
t_{en}	$\overline{OE}$		6.2		5.0	1.5	4.5	1.0	4.5	1.0	4.0	
t_{dis}	$\overline{OE}$		5.5		4.5	1.5	4.5	1.0	4.5	1.0	4.0	

Operating Characteristics, T_A = 25°C

Parameters		Test Conditions	V_{CC} = 1.8V ±0.1V	V_{CC} = 2.5V ±0.2V	V_{CC} = 3.3V ±0.3V	Units
			Typical	Typical	Typical	
C_{pd} Power Dissipation Capacitance	Outputs Enabled	C_L = 0pF, f = 10 MHz	45	48	52	pF
	Outputs Disabled		23	25	28	

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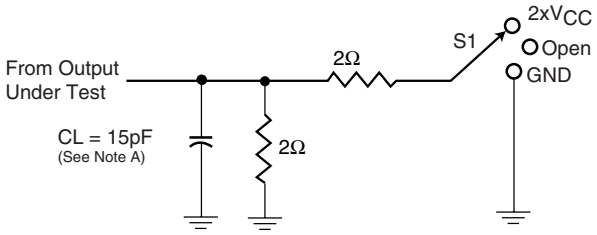
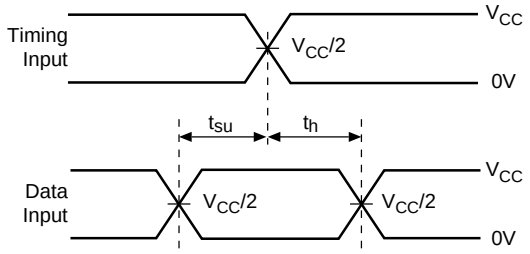
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.2V and 1.5V ±0.1V

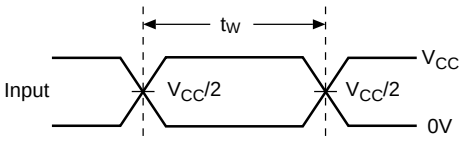


Test	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

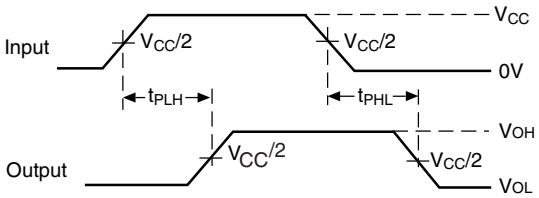
Load Circuit



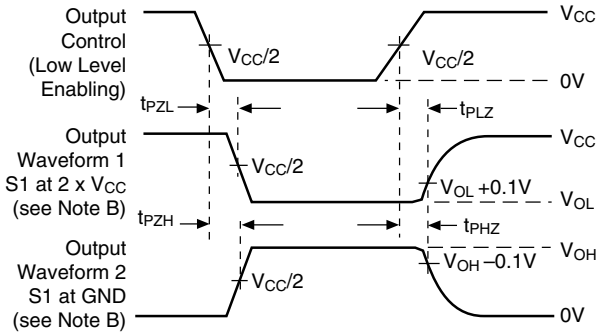
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 1. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

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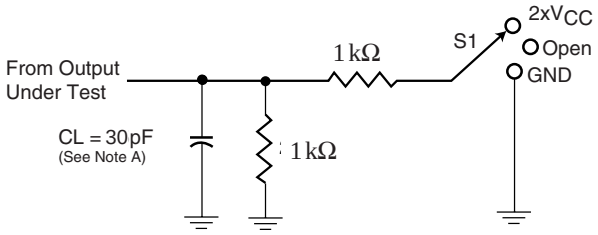
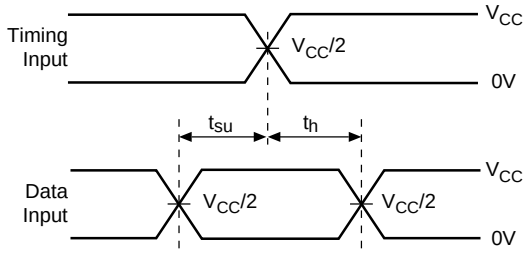
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 1.8V ±0.15V

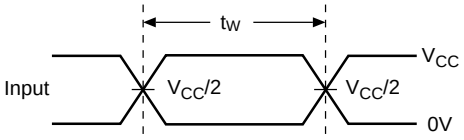


Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND

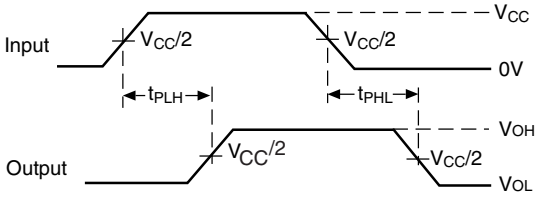
Load Circuit



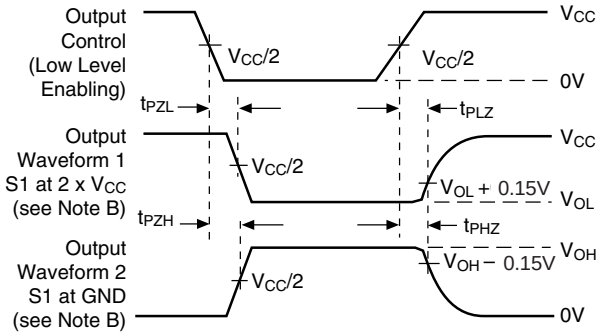
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 2. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- All input impulses are supplied by generators having these characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

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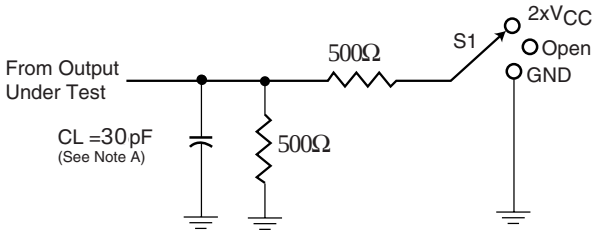
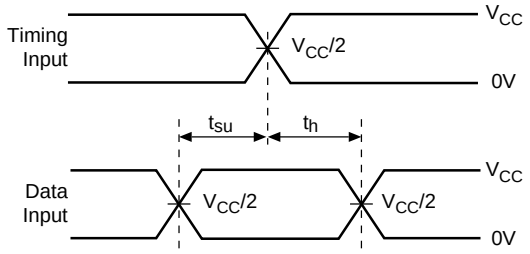
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 2.5V ±0.2V

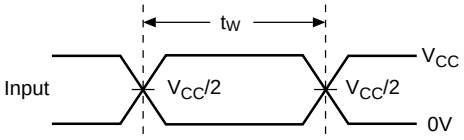


Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND

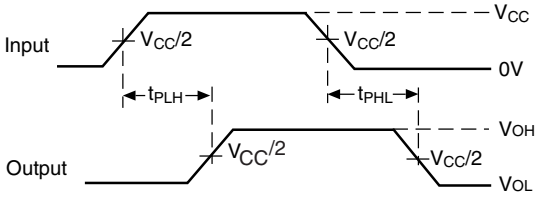
Load Circuit



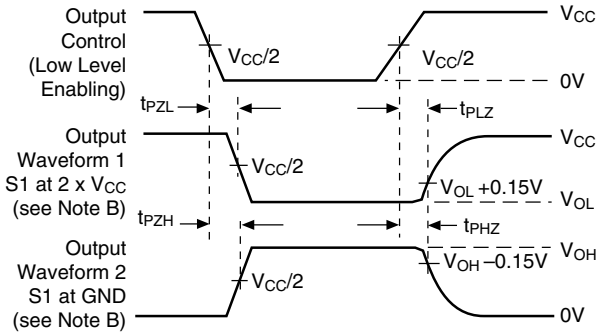
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 3. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- All input impulses are supplied by generators having these characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

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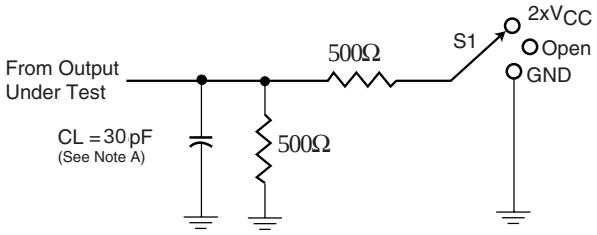
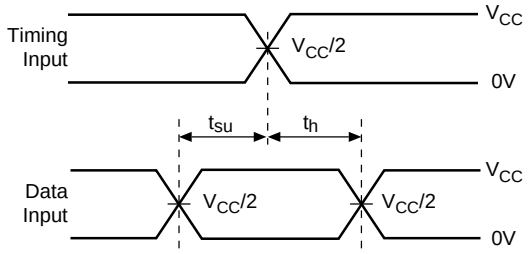
PARAMETER MEASUREMENT INFORMATION
V_{CC} = 3.3V ±0.3V

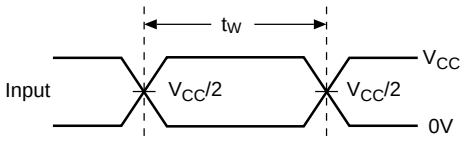


Test	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 x V_{CC} GND

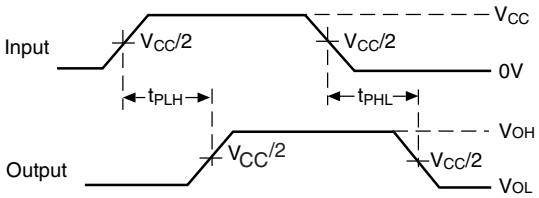
Load Circuit



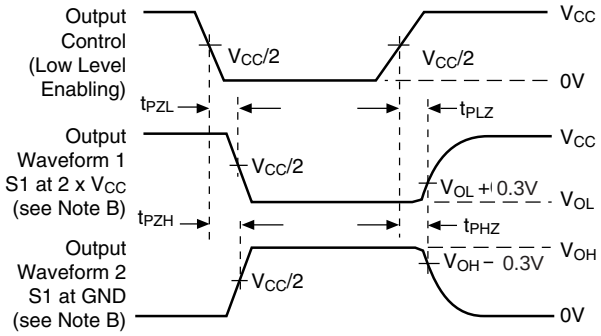
Voltage Waveforms
Setup and Hold Times



Voltage Waveforms
Pulse Duration



Voltage Waveforms
Propagation Delay Times



Voltage Waveforms
Enable and Disable Times

Figure 4. Load Circuit and Voltage Waveforms

Notes:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- All input impulses are supplied by generators having these characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2.0ns, t_F ≤ 2.0ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}
- t_{PZL} and t_{PZH} are the same as t_{en}
- t_{PLH} and t_{PHL} are the same as t_{pd}

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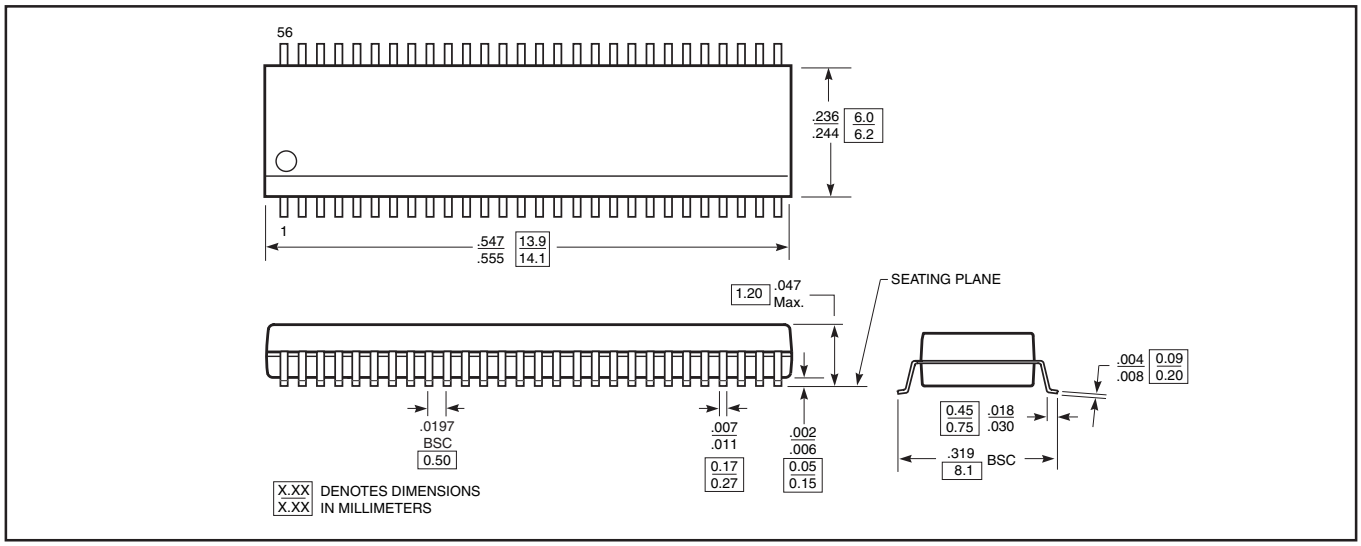
Packaging Mechanical: 56-pin TSSOP (A)



Ordering Information

Ordering Code	Package Code	Package Type
PI74AVC+16836A	A	56-pin, 240-mil wide plastic TSSOP
PI74AVC+16836AE	A	Pb-free & Green, 56-pin, 240-mil wide plastic TSSOP

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- Adding an X suffix = Tape/Reel