DDR3 SDRAM UDIMM

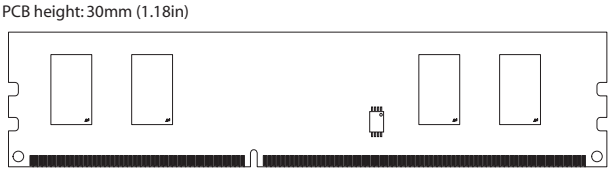
MT4JTF6464AY – 512MB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- DDR3 functionality and operations supported as per component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates: PC3-10600, PC3-8500, or PC3-6400
- 512MB (64 Meg x 64)
- $V_{DD} = V_{DD}Q = +1.5V \pm .075V$
- $V_{DDSPD} = +3.0V$ to $+3.6V$
- Reset pin for improved system stability
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Single rank
- 8 internal device banks for concurrent operation
- Fixed burst length of 8 (BL8) and burst chop of 4 (BC4) via the mode register
- Adjustable data-output drive strength
- Serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Pb-free
- Fly-by topology
- Terminated command, address, and control bus

Figure 1: 240-Pin UDIMM (MO-269 R/C C)



Options	Marking
• Operating temperature[1]	
– Commercial ($0°C \le T_A \le +70°C$)	None
– Industrial ($–40°C \le T_A \le +85°C$)	I
• Frequency/CAS latency	
– 1.5ns @ CL = 9 (DDR3-1333)	-1G4
– 1.5ns @ CL = 10 (DDR3-1333)	-1G3
– 1.87ns @ CL = 7 (DDR3-1066)	-1G1
– 1.87ns @ CL = 8 (DDR3-1066)	-1G0
– 2.5ns @ CL = 5 (DDR3-800)	-80C
– 2.5ns @ CL = 6 (DDR3-800)	-80B

Notes: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)						^tRCD (ns)	^tRP (ns)	^tRC (ns)
		CL = 10	CL = 9	CL = 8	CL = 7	CL = 6	CL = 5			
-1G4	PC3-10600	–	1333	1066	800	–	–	13.5	13.5	49.5
-1G3	PC3-10600	1333	1066	800	–	–	–	15	15	51
-1G1	PC3-8500	–	–	–	1066	800	–	13.125	13.125	50.625
-1G0	PC3-8500	–	–	1066	800	–	–	15	15	52.5
-80C	PC3-6400	–	–	–	–	–	800	12.5	12.5	50
-80B	PC3-6400	–	–	–	–	800	–	15	15	52.5

Table 2: Addressing

Parameter	512MB
Refresh count	8K
Row address	8K (A0–A12)
Device bank address	8 (BA0–BA2)
Device page size per bank	1KB
Device configuration	1Gb (64 Meg x 16)
Column address	1K (A0–A9)
Module rank address	1 (S0#)

Table 3: Part Numbers and Timing Parameters 512MB Modules

Base device: MT41J64M16[1], 1Gb DDR3 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	CL-^{t}RCD-^{t}RP (Clock Cycles)
MT4JTF6464AY-1G4__	512MB	64 Meg x 64	10.7 GB/s	1.5ns/1333 MT/s	9-9-9
MT4JTF6464AY-1G3__	512MB	64 Meg x 64	10.7 GB/s	1.5ns/1333 MT/s	10-10-10
MT4JTF6464AY-1G1__	512MB	64 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	7-7-7
MT4JTF6464AY-1G0__	512MB	64 Meg x 64	8.5 GB/s	1.87ns/1066 MT/s	8-8-8
MT4JTF6464AY-80C__	512MB	64 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT4JTF6464AY-80B__	512MB	64 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6

Notes:
1. Data sheets for the base device parts can be found on Micron's Web site.
2. All numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT4JTF6464AY-1G1B1.

Pin Assignments and Descriptions

Table 4: Pin Assignment

240-Pin UDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41
2	VSS	32	VSS	62	VDD	92	VSS
3	DQ0	33	DQS3#	63	CK1	93	DQS5#
4	DQ1	34	DQS3	64	CK1#	94	DQS5
5	VSS	35	VSS	65	VDD	95	VSS
6	DQS0#	36	DQ26	66	VDD	96	DQ42
7	DQS0	37	DQ27	67	VREFCA	97	DQ43
8	VSS	38	VSS	68	NC	98	VSS
9	DQ2	39	NC	69	VDD	99	DQ48
10	DQ3	40	NC	70	A10	100	DQ49
11	VSS	41	VSS	71	BA0	101	VSS
12	DQ8	42	NC	72	VDD	102	DQS6#
13	DQ9	43	NC	73	WE#	103	DQS6
14	VSS	44	VSS	74	CAS#	104	VSS
15	DQS1#	45	NC	75	VDD	105	DQ50
16	DQS1	46	NC	76	NC	106	DQ51
17	VSS	47	VSS	77	NC	107	VSS
18	DQ10	48	NC	78	VDD	108	DQ56
19	DQ11	49	NC	79	NC	109	DQ57
20	VSS	50	CKE0	80	VSS	110	VSS
21	DQ16	51	VDD	81	DQ32	111	DQS7#
22	DQ17	52	BA2	82	DQ33	112	DQS7
23	VSS	53	NC	83	VSS	113	VSS
24	DQS2#	54	VDD	84	DQS4#	114	DQ58
25	DQS2	55	A11	85	DQS4	115	DQ59
26	VSS	56	A7	86	VSS	116	VSS
27	DQ18	57	VDD	87	DQ34	117	SA0
28	DQ19	58	A5	88	DQ35	118	SCL
29	VSS	59	A4	89	VSS	119	SA2
30	DQ24	60	VDD	90	DQ40	120	VTT

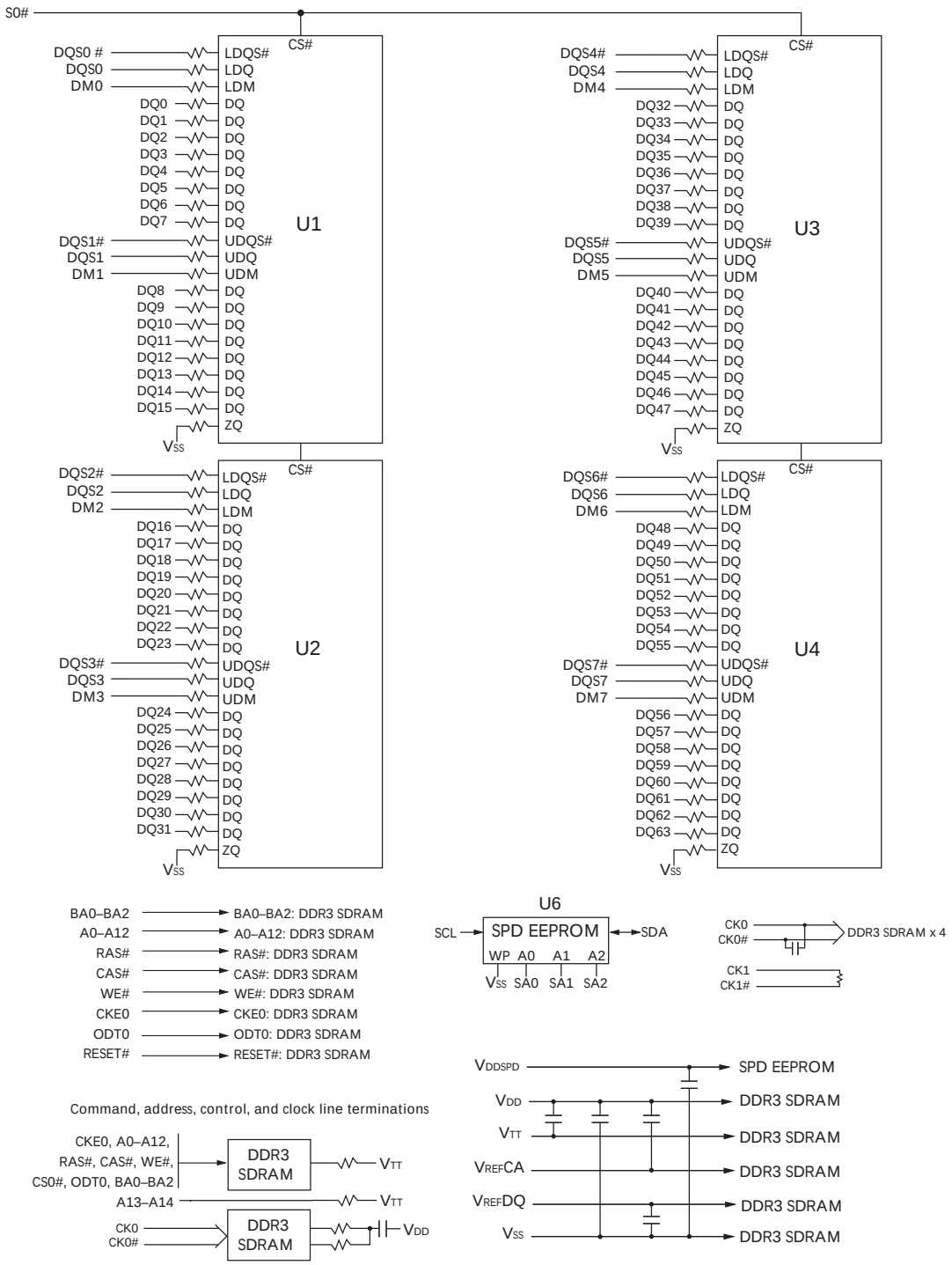
240-Pin UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VSS	151	VSS	181	A1	211	VSS
122	DQ4	152	DM3	182	VDD	212	DM5
123	DQ5	153	NC	183	VDD	213	NC
124	VSS	154	VSS	184	CK0	214	VSS
125	DM0	155	DQ30	185	CK0#	215	DQ46
126	NC	156	DQ31	186	VDD	216	DQ47
127	VSS	157	VSS	187	NC	217	VSS
128	DQ6	158	NC	188	A0	218	DQ52
129	DQ7	159	NC	189	VDD	219	DQ53
130	VSS	160	VSS	190	BA1	220	VSS
131	DQ12	161	NC	191	VDD	221	DM6
132	DQ13	162	NC	192	RAS#	222	NC
133	VSS	163	VSS	193	S0#	223	VSS
134	DM1	164	NC	194	VDD	224	DQ54
135	NC	165	NC	195	ODT0	225	DQ55
136	VSS	166	VSS	196	NC	226	VSS
137	DQ14	167	NC	197	VDD	227	DQ60
138	DQ15	168	RESET#	198	NC	228	DQ61
139	VSS	169	NC	199	VSS	229	VSS
140	DQ20	170	VDD	200	DQ36	230	DM7
141	DQ21	171	NC	201	DQ37	231	NC
142	VSS	172	NC	202	VSS	232	VSS
143	DM2	173	VDD	203	DM4	233	DQ62
144	NC	174	A12	204	NC	234	DQ63
145	VSS	175	A9	205	VSS	235	VSS
146	DQ22	176	VDD	206	DQ38	236	VDDSPD
147	DQ23	177	A8	207	DQ39	237	SA1
148	VSS	178	A6	208	VSS	238	SDA
149	DQ28	179	VDD	209	DQ44	239	VSS
150	DQ29	180	A3	210	DQ45	240	VTT

Table 5: Pin Descriptions

Symbol	Type	Description
A0–A12	Input	**Address inputs:** Provide the row address for ACTIVE commands and the column address and auto precharge bit for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. The address inputs also provide the op-code during the mode register command set.
BA0–BA2	Input	**Bank address inputs:** BA0–BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. BA0–BA2.
CK0, CK0#	Input	**Clock:** CK0 and CK0# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR3 SDRAM.
DM0–DM7	Input	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
ODT0	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** An active LOW CMOS input referenced to V_{SS} and not referenced to $V_{REF}CA$ or $V_{REF}DQ$. The reset pin input receiver is a CMOS input and is defined as a rail-to-rail signal with a DC HIGH ≥ 0.8 x $V_{DD}Q$ and DC LOW ≤ 0.2 x $V_{DD}Q$ (1.20V for HIGH and 0.30V for LOW). RESET# assertion and desertion are asynchronous. System applications will most likely be unterminated, heavily loaded, and have very slow slew rates. A slow slew rate receiver design is recommended along with implementing on-chip noise filtering to prevent false triggering (RESET# assertion minimum pulse width is 100ns).
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. With both inputs HIGH, all outputs of the register(s) are disabled except for CKE and ODT. CKE, ODT and chip select remain in previous state when both outputs are HIGH.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module.
DQ0–DQ63	I/O	**Data input/output:** Bidirectional data bus.
DQS0–DQS7 DQS0#–DQS7#	I/O	**Data strobe:** Output with READ data, input with WRITE data for source synchronous operation. Edge-aligned with READ data, center-aligned with WRITE data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +3.0V to +3.6V.
$V_{REF}DQ$	Supply	**Reference voltage:** DQ, DM. $V_{DD}/2$.
$V_{REF}CA$	Supply	**Reference voltage:** Command, address, and control. $V_{DD}/2$.
V_{SS}	Supply	**Ground.**
V_{TT}	Supply	**Termination voltage:** Used for address, command, control, and clock nets. $V_{DD}/2$.
NC	–	**No connect:** These pins should be left unconnected.

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. ZQ ball on each DDR3 component is connected to an external 240Ω resistor that is tied to ground. Used for the calibration of the component's on-die termination and output driver.

General Description

The MT4JTF6464AY DDR3 SDRAM module is a high-speed, CMOS, dynamic random-access 512MB memory module organized in a x64 configuration. This DDR3 SDRAM module uses an internally configured 8-bank (1Gb) DDR3 SDRAM device.

DDR3 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR3 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR3 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Fly-By Topology

DDR3 modules utilize faster clock speeds than earlier DDR technologies, making signal quality more important than ever. To ensure the best possible signal quality the clock and command/address busses have been routed in a fly-by topology, where each clock and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by utilizing the write leveling feature of DDR3.

Serial Presence-Detect Operation

DDR3 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 6, may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}[1]	V_{DD} supply voltage relative to V_{SS}		–0.4	+1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.4	+1.975	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, S#, CKE, ODT, BA	–4	+4	µA
		CK, CK#	–1	+1	
		DM	–1	+1	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ $V_{DD}Q$; DQs and ODT are disabled	DQ, DQS, DQS#	–1	+1	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–8	+8	µA

Notes: 1. V_{REF} must not be greater than 0.6 x V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be equal to or less than 300mV.

Table 7: Operating Conditions

Symbol	Parameter		Min	Max	Units
I_{VTT}	Termination reference current from V_{TT}		–600	+600	mA
V_{TT}[1]	Termination reference voltage – command address bus		–0.483 x V_{DD}	+0.517	V
T_A[2,4]	Module ambient operating temperature1	Commercial	0	+70	°C
		Industrial	–40	+85	°C
T_C[2,4]	DDR3 SDRAM component case operating temperature [3]	Commercial	0	+85	°C
		Industrial	–40	+95	°C

Notes:
1. V_{TT} termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. Refresh rate is required to double when 85°C < T_C ≤ 95°C.
4. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades

DDR3 components must be able to meet or exceed the listed speed grade.

Module Speed Grade	Component Speed Grade
-1G4	-15E
-1G3	-15
-1G1	-187E
-1G0	-187
-80C	-25E
-80B	-25

IDD Specifications

Table 9: DDR3 IDD Specifications and Conditions – 512MB

Values shown for each data rate are for the MT41J64M16 DDR3 SDRAM only and are computed from values specified in the 1Gb (64 Meg x 16) component data sheet

Parameter	Symbol	1333	1067	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	IDD0	620	560	480	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	IDD1	780	700	620	mA
Precharge power down current: Slow exit	IDD2P	40	40	40	mA
Precharge power down current: Fast exit	IDD2P	100	100	100	mA
Precharge quiet standby current	IDD2Q	280	240	200	mA
Precharge standby current	IDD2N	300	260	220	mA
Active power-down current	IDD3P	220	180	160	mA
Active standby current	IDD3N	380	320	260	mA
Burst read operating current	IDD4R	1,320	1,120	920	mA
Burst write operating current	IDD4W	1,600	1,400	1,200	mA
Refresh current	IDD5B	1,160	1,020	860	mA
Self-refresh temperature current (SRT-enabled): MAX T_C = 95°C	IDD6ET	36	36	36	mA
Self-refresh temperature current: MAX T_C = 85°C	IDD6	24	24	24	mA
All bank interleaved read current	IDD7	2,780	2,660	2,540	mA

Serial Presence-Detect

Table 10: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 kHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	ICC_W	2	3	mA

Table 11: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	kHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Table 12: Serial Presence-Detect Matrix

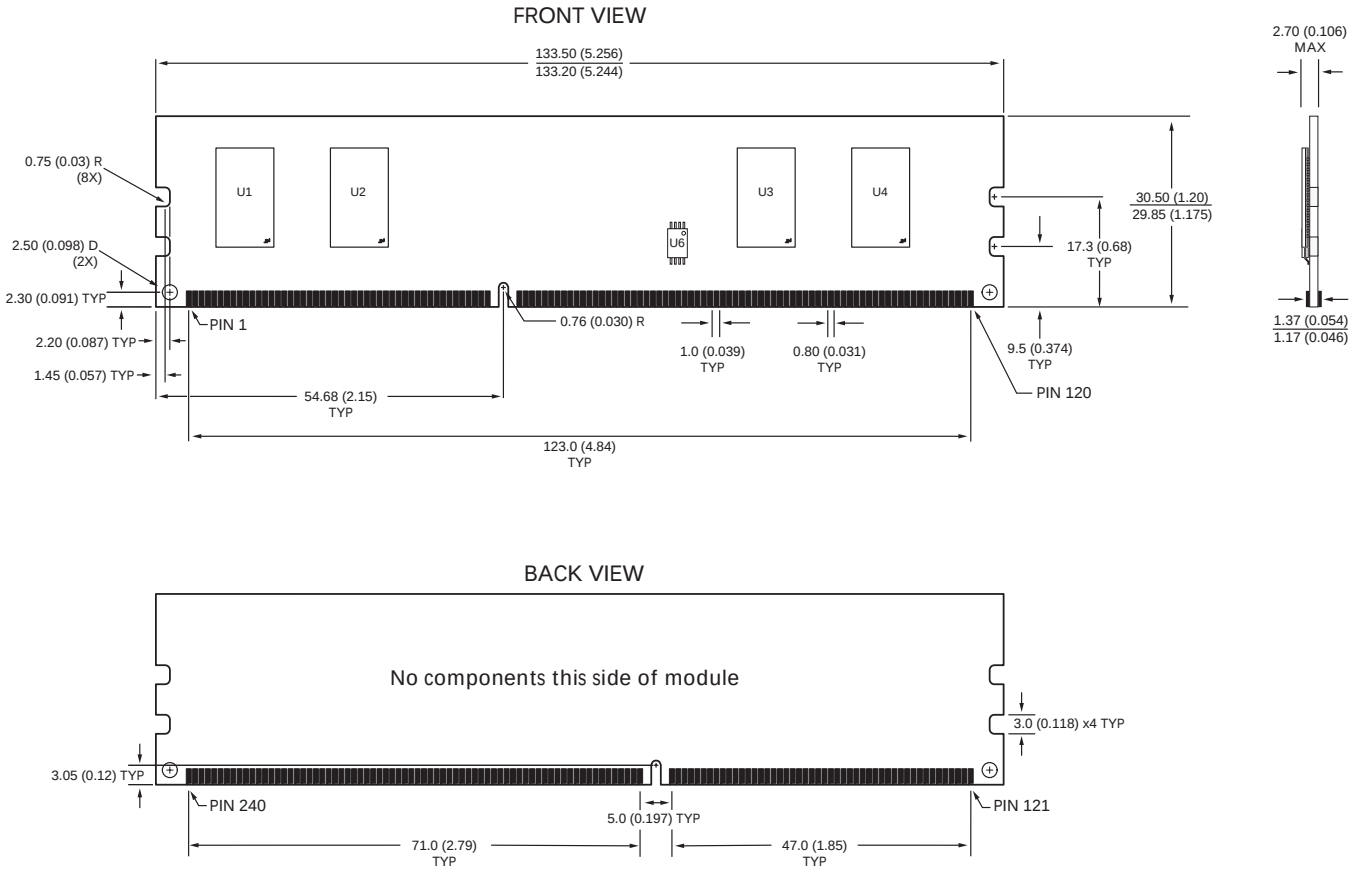
Byte	Description	Entry (Version)	512MB
0	CRC coverage EEPROM device size Number of SPD bytes written	Bytes 0–116 256 bytes 176 bytes	 92
1	SPD revision	Rev 1.0	10
2	DRAM device type (technology)	DDR3 SDRAM	0B
3	Module type (form factor)	UDIMM	02
4	SDRAM device density and internal banks	1Gb/8 banks	02
5	SDRAM device addressing (row and column counts)	(13, 10)	09
6	Reserved	0	00
7	Module organization (module ranks, SDRAM device width)	1 rank, x16 I/O	02
8	Module memory bus width	No ECC, 64-bit	03
9	Fine time base (FTB) dividend/divisor	5/2	52
10	Medium time base (MTB) dividend	1	01
11	Medium time base (MTB) divisor	8	08
12	SDRAM devise minimum cycle time (^{t}CK [MIN])	-1G4/-1G3/-1G1/-1G0 -80C/-80B	0F 14
13	Reserved	0	00
14	CAS latencies supported, low byte	-1G4 -1G3 -1G1 -1G0 -80C -80B	34 54 1C 14 06 04
15	CAS latencies supported, high byte	0	00
16	MIN CAS latency time (^{t}AA [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78
17	MIN write recovery time (^{t}WR [MIN])		78
18	MIN RAS# to CAS# delay time (^{t}RCD [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78
19	MIN row active-to-row active delay time (^{t}RRD [MIN])	-1G4/-1G3 -1G1/-1G0/-80C/-80B	3C 50
20	MIN row precharge delay time (^{t}RP [MIN])	-1G4 -1G3 -1G1 -1G0 -80C -80B	6C 78 69 78 64 78
21	Upper nibble for ^{t}RAS and ^{t}RC		11
22	MIN active-to-precharge delay time (^{t}RAS [MIN]), LSB	-1G4/-1G3 -1G1/-1G0/-80C/-80B	20 2C

Table 12: Serial Presence-Detect Matrix (continued)

Byte	Description	Entry (Version)	512MB
23	MIN active-to-active/refresh (^{t}RC [MIN]), LSB	-1G4 -1G3 -1G1 -1G0 -80C -80B	8C 98 95 A4 90 A4
24	MIN refresh recovery delay time (^{t}RFC [MIN]), LSB	1Gb	70
25	MIN refresh recovery delay time (^{t}RFC [MIN]), MSB	1Gb	03
26	MIN internal WRITE-to-READ command delay time (^{t}WTR [MIN])		3C
27	MIN internal READ-to-PRECHARGE command delay time (^{t}RTP [MIN])		3C
28	MIN four active window delay time (^{t}FAW [MIN]) upper nibble		01
29	MIN four activate window delay time (^{t}FAW [MIN]), LSB	-1G4/-1G3 -1G1/-1G0/-80C/-80B	68 90
30	SDRAM device output drivers supported		82
31	SDRAM device thermal refresh options		05
32–59	Reserved, general section		00
60	Module NOM height	30mm	0F
61	Module MAX thickness	Single rank, 2.7mm	01
62	Reference raw card used	UDIMM R/C C	02
63	Address mapping from edge connector to DRAM devices	Standard	00
64–116	Reserved	0	00
117	Module manufacturer ID (continuation code)		80
118	Module manufacturer ID (manufacturer's ID code)		2C
119	Module manufacturing location	1–12	01-0C
120–121	Module manufacturing date	–	Variable data
122–125	Module serial number	–	Variable data
126, 127	CRC (cyclic redundancy check)	-1G4 -1G3 -1G1 -1G0 -80C -80B	838E 6091 65D5 D620 31F0 3E01
128–145	Module part number (ASCII)	–	Variable data
146	Module revision code, SDRAM device die revision	–	Variable data
147	Module revision code, PCB revision	–	Variable data
148	DRAM device manufacturer ID (continuation code)		80
149	DRAM device manufacturer ID (manufacturer's ID code)		2C
150–175	Reserved for manufacturer-specific data		00
176–255	Reserved for customer-specific data		FF

Module Dimensions

Figure 3: 240-Pin DDR3 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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