Mobile DDR SDRAM Addendum

MT46H64M16LF – 16 Meg x 16 x 4 banks
MT46H32M32LF – 8 Meg x 32 x 4 banks

Features

- VDD/VDDQ = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16[1]
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes[2]
- 1.8V LVCMOS-compatible inputs
- On-chip temperature sensor to control self refresh rate[2]
- Partial-array self refresh (PASR)[2]
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive strength (DS)
- Clock stop capability
- 64ms refresh ≤ +85°C
- 16ms refresh ≤ +105°C

Notes: 1. Contact factory for availability of BL16.
2. Self refresh only supported ≤ +85°C.

Options — Marking

- VDD/VDDQ
  - 1.8V/1.8V — H
- Configuration
  - 64 Meg x 16 (16 Meg x 16 x 4 banks) — 64M16
  - 32 Meg x 32 (8 Meg x 32 x 4 banks) — 32M32
- Row-size option
  - JEDEC-standard option — LF
  - Reduced page-size option[1] — LG
- Plastic "green" package
  - 60-ball VFBGA (10mm x 11.5mm)[2] — CK
  - 90-ball VFBGA (10mm x 13mm)[3] — CM
- Timing – cycle time
  - 5ns @ CL = 3 — -5
  - 5.4ns @ CL = 3 — -54
  - 6ns @ CL = 3 — -6
  - 7.5ns @ CL = 3 — -75
- Operating temperature range
  - Automotive (–40°C to +105°C) — AT
- Revision — :A

Notes: 1. Contact factory for availability.
2. Only available for x16 configuration.
3. Only available for x32 configuration.

Table 1: Key Timing Parameters (CL = 3)

Speed Grade	Clock Rate (MHz)	Access Time
-5	200	5.0ns
-54	185	5.0ns
-6	166	5.5ns
-75	133	6.0ns

Table 2: Configuration Addressing

Architecture	64 Meg x 16	32 Meg x 32	Reduced Page-Size Option 32 Meg x 32
Configuration	16 Meg x 16 x 4 banks	8 Meg x 32 x 4 banks	8 Meg x 32 x 4 banks
Refresh count	8K	8K	8K
Row addressing	16K (A0–A13)	8K (A0–A12)	16K (A0–A13)
Column addressing	1K (A0–A9)	1K (A0–A9)	512 (A0–A8)

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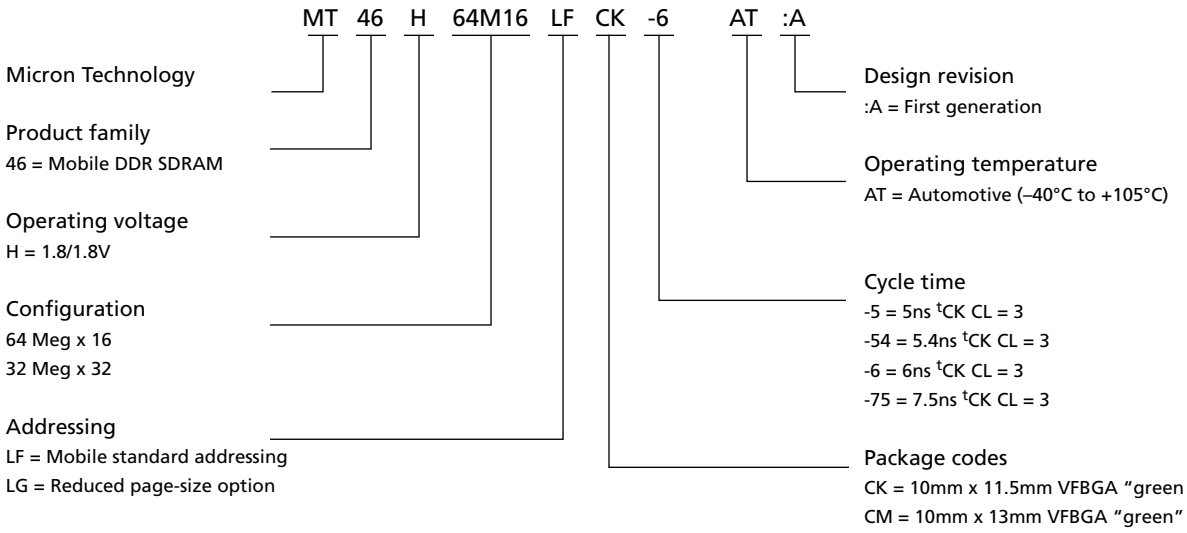
Figure 1: Mobile DDR Part Numbering



FBGA Part Marking

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA Part Marking Decoder is available at www.micron.com/decoder.

General Description

The information in this addendum is specific to the 1Gb: x16, x32 Mobile DDR SDRAM VFBGA-packaged part. For detailed specification information, refer to the 1Gb Mobile DDR SDRAM data sheet available on Micron's Web site: www.micron.com.

Note: Any values specified in this addendum replace the same values listed in the 1Gb Mobile DDR SDRAM data sheet.

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Electrical Specifications

Table 3: IDD Specifications and Conditions (x16/x32)
Refer to the standard product data sheet for applicable notes; VDD/VDDQ = 1.70–1.95V

Parameter/Condition		Symbol	Max				Unit	Notes
			-5	-54	-6	-75		
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD2P	1,200				µA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		IDD2PS	1,200				µA	7
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		IDD2NS	28	26	25	20	mA	9
Active power-down standby current: One bank active; CKE = LOW; CS = HIGH; ^{t}CK = ^{t}CK (MIN); Address and control inputs are switching; Data bus inputs are stable		IDD3P	4.6				mA	8
Active power-down standby current: Clock stopped; One bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		IDD3PS	4.6				mA	
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	^{t}RFC = ^{t}REFI	IDD5A	16	16	16	15	mA	10, 11

Table 4: Electrical Characteristics and Recommended AC Operating Conditions
Refer to the standard product data sheet for applicable notes; VDD/VDDQ = 1.70–1.95V; +85°C ≤ operating temperature ≤ +105°C

Parameter	Symbol	-5		-54		-6		-75		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Refresh period	^{t}REF	–	16	–	16	–	16	–	16	ms	
Average periodic refresh interval	^{t}REFI	–	1.95	–	1.95	–	1.95	–	1.95	µs	22

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992
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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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Revision History

Rev. B 05/08

- Restructured to include latest product data sheet changes/updates
- Updated to “Production” status

Rev. A 05/07

- Initial revision

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