Mobile SDRAM

MT48H32M16LF – 8 Meg x 16 x 4 banks
MT48H16M32LF/LG – 4 Meg x 32 x 4 banks

Features

- VDD/VDDQ = 1.7–1.95V
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, and continuous
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive strength (DS)

Options — Marking

- VDD/VDDQ
  - 1.8V/1.8V — H
- Row size option
  - Standard addressing option — LF
  - Reduced page-size option — LG[1]
- Configuration
  - 32 Meg x 16 (8 Meg x 16 x 4 banks) — 32M16
  - 16 Meg x 32 (4 Meg x 32 x 4 banks) — 16M32
- Plastic "green" packages
  - 54-ball VFBGA (8mm x 9mm) — BF[2]
  - 90-ball VFBGA (10mm x 13mm) — CM[3]
- Timing – cycle time
  - 6ns at CL = 3 — -6
  - 7.5ns at CL = 3 — -75
- Operating temperature range
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
- Design revision — :B

Table 1: Configuration Addressing

Architecture	32 Meg x 16	16 Meg x 32	16 Meg x 32 Reduced Page-Size Option[1]
Number of banks	4	4	4
Bank address balls	BA0, BA1	BA0, BA1	BA0, BA1
Row address balls	A[12:0]	A[12:0]	A[13:0]
Column address balls	A[9:0]	A[8:0]	A[7:0]

Table 2: Key Timing Parameters
CL = CAS (READ) latency

Speed Grade	Clock Rate (MHz)		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-6	104	166	8ns	5ns
-75	104	133	8ns	5.4ns

Notes: 1. For reduced page-size option (marking LG), contact factory for availability.
2. Only available for x16 configuration.
3. Only available for x32 configuration.

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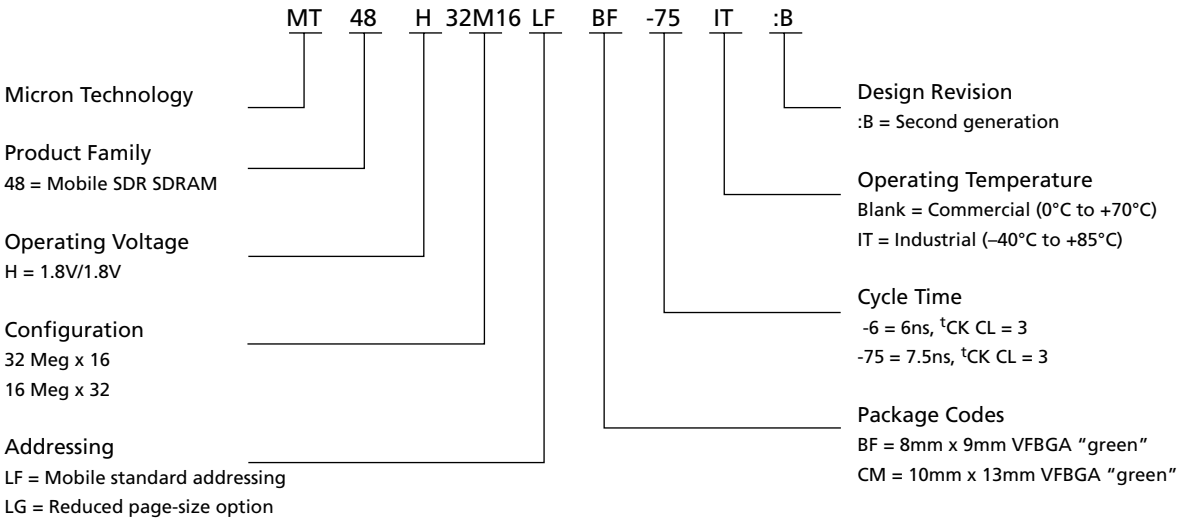
Figure 1: 512Mb Mobile SDRAM Part Numbering



General Description

The Micron® 512Mb Mobile SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1K columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits. In a reduced page-size option, each of the x32's 134,217,728-bit banks is organized as 16,384 rows by 256 columns x32 bits.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Functional Block Diagrams

Figure 2: 32 Meg x 16 SDRAM

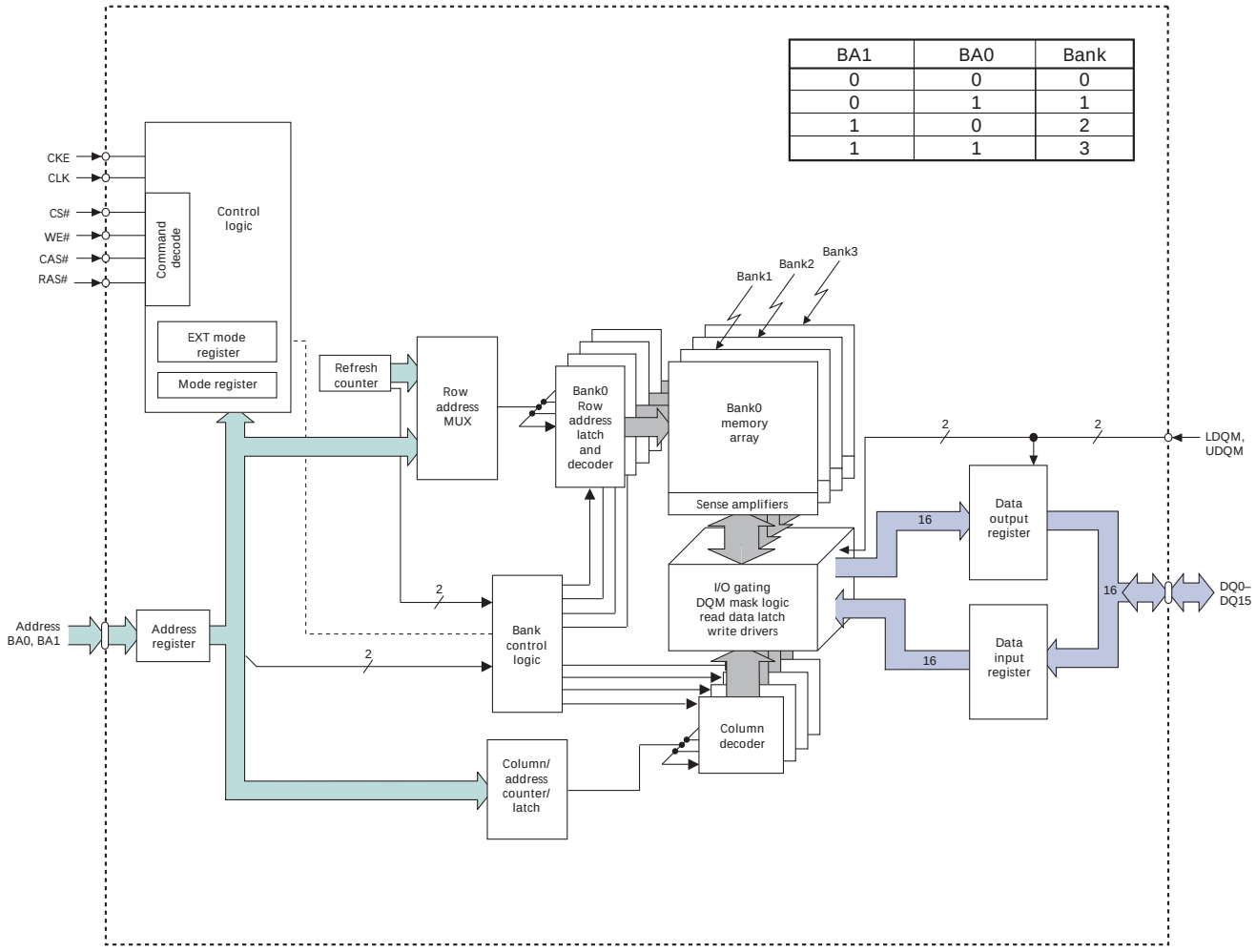
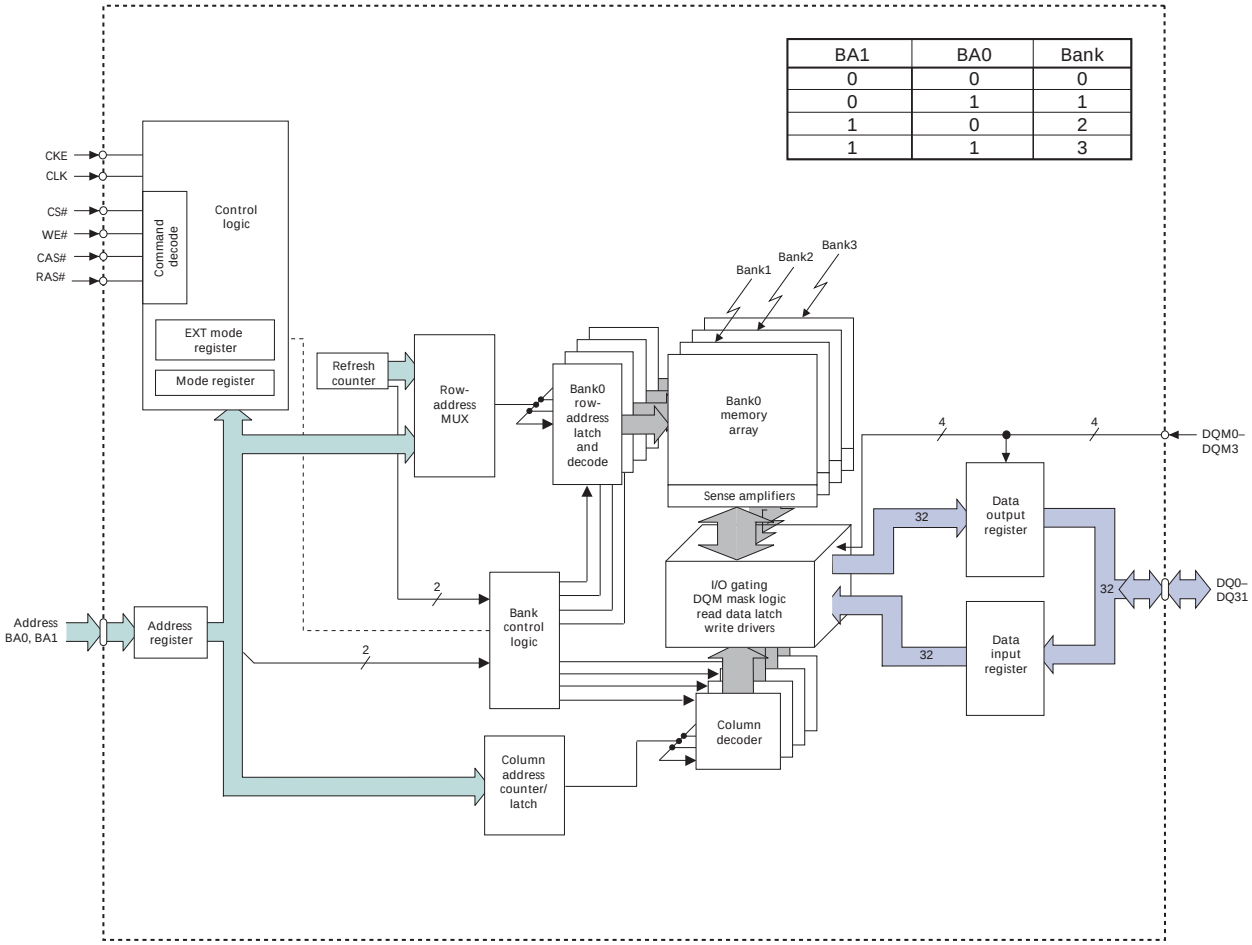
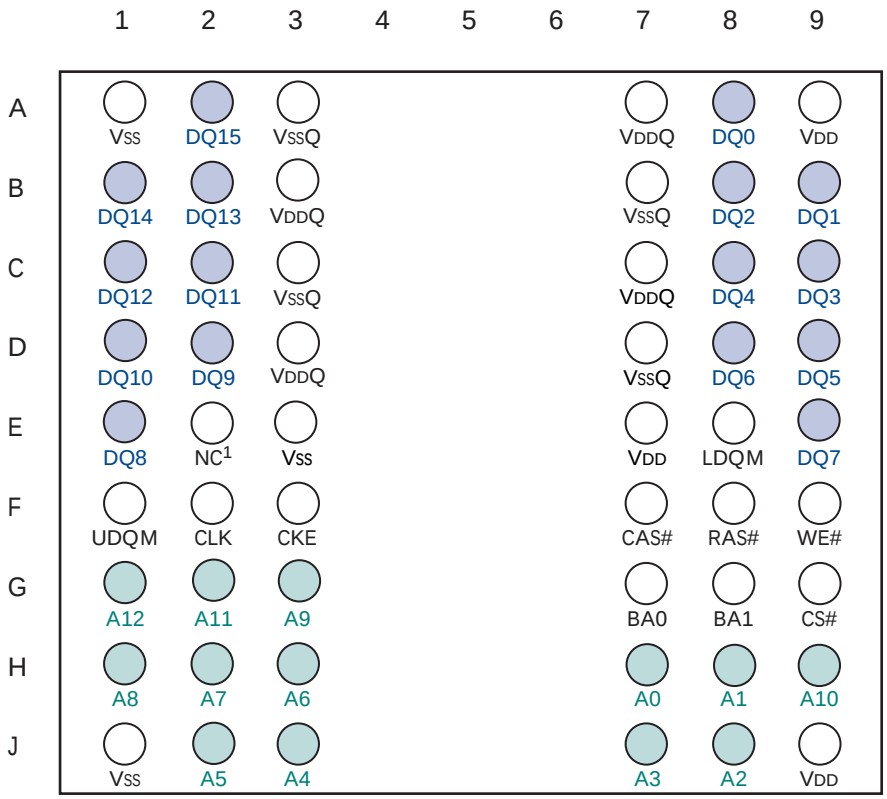


Figure 3: 16 Meg x 32 SDRAM



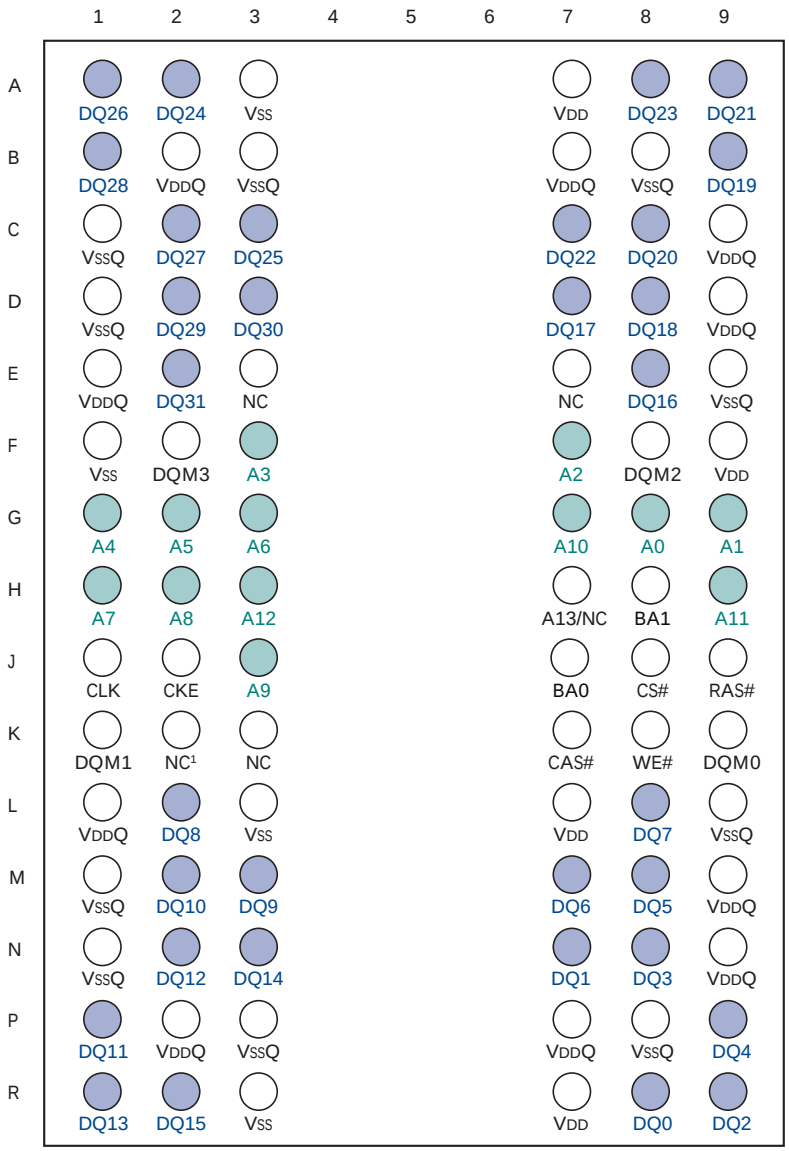
Ball Assignments

Figure 4: 54-Ball VFBGA (Top View)



Notes: 1. The E2 pin must be connected to VSS, VSSQ, or left floating.

Figure 5: 90-Ball VFBGA (Top View)



Notes: 1. The K2 pin must be connected to VSS, VSSQ, or left floating.

Ball Descriptions

Table 3: VFBGA Ball Descriptions

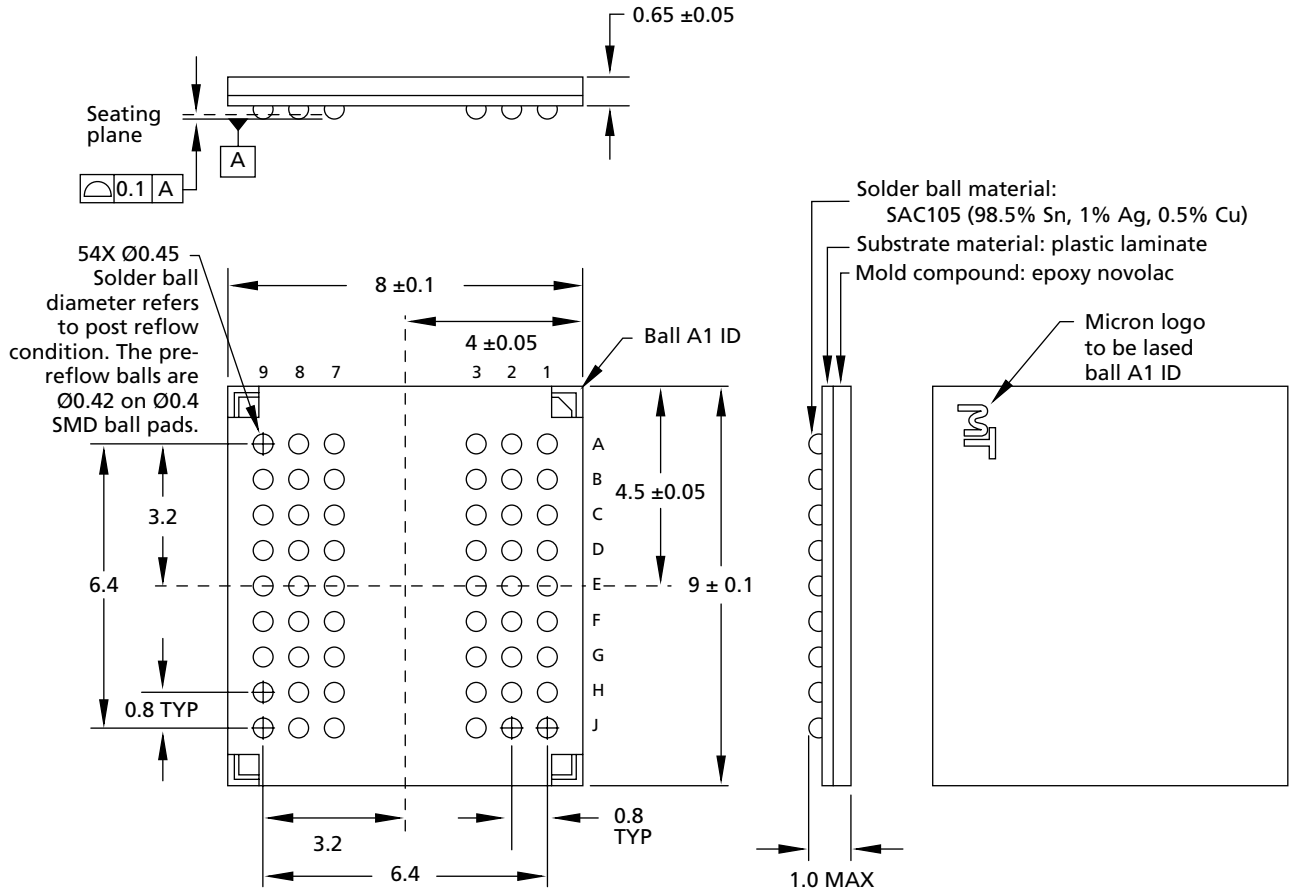
54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
F2	J1	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	J2	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
G9	J8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	K7, J9, K8	CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
E8, F1	K9, K1, F8, F2	DQM[3:0] LDQM, UDQM	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. For the x16, LDQM corresponds to DQ[7:0] and UDQM corresponds to DQ[16:8]. For the x32, DQM0 corresponds to DQ[7:0], DQM1 corresponds to DQ[15:8], DQM2 corresponds to DQ[23:16], and DQM3 corresponds to DQ[31:24]. DQM[3:0] (or LDQM and UDQM if x16) are considered same state when referenced as DQM.
G7, G8	J7, H8	BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 become when registering an ALL BANK PRECHARGE (A10 HIGH).
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2, G1	G8, G9, F7, F3, G1, G2, G3, H1, H2, J3, G7, H9, H3	A[12:0]	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row-address A[12:0]) and READ/WRITE command [column-address A[8:0] (x32); column-address A[9:0] (x16); with A10 defining auto precharge] to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command.
–	H7	A13/NC	Input	H7 is used for the LG, reduced page-size, option (see Table 1 on page 1); otherwise, leave as NC.

Table 3: VFBGA Ball Descriptions (continued)

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	R8, N7, R9, N8, P9, M8, M7, L8, L2, M3, M2, P1, N2, R1, N3, R2, E8, D7, D8, B9, C8, A9, C7, A8, A2, C3, A1, C2, B1, D2, D3, E2	DQ[31:0]	I/O	Data input/output: Data bus.
A7, B3, C7, D3	B2, B7, C9, D9, E1, L1, M9, N9, P2, P7	$V_{DD}Q$	Supply	DQ power: Provide isolated power to DQ for improved noise immunity.
A3, B7, C3, D7	B8, B3, C1, D1, E9, L9, M1, N1, P3, P8	$V_{SS}Q$	Supply	DQ ground: Provide isolated ground to DQ for improved noise immunity.
A9, E7, J9	A7, F9, L7, R7	V_{DD}	Supply	Core power supply.
A1, E3, J1	A3, F1, L3, R3	V_{SS}	Supply	Ground.
E2	K2	NC	–	Ball E2 on the 54 ball and K2 on the 90 ball must be connected to V_{SS}, $V_{SS}Q$, or left floating.
	E3, E7, K3	NC	–	Internally not connected. These balls can be left unconnected but it is recommended that they be connected to V_{SS}.

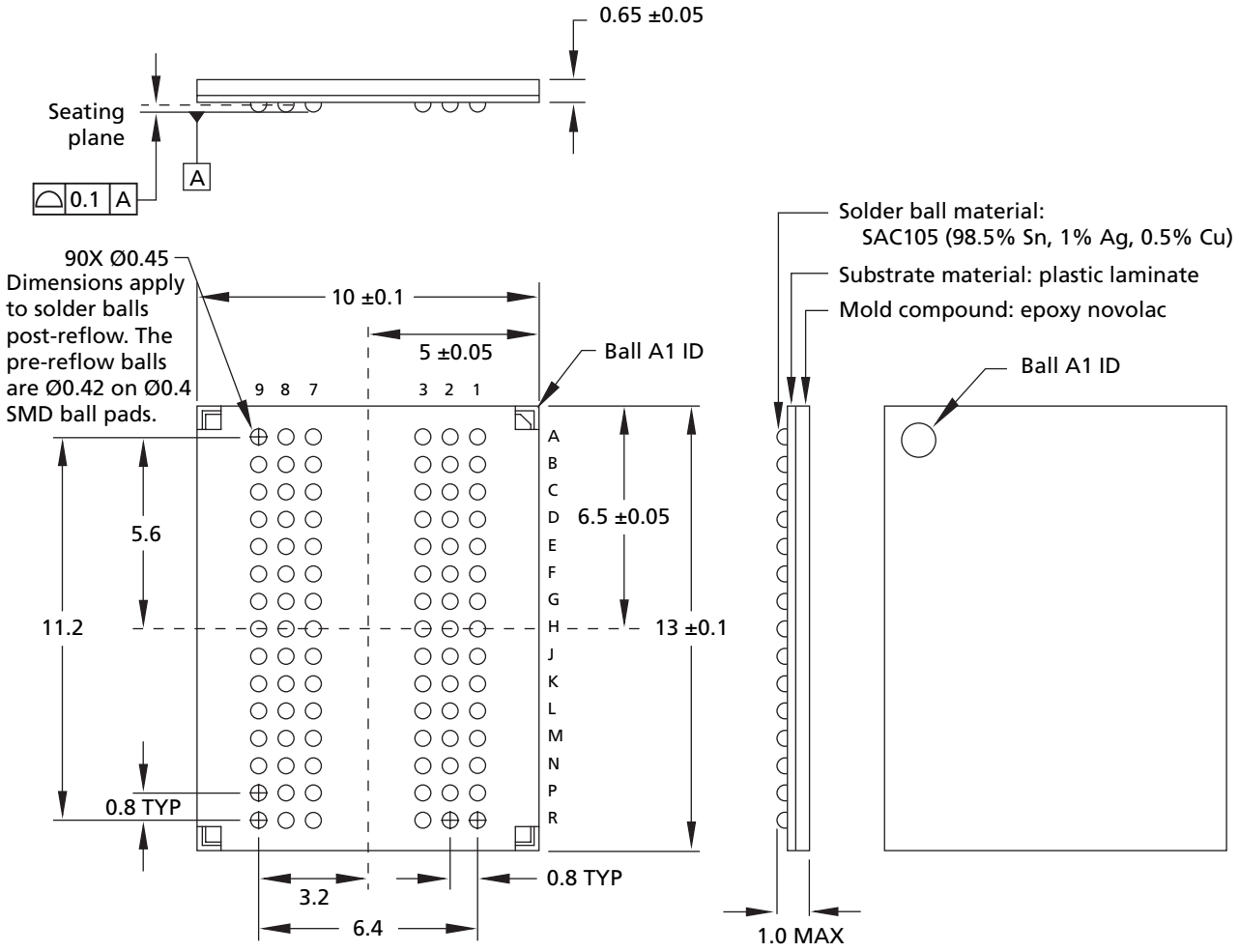
Package Dimensions

Figure 6: 54-Ball VFBGA (8mm x 9mm)



Notes: 1. All dimensions are in millimeters.

Figure 7: 90-Ball VFBGA (10mm x 13mm)



Notes: 1. All dimensions are in millimeters.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in Table 4 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Voltage/Temperature	Symbol	Min	Max	Units
Voltage on V_{DD}/$V_{DD}Q$ supply relative to V_{SS}[1]	V_{DD}/$V_{DD}Q$	–0.5	+2.4	V
Voltage on inputs, NC or I/O balls relative to V_{SS}	V_{IN}	–0.5	+2.4	
Storage temperature plastic	T_{STG}	–55	+150	°C

Notes: 1. V_{DD} and $V_{DD}Q$ must be within 300mV of each other at all times. $V_{DD}Q$ must not exceed V_{DD}.

Table 5: DC Electrical Characteristics and Operating Conditions
Notes: 1 and 2 apply to all parameters and conditions; V_{DD}/$V_{DD}Q$ = 1.7–1.95V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.95	V	
I/O supply voltage	V_{DDQ}	1.7	1.95	V	
Input high voltage: Logic 1; All inputs	V_{IH}	0.8 × $V_{DD}Q$	$V_{DD}Q$ + 0.3	V	3
Input low voltage: Logic 0; All inputs	V_{IL}	–0.3	+0.3	V	3
Output high voltage	V_{OH}	0.9 × $V_{DD}Q$	–	V	4
Output low voltage	V_{OL}	–	0.2	V	4
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other balls not under test = 0V)	I_I	–1.0	1.0	µA	
Output leakage current: DQs are disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	–1.5	1.5	µA	
Operating temperature: Commercial Industrial	 T_A T_A	 0 –40	 +70 +85	°C	

Notes:
1. All voltages referenced to V_{SS}.
2. A full initialization sequence is required before proper device operation is ensured
3. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = –2V for a pulse width ≤ 3ns.
4. I_{OUT} = 4mA for full drive strength. Other drive strengths require appropriate scale.

Table 6: Capacitance
Note 1 applies to all parameters and conditions.

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	C_{I1}	2.0	5.0	pF
Input capacitance: All other input-only balls	C_{I2}	2.0	5.0	pF
Input/output capacitance: DQs	C_{IO}	2.5	6.0	pF

Notes: 1. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +1.8V; T_A = 25°C; ball under test biased at 0.9V, f = 1 MHz.

Table 7: IDD Specifications and Conditions (x16)

Note 1 applies to all parameters and conditions; notes appear on page 16; VDD/VDDQ = 1.70–1.95V.

Parameter/Condition		Symbol	Max -6	Max -75	Units	Notes
Operating current: Active mode; Burst = 1; READ or WRITE; tRC = tRC (MIN)		IDD1	90	80	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		IDD2P	300	300	µA	5
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		IDD2N	10	10	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		IDD3P	5	5	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3N	20	18	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle		IDD4	100	90	mA	2, 3, 4
Auto refresh current CKE = HIGH; CS# = HIGH	tRFC = 110ns	IDD5	120	120	mA	2, 3, 4, 6
	tRFC = 7.8125µs	IDD6	3	3	mA	2, 3, 4, 7
Deep power-down		IZZ	10	10	µA	5, 8

Table 8: IDD Specifications and Conditions (x32)

Note 1 applies to all parameters and conditions; notes appear on page 16; VDD/VDDQ = 1.70–1.95V

Parameter/Condition		Symbol	Max -6	Max -75	Units	Notes
Operating current: Active mode; Burst = 1; READ or WRITE; tRC = tRC (MIN)		IDD1	90	80	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		IDD2P	300	300	µA	5
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		IDD2N	10	10	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		IDD3P	5	5	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3N	20	18	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle		IDD4	105	95	mA	2, 3, 4
Auto refresh current CKE = HIGH; CS# = HIGH	tRFC = 110ns	IDD5	120	120	mA	2, 3, 4, 6
	tRFC = 7.8125µs	IDD6	3	3	mA	2, 3, 4, 7
Deep power-down		IZZ	10	10	µA	5, 8

Table 9: IDD7 Specifications and Conditions (x16 and x32)

Notes: 1, 5, 9, and 10 apply to all conditions and parameters; VDD/VDDQ = 1.70–1.95V

Parameter/Condition		Symbol	IDD7	Units
Self refresh CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus inputs are stable.	Full array, 85°C	IDD7	700	µA
	Full array, 45°C	IDD7	390	µA
	Half array, 85°C	IDD7	520	µA
	Half array, 45°C	IDD7	310	µA
	1/4 array, 85°C	IDD7	430	µA
	1/4 array, 45°C	IDD7	275	µA
	1/8 array, 85°C	IDD7	430	µA
	1/8 array, 45°C	IDD7	275	µA
	1/16 array, 85°C	IDD7	375	µA
	1/16 array, 45°C	IDD7	250	µA

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. Measurement is taken 500ms after entering into this operating mode to allow tester measuring unit settling time.
6. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
7. CKE is HIGH during REFRESH command period tRFC else CKE is LOW.
8. Typical values at 25°C (not a maximum value).
9. Enables on-die refresh and address counters.
10. Values for IDD7 85°C full array and partial array are guaranteed for the entire temperature range. All other IDD7 values are estimated.

Figure 8: Typical IDD7 Curves

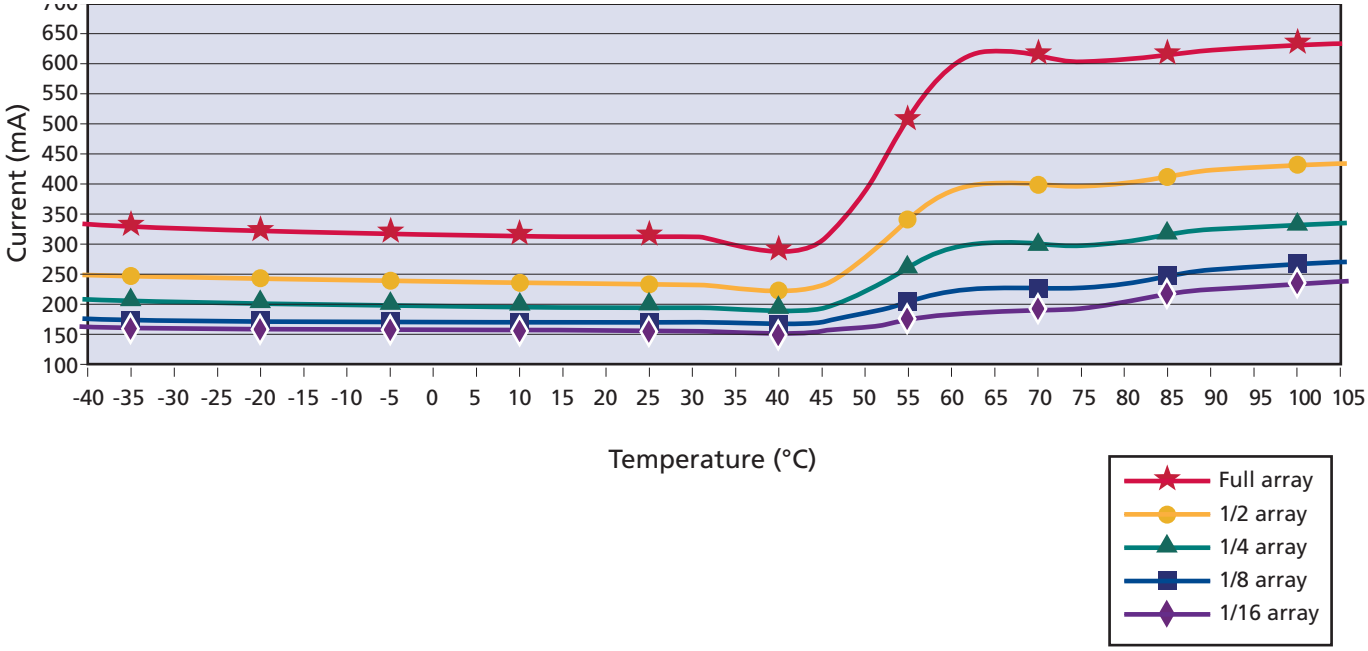


Table 10: Electrical Characteristics and Recommended AC Operating Conditions

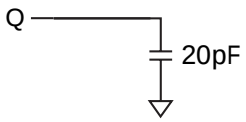
Notes 1–5 apply to all parameters; notes begin below Table 11 on page 19.

AC Characteristics			-6		-75			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from CLK (positive edge)	CL = 3	^{t}AC	–	5	–	5.4	ns	
	CL = 2		–	8	–	8		
Address hold time		^{t}AH	1	–	1	–	ns	
Address setup time		^{t}AS	1.5	–	1.5	–	ns	
CLK high-level width		^{t}CH	2.5	–	2.5	–	ns	
CLK low-level width		^{t}CL	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	^{t}CK	6	–	7.5	–	ns	6
	CL = 2		9.6	–	9.6	–		
CKE hold time		^{t}CKH	1	–	1	–	ns	
CKE setup time		^{t}CKS	1.5	–	1.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	1	–	1	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	1.5	–	1.5	–	ns	
Data-in hold time		^{t}DH	1	–	1	–	ns	
Data-in setup time		^{t}DS	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	^{t}HZ	–	5	–	5.4	ns	7
	CL = 2		–	8	–	8	ns	
Data-out Low-Z time		^{t}LZ	1	–	1	–	ns	
Data-out hold time (load)		^{t}OH	2.5	–	2.5	–	ns	
Data-out hold time (no load)		^{t}OHN	1.8	–	1.8	–	ns	
ACTIVE-to-PRECHARGE command		^{t}RAS	42	120,000	45	120,000	ns	
ACTIVE-to-ACTIVE command period		^{t}RC	60	–	67.5	–	ns	
ACTIVE-to-READ or WRITE delay		^{t}RCD	18	–	19.2	–	ns	
Refresh period (8,192 rows)		^{t}REF		64	–	64	ms	8
AUTO REFRESH period		^{t}RFC	97.5	–	97.5	–	ns	
PRECHARGE command period		^{t}RP	18	–	19.2	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	2	–	2	–	^{t}CK	
Transition time		^{t}T	0.3	1.2	0.3	1.2	ns	9
WRITE recovery time		^{t}WR	15	–	15	–	ns	10
Exit SELF REFRESH-to-ACTIVE command		^{t}XSR	120	–	120	–	ns	11

Table 11: AC Functional Characteristics
Notes 1–5 apply to all parameters

Parameter		Symbol	-75	-8	Units	Notes
Last data-in to burst STOP command		tBDL	1	1	tCK	12
READ/WRITE command to READ/WRITE command		tCCD	1	1	tCK	12
Last data-in to new READ/WRITE command		tCDL	1	1	tCK	13
CKE to clock disable or power-down entry mode		tCKED	1	1	tCK	13
Data-in to ACTIVE command		tDAL	5	5	tCK	14, 16
Data-in to PRECHARGE command		tDPL	2	2	tCK	15, 16
DQM to input data delay		tDQD	0	0	tCK	12
DQM to data mask during WRITEs		tDQM	0	0	tCK	12
DQM to data High-Z during READs		tDQZ	2	2	tCK	12
WRITE command to input data delay		tDWD	0	0	tCK	12
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	tCK	
CKE to clock enable or power-down exit mode		tPED	1	1	tCK	13
Last data-in to PRECHARGE command		tRDL	2	2	tCK	15, 16
Data-out High-Z from PRECHARGE command	CL = 3	tROH	3	3	tCK	12
	CL = 2		2	2	tCK	

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le +70°C$ standard temperature and $–40°C \le T_A \le +85°C$ industrial temperature) is ensured.
3. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
4. Outputs measured for 1.8V at 0.9V with equivalent load:



Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.

5. AC timing tests have VIL and Vih with timing referenced to VIH/2 = crossover point. If the input transition time is longer than tT (MAX), then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the VIH/2 crossover point.
6. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) during access or precharge states (READ, WRITE, including tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
7. tHZ defines the time at which the output achieves the open circuit condition, it is not a reference to VOH or VOL. The last valid data element will meet tOH before going High-Z.
8. The 512Mb Mobile SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 7.8125µs meets the refresh requirement and ensures that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), once every 64ms.
9. AC characteristics assume tT = 1ns.
10. Auto precharge mode only. The precharge timing budget (tRP) begins at *x* ns for -75 after the first clock delay and after the last WRITE is executed. May not exceed the limit set for precharge mode.
11. CLK must be toggled a minimum of two times during this period.

12. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
13. Timing is specified by ^{t}CKS. Clock(s) specified as a reference only at minimum cycle rate.
14. Timing is specified by ^{t}WR plus ^{t}RP. Clock(s) specified as a reference only at minimum cycle rate.
15. Timing is specified by ^{t}WR.
16. Based on ^{t}CK (MIN), CL = 3.

Table 12: Target Output Drive Characteristics (Full Strength)

Notes 1–2 apply to all values. Characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	–2.80	–18.53
0.20	5.60	26.80	–5.60	–26.80
0.30	8.40	32.80	–8.40	–32.80
0.40	11.20	37.05	–11.20	–37.05
0.50	14.00	40.00	–14.00	–40.00
0.60	16.80	42.50	–16.80	–42.50
0.70	19.60	44.57	–19.60	–44.57
0.80	22.40	46.50	–22.40	–46.50
0.85	23.80	47.48	–23.80	–47.48
0.90	23.80	48.50	–23.80	–48.50
0.95	23.80	49.40	–23.80	–49.40
1.00	23.80	50.05	–23.80	–50.05
1.10	23.80	51.35	–23.80	–51.35
1.20	23.80	52.65	–23.80	–52.65
1.30	23.80	53.95	–23.80	–53.95
1.40	23.80	55.25	–23.80	–55.25
1.50	23.80	56.55	–23.80	–56.55
1.60	23.80	57.85	–23.80	–57.85
1.70	23.80	59.15	–23.80	–59.15
1.80	–	60.45	–	–60.45
1.90	–	61.75	–	–61.75

Notes:
1. Table values based on nominal impedance of 25Ω (full-drive) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Table 13: Target Output Drive Characteristics (Three-Quarter Strength)

Notes 1–3 apply to all values. Characteristics are specified under best and worst process variations/conditions.

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	-1.96	-12.97
0.20	3.92	18.76	-3.92	-18.76
0.30	5.88	22.96	-5.88	-22.96
0.40	7.84	25.94	-7.84	-25.94
0.50	9.80	28.00	-9.80	-28.00
0.60	11.76	29.75	-11.76	-29.75
0.70	13.72	31.20	-13.72	-31.20
0.80	15.68	32.55	-15.68	-32.55
0.85	16.66	33.24	-16.66	-33.24
0.90	16.66	33.95	-16.66	-33.95
0.95	16.66	34.58	-16.66	-34.58
1.00	16.66	35.04	-16.66	-35.04
1.10	16.66	35.95	-16.66	-35.95
1.20	16.66	36.86	-16.66	-36.86
1.30	16.66	37.77	-16.66	-37.77
1.40	16.66	38.68	-16.66	-38.68
1.50	16.66	39.59	-16.66	-39.59
1.60	16.66	40.50	-16.66	-40.50
1.70	16.66	41.41	-16.66	-41.41
1.80	–	42.32	–	-42.32
1.90	–	43.23	–	-43.23

Notes:
1. Table values based on nominal impedance of 37Ω (three-quarter drive strength) at $V_{DD}Q/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Table 14: Target Output Drive Characteristics (One-Half Strength)

Notes 1–2 apply to all values. Characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.30	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.20	–6.36	–18.20
0.60	7.64	19.30	–7.64	–19.30
0.70	8.91	20.30	–8.91	–20.30
0.80	10.16	21.20	–10.16	–21.20
0.85	10.80	21.60	–10.80	–21.60
0.90	10.80	22.00	–10.80	–22.00
0.95	10.80	22.45	–10.80	–22.45
1.00	10.80	22.73	–10.80	–22.73
1.10	10.80	23.21	–10.80	–23.21
1.20	10.80	23.67	–10.80	–23.67
1.30	10.80	24.14	–10.80	–24.14
1.40	10.80	24.61	–10.80	–24.61
1.50	10.80	25.08	–10.80	–25.08
1.60	10.80	25.54	–10.80	–25.54
1.70	10.80	26.01	–10.80	–26.01
1.80	–	26.48	–	–26.48
1.90	–	26.95	–	–26.95

Notes:
1. Table values based on nominal impedance of 55Ω (half-drive) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.
3. The I-V curve for one-quarter drive strength is approximately 50 percent of one-half drive strength.

Functional Description

Mobile SDRAMs are quad-bank DRAMs that operate at 1.8V and include a synchronous interface. All signals are registered on the positive edge of the clock signal, CLK.

Read and write accesses to SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, that is followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Mobile SDRAMs provide for programmable read or write burst lengths. An auto-precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

Mobile SDRAMs use an internal pipelined architecture to achieve high-speed operation. This architecture enables changing the column address on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

Mobile SDRAMs are designed to operate in 1.8V memory systems. An auto refresh mode is provided, along with power-saving, power-down, and deep power-down modes. All inputs and outputs are LVTTL-compatible.

Mobile SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Commands

Table 15 provides a quick reference of available commands. A written description of each command follows the table. Three additional Truth Tables appear on pages 31–35; these tables provide current state/next state information.

Table 15: Truth Table – Commands and DQM Operation
Note 1 applies to all commands; notes appear below this table

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	2
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/Col	X	3
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/Col	Valid	3
BURST TERMINATE or deep power-down (Enter deep power-down mode)	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	6
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	7, 8
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	9
Write enable/output enable	X	X	X	X	L	X	Active	10
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	10

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.
2. A[0:*n*] provide row address (where A*n* is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:*i*] provide column address (where *i* = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (non-persistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.
5. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQs column reads a "Don't Care" state to illustrate that the BURST TERMINATE command can occur when there is no data present.
6. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are "Don't Care."
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
9. A[11:0] define the op-code written to the mode register.
10. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

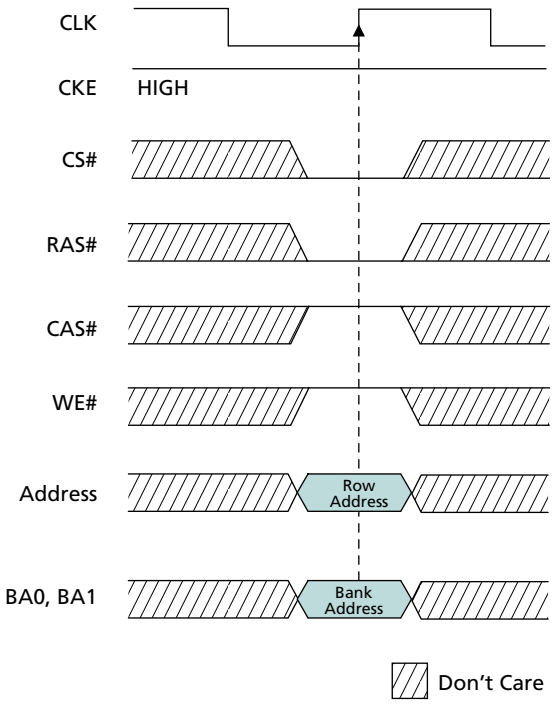
LOAD MODE REGISTER (LMR)

The mode register is loaded via inputs A[0:*n*] (where A*n* is the most significant address term), BA0, and BA1(See "Mode Register" on page 37). The LOAD MODE REGISTER command can only be issued when all banks are idle and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank. Figure 9 shows the ACTIVE command.

Figure 9: ACTIVE Command

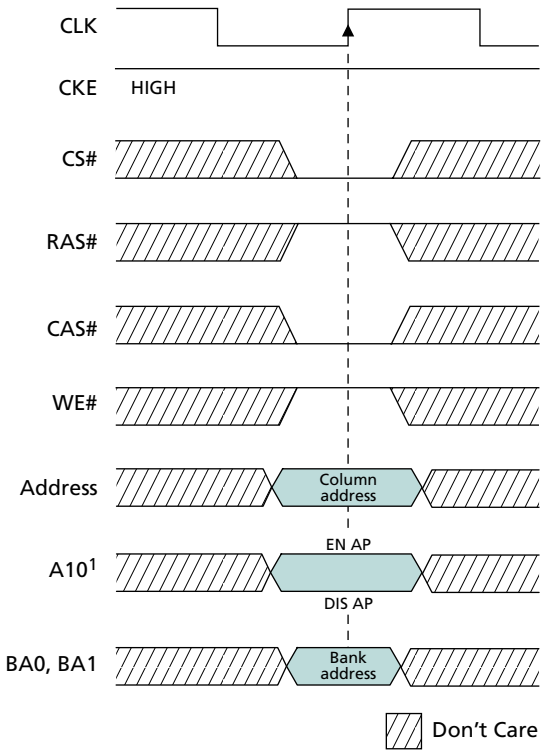


READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the read burst; if auto precharge is not selected, the row remains open for subsequent

accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data. Figure 10 shows the READ command.

Figure 10: READ Command

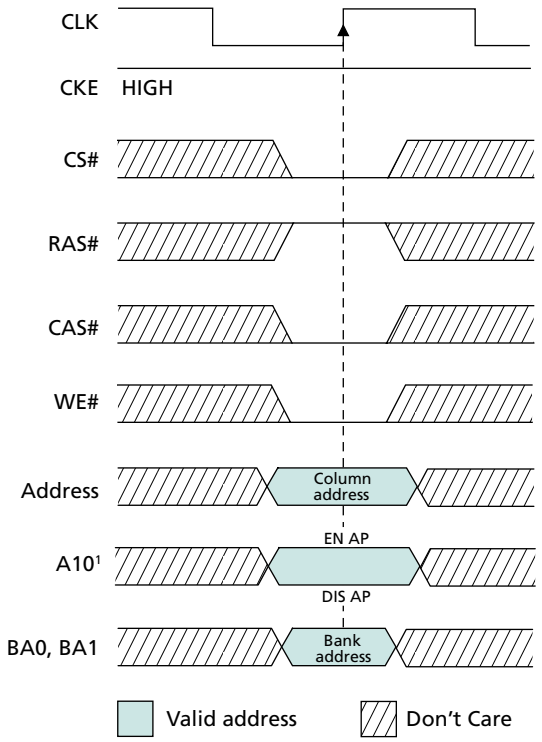


Notes: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the write burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data is written to memory; if the DQM signal is registered HIGH, the corresponding data inputs are ignored and a write is not executed to that byte/column location. Figure 11 shows the WRITE command.

Figure 11: WRITE Command

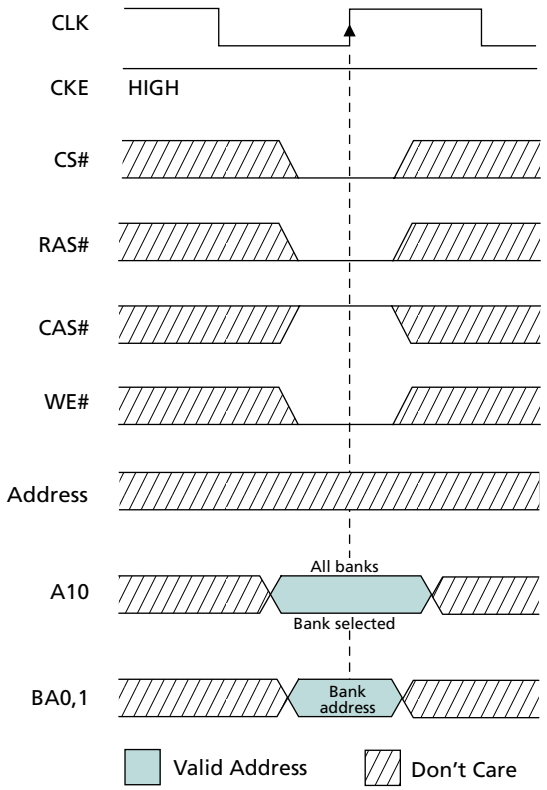


Notes: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. Figure 12 on page 29 shows the PRECHARGE command.

Figure 12: PRECHARGE Command



BURST TERMINATE

The BURST TERMINATE command is used to either truncate fixed-length or continuous page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command is truncated.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. Addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command.

SELF REFRESH

The SELF REFRESH command is used to place the device in self refresh mode. The self refresh mode is used to retain data in the SDRAM while the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

DEEP POWER-DOWN (DPD)

The DEEP POWER-DOWN command causes the Mobile SDRAM to enter deep power-down mode. DPD is an operating mode used to achieve maximum power reduction by eliminating the power of the whole memory array of the devices. This mode is entered by having all banks idle then holding CS# and WE# LOW with RAS# and CAS# held HIGH at the rising edge of the clock, while CKE is LOW. This mode is exited by asserting CKE HIGH.

Operations

Truth Tables

Table 16: Truth Table – Current State Bank *n*, Command to Bank *n*
Notes 1–6; notes appear below this table

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	11
Row active	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9, 10
Write (auto precharge disabled)	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9, 10

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 18 on page 35) and after ^tXSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown can be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or supported commands to the other bank should be issued on any clock edge occurring during these states. Supported commands to the other bank are determined by its current state and Table 16, and according to Table 17 on page 33.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. After ^tRP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. After ^tRCD is met, the bank will be in the row active state.

Read w/auto-precharge enabled:	Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.
Write w/auto-precharge enabled:	Starts with registration of a WRITE command with auto precharge enabled and ends when^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. After ^{t}RFC is met, the SDRAM will be in the all banks idle state.
Accessing mode register:	Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. After ^{t}MRD is met, the Mobile SDRAM will be in the all banks idle state.
Precharging all:	Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

Table 17: Truth Table – Current State Bank *n*, Command to Bank *m*
Notes 1–6; notes appear below this table

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	X	X	X	X	Any command otherwise supported for bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 12
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (Table 18 on page 35) and after ^tXSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown can be issued to bank *m* (assuming that bank *m* is in such a state that the given command is supported). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.

   Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.
4. AUTO REFRESH, SELF REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.

5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m* burst.
9. Burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later.
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank will interrupt the WRITE on bank *n* when registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

Table 18: Truth Table – CKE
Notes 1–4; notes appear below this table

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$	Notes
L	L	Power-down	X	Maintain power-down	
		Self refresh	X	Maintain self refresh	
		Clock suspend	X	Maintain clock suspend	
		Deep power-down	X	Maintain deep power-down	
L	H	Power-down	COMMAND INHIBIT or NOP	Exit power-down	5
		Deep power-down	X	Exit deep power-down	
		Self refresh	COMMAND INHIBIT or NOP	Exit self refresh	6
		Clock suspend	X	Exit clock suspend	7
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-down entry	
		All banks idle	BURST TERMINATE	Deep power-down entry	8
		All banks idle	AUTO REFRESH	Self refresh entry	
		Reading or writing	VALID	Clock suspend entry	
H	H		Table 17 on page 33		

Notes:
1. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that ^tCKS is met).
6. Exiting self refresh at clock edge *n* will put the device in the all banks idle state after ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^tXSR period. A minimum of two NOP commands must be provided during the ^tXSR period.
7. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.
8. Deep power-down is a power savings feature of this Mobile SDRAM device. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.

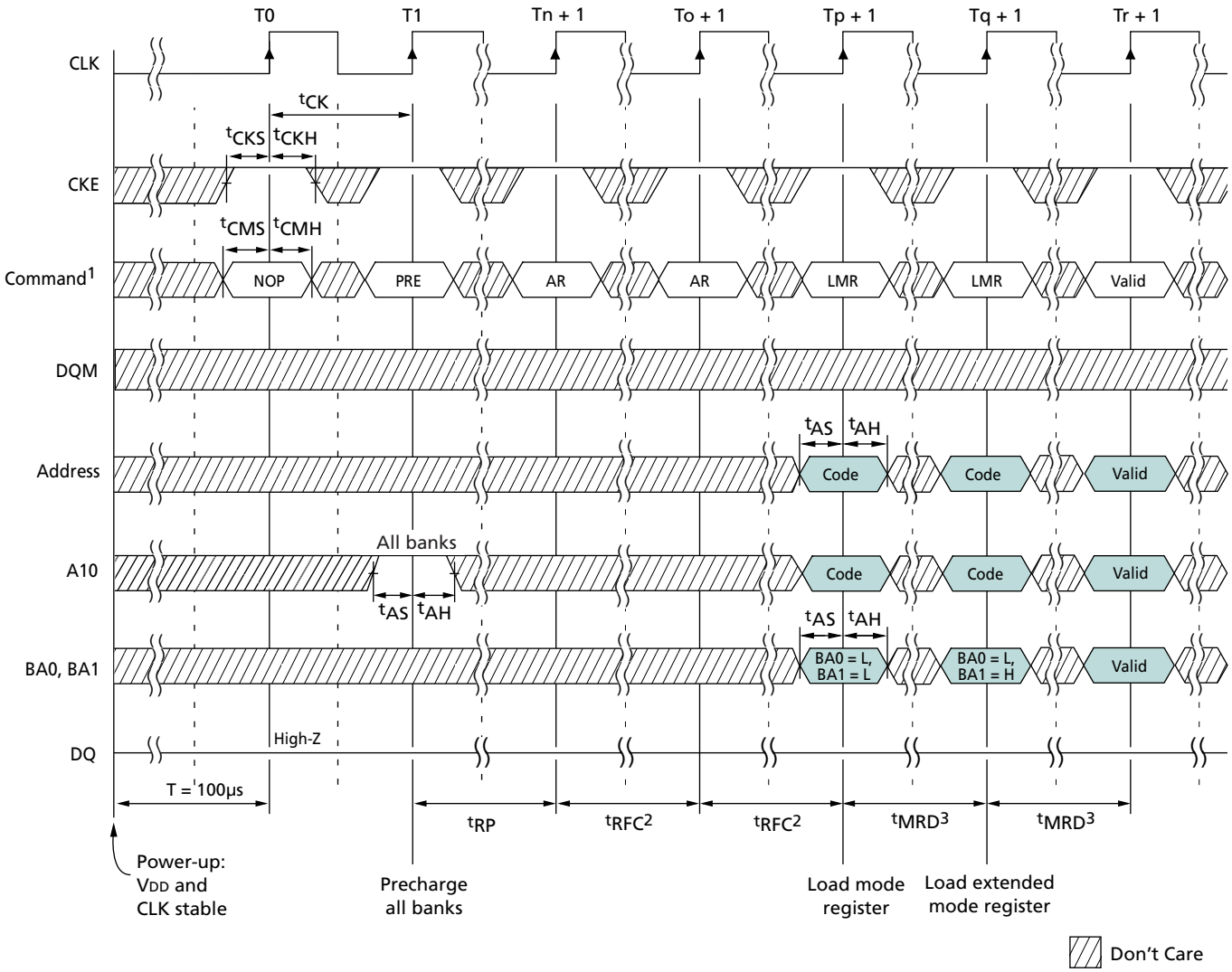
Initialization

Low-power SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. After the power is applied to V_{DD} and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

After the 100µs delay is satisfied by applying at least one COMMAND INHIBIT or NOP command, a PRECHARGE command must be applied. All banks must then be precharged, which places the device in the all banks idle state.

When in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode registers power up in an unknown state, they should be loaded prior to applying any operational command. The low-power SDRAM initialization sequence is shown in Figure 13.

Figure 13: Initialize and Load Mode Register



Notes:
1. PRE = PRECHARGE command, AR = AUTO REFRESH command, LMR = LOAD MODE REGISTER command.
2. NOPs or DESELECTs must only be provided during ^{t}RFC time.
3. NOPs or DESELECTs must only be provided during ^{t}MRD time.

Register Definition

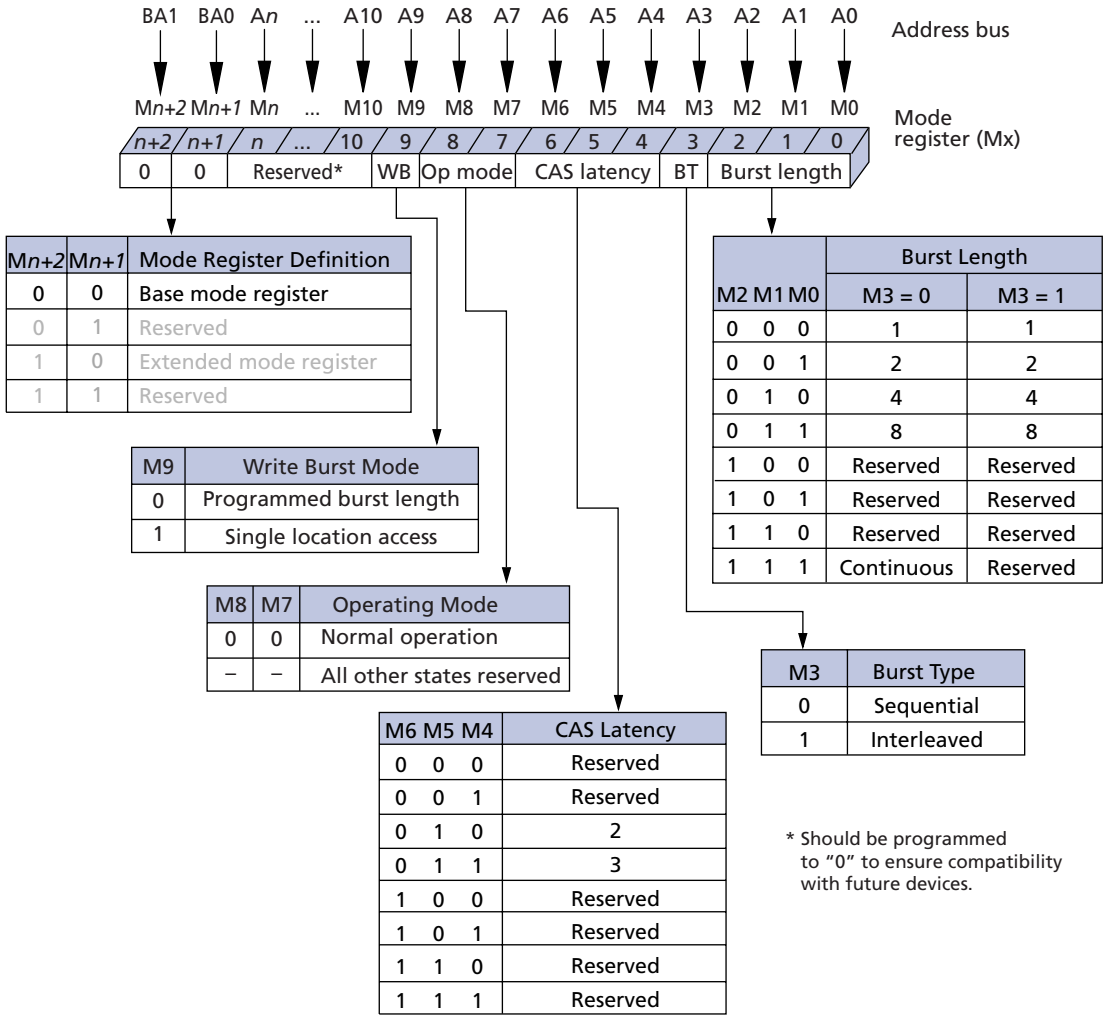
Mode Register

There are two mode registers in the Mobile SDRAM component, the mode register and the extended mode register (EMR). The mode register is illustrated in Figure 14 on page 37. The mode register defines the specific mode of operation of the Mobile SDRAM, including burst length (BL), burst type, CAS latency (CL), operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and retains the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the BL, M3 specifies the type of burst, M4–M6 specify the CL, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 through M*n* should be set to zero to ensure compatibility with future revisions. M*n* + 1and M*n* + 2 should be set to zero to prevent the extended mode register from being programmed.

The mode registers must be loaded when all banks are idle, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure 14: Mode Register Definition



Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with the BL being programmable, as shown in Figure 14 on page 37. The BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst length of 1, 2, 4, 8, or continuous locations are available for both the sequential and the interleaved burst types, and a continuous page burst is available for the sequential type. The continuous page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary BLs.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1–A8 when BL = 2, A2–A8 when BL = 4, and A3–A8 when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Continuous page burst wraps within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the BL, the burst type, and the starting column address, as shown in Table 19.

Table 19: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Continuous	n = A0–An/9/8 (location 0–y)			Cn, Cn + 1, Cn + 2, Cn + 3...Cn - 1, Cn...	Not supported

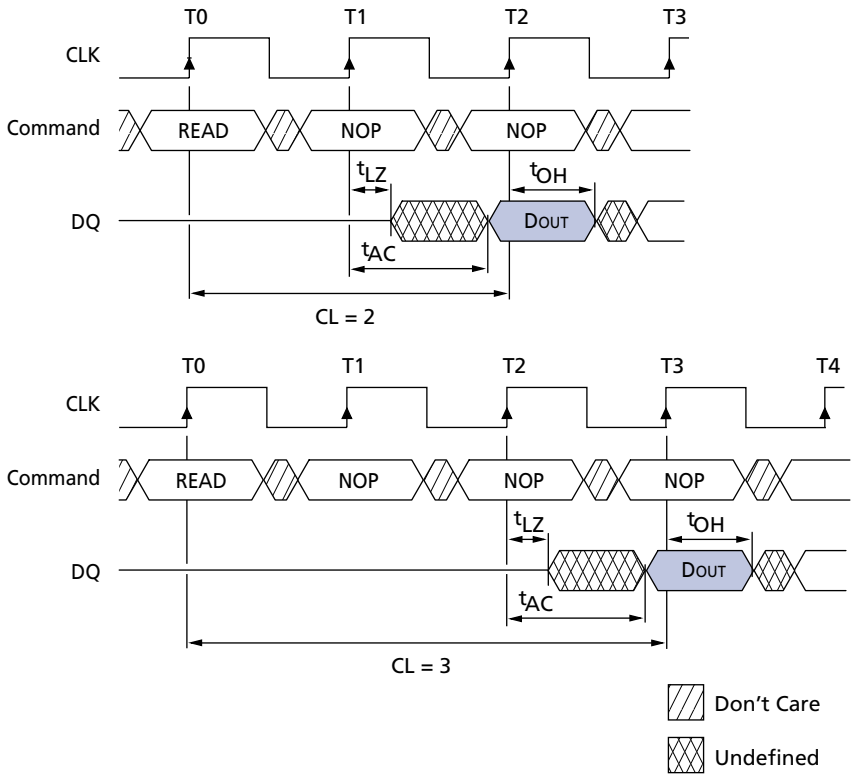
CAS Latency (CL)

The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data is valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs start driving after T1 and the data is valid by T2, as shown in Figure 15.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 15: CAS Latency



Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use. Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

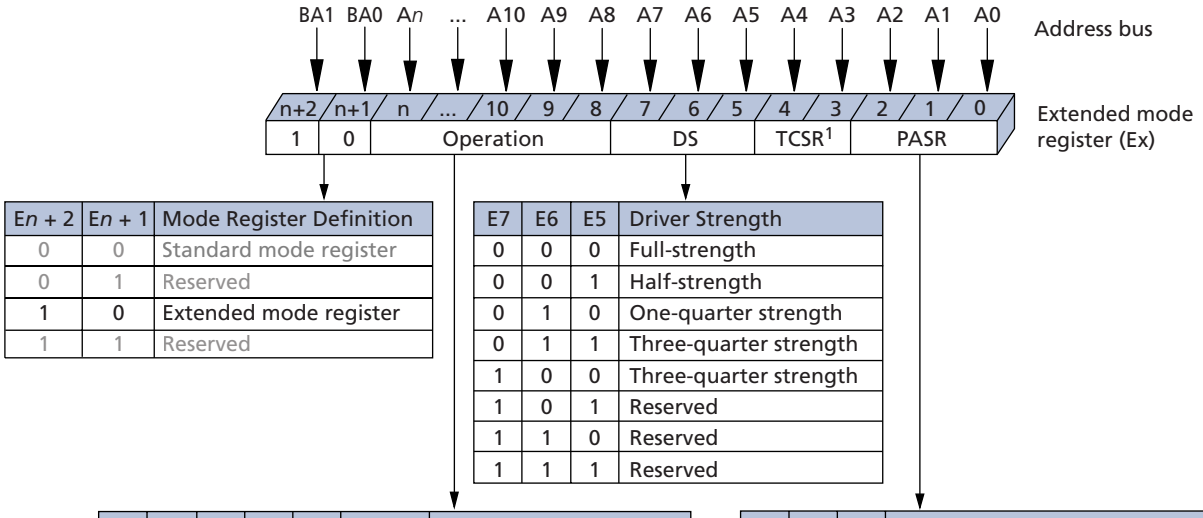
When M9 = 0, the BL programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Extended Mode Register (EMR)

The EMR controls the functions beyond those controlled by the mode register. These additional functions are special features of the mobile device that helps reduce overall system power consumption. They include temperature-compensated self refresh (TCSR) control, partial-array self refresh (PASR), and output drive strength.

The EMR is programmed via the MODE REGISTER SET command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

Figure 16: Extended Mode Register



En + 2	En + 1	Mode Register Definition
0	0	Standard mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

E7	E6	E5	Driver Strength
0	0	0	Full-strength
0	0	1	Half-strength
0	1	0	One-quarter strength
0	1	1	Three-quarter strength
1	0	0	Three-quarter strength
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

En	...	E10	E9	E8	E7–E0	
0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	Half array
0	1	0	Quarter array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array
1	1	0	One-sixteenth array
1	1	1	Reserved

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

The EMR must be programmed with E7–E*n* set to "0." It must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. After the values are entered, the EMR settings are retained even after exiting deep power-down mode.

Temperature-Compensated Self Refresh (TCSR)

Micron Mobile SDRAM includes a temperature sensor that is implemented for automatic control of the self refresh oscillator on the device. Therefore, it is recommended that the TCSR control bits in the EMR not be programmed or used. Programming the TCSR bits has no effect on the device. The self refresh oscillator will continue refresh at the optimal factory programmed rate for the device temperature.

Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the PASR feature enables the controller to select the amount of memory that is refreshed during self refresh. The following refresh options are available:

1. All banks (banks 0, 1, 2, and 3)
2. Two banks (banks 0 and 1; BA1= 0)
3. One bank (bank 0; BA1 = BA0 = 0)
4. Half bank (bank 0; BA1 = BA0 = row address MSB = 0)
5. Quarter bank (bank 0; BA1 = BA0 = row address MSB - 1 = 0)

WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks or segments of a bank in PASR are refreshed during self refresh. It is important to note that data in unused banks or portions of banks is lost when PASR is used.

Output Drive Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four supported settings for the output drivers: 25Ω, 37Ω, 55Ω, and 80Ω internal impedance. These are full, three-quarter, one-half, and one-quarter drive strengths, respectively.

Bank/Row Activation

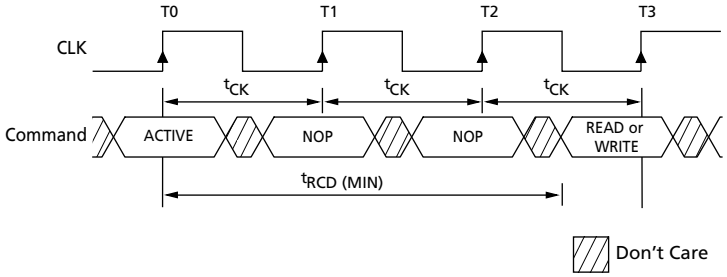
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, that selects both the bank and the row to be activated (see Figure 17 on page 42).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 17 on page 42, which covers any case where $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 17: Example: Meeting ^{t}RCD (MIN) When 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3



READs

READ bursts are initiated with a READ command, as shown in Figure 10. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

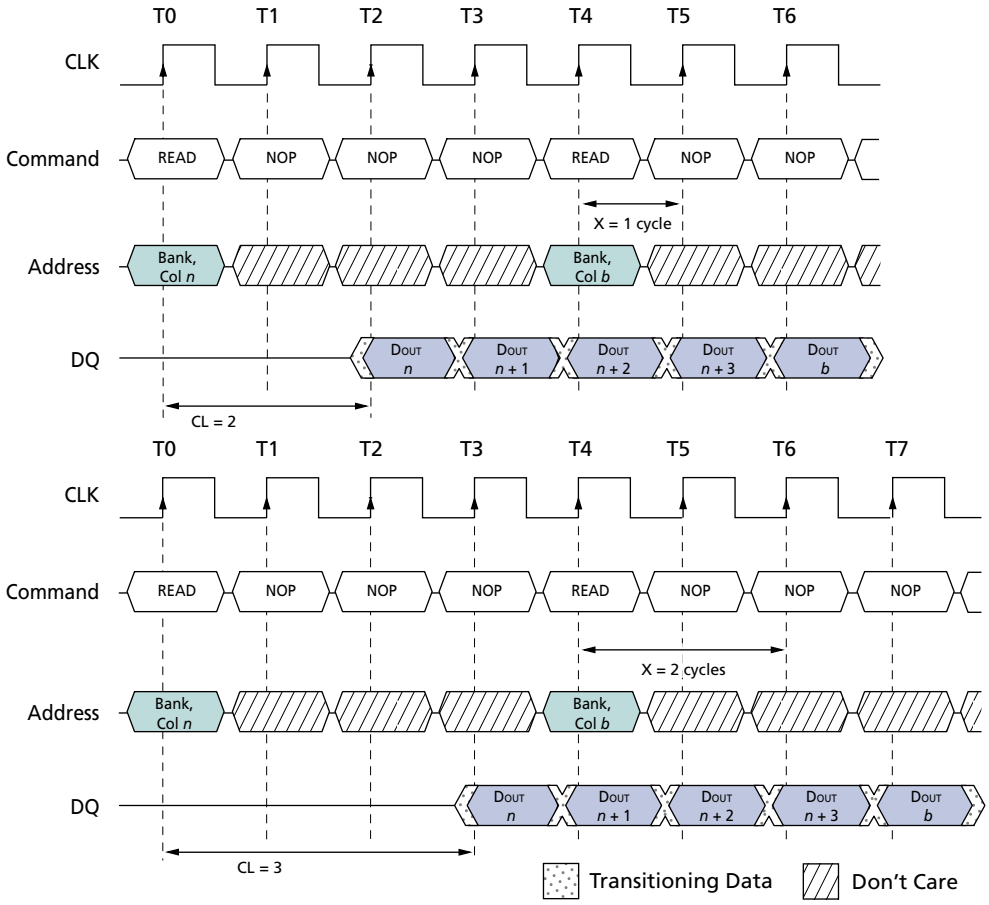
During READ bursts, the valid data-out element from the starting column address is available following the CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 18 on page 43 shows general timing for each possible CL setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A continuous page burst continues until terminated. At the end of the page, it wraps to column 0 and continues.

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 19 on page 44 for CAS latencies of two and three.

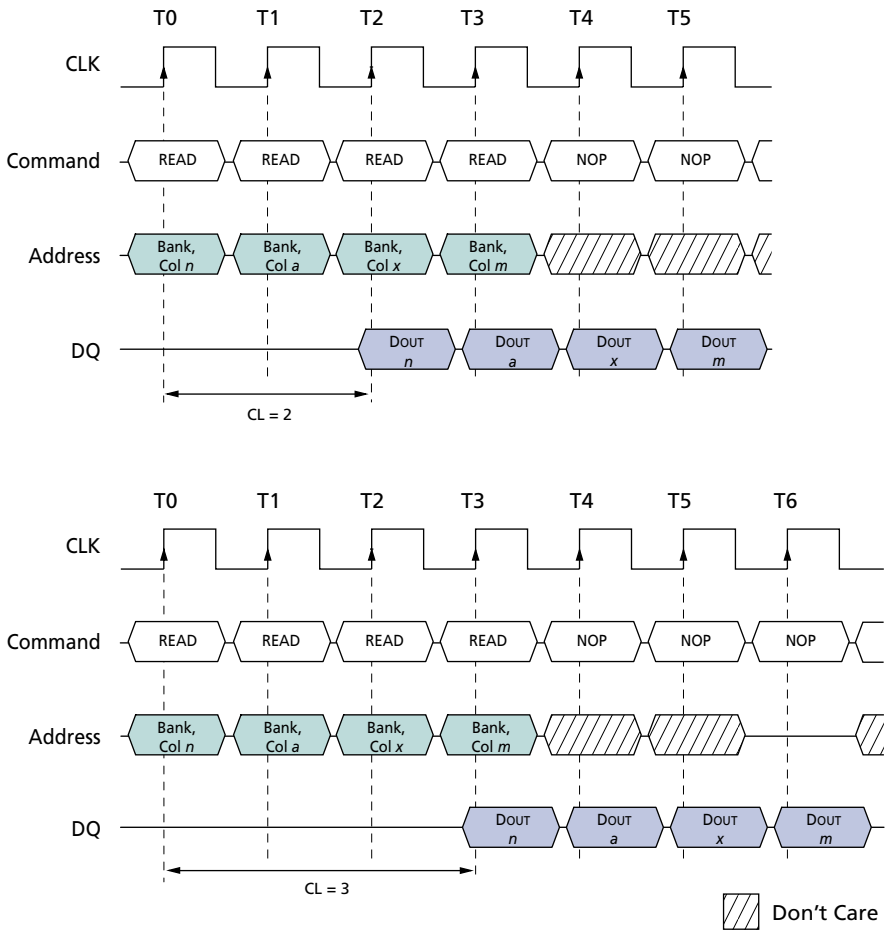
Mobile SDRAMs use a pipelined architecture and therefore do not require the 2*n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 18 on page 43, or each subsequent READ may be performed to a different bank.

Figure 18: Consecutive READ Bursts



Notes: 1. Each READ command may be to any bank. DQM is LOW.

Figure 19: Random READ Accesses



Notes: 1. Each READ command may be to any bank. DQM is LOW.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there is a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

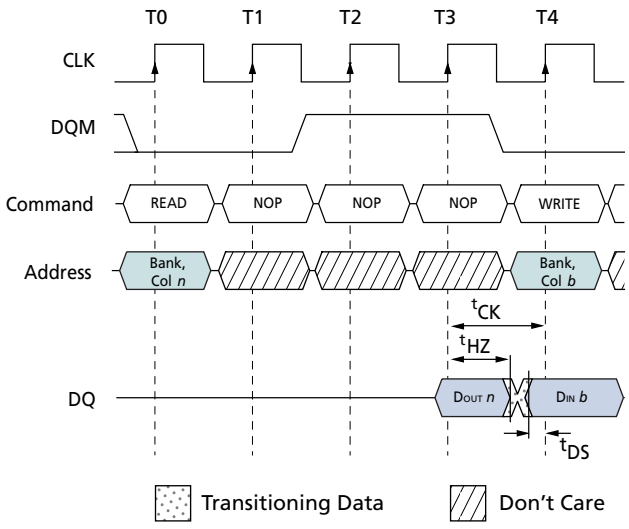
The DQM input is used to avoid I/O contention, as shown in Figure 20 on page 45 and Figure 21 on page 46. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. After the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 19 on page 44 shows the case where the clock frequency provides for bus contention to be avoided without adding a NOP cycle, and Figure 21 on page 46 shows the case where the additional NOP is needed.

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 22 on page 46 for each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

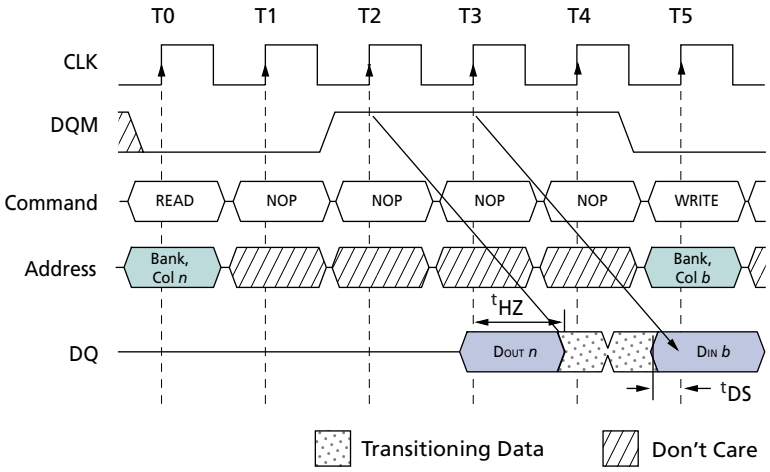
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. However, the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or continuous page bursts.

Figure 20: READ-to-WRITE



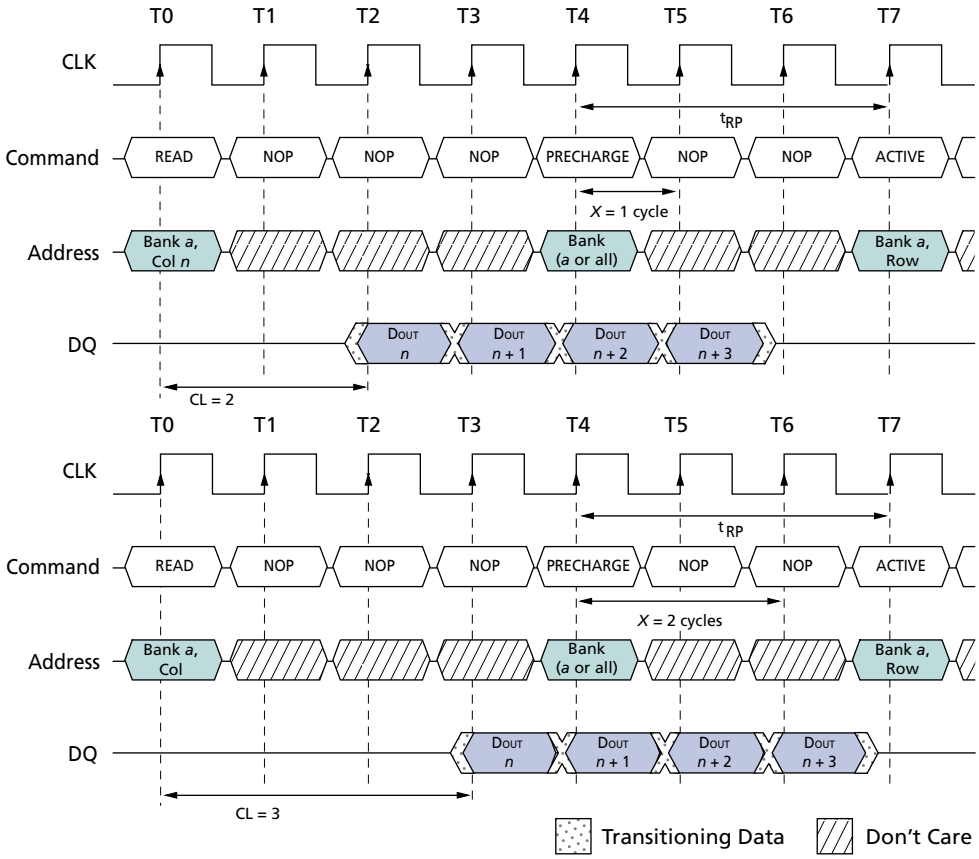
Notes: 1. CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank. If a burst of one is used, then DQM is not required.

Figure 21: READ-to-WRITE with Extra Clock Cycle



Notes: 1. CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank.

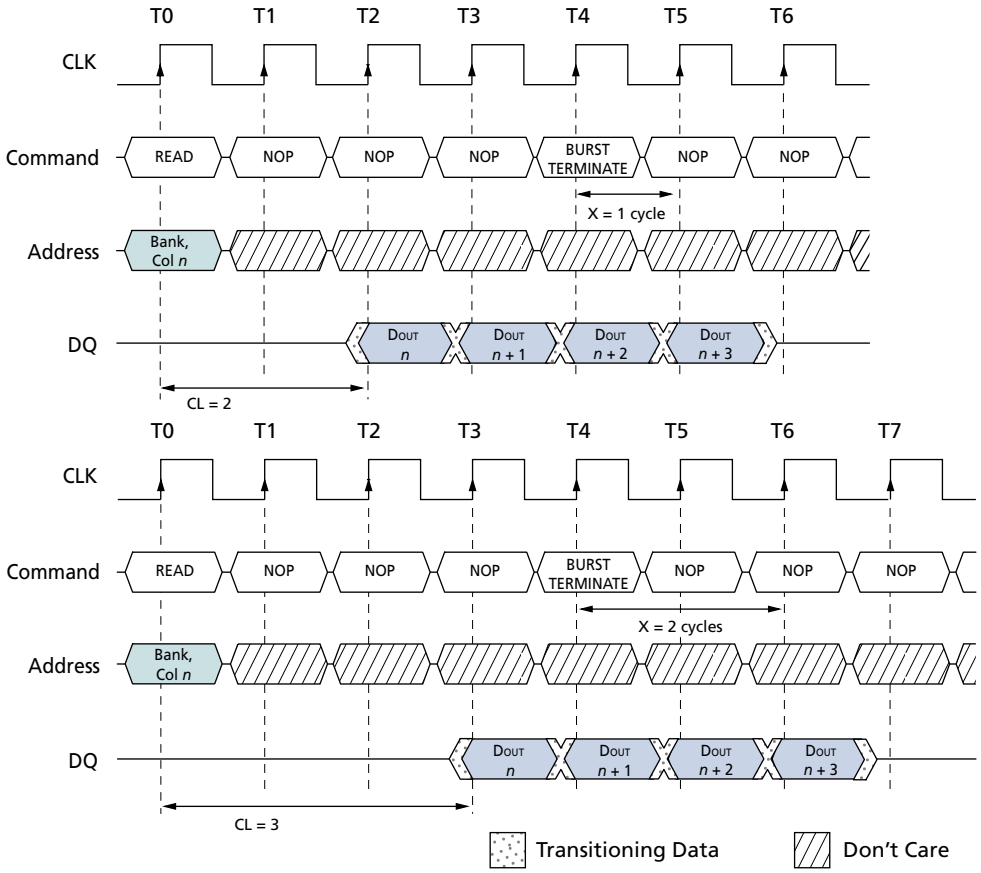
Figure 22: READ-to-PRECHARGE



Notes: 1. DQM is LOW.

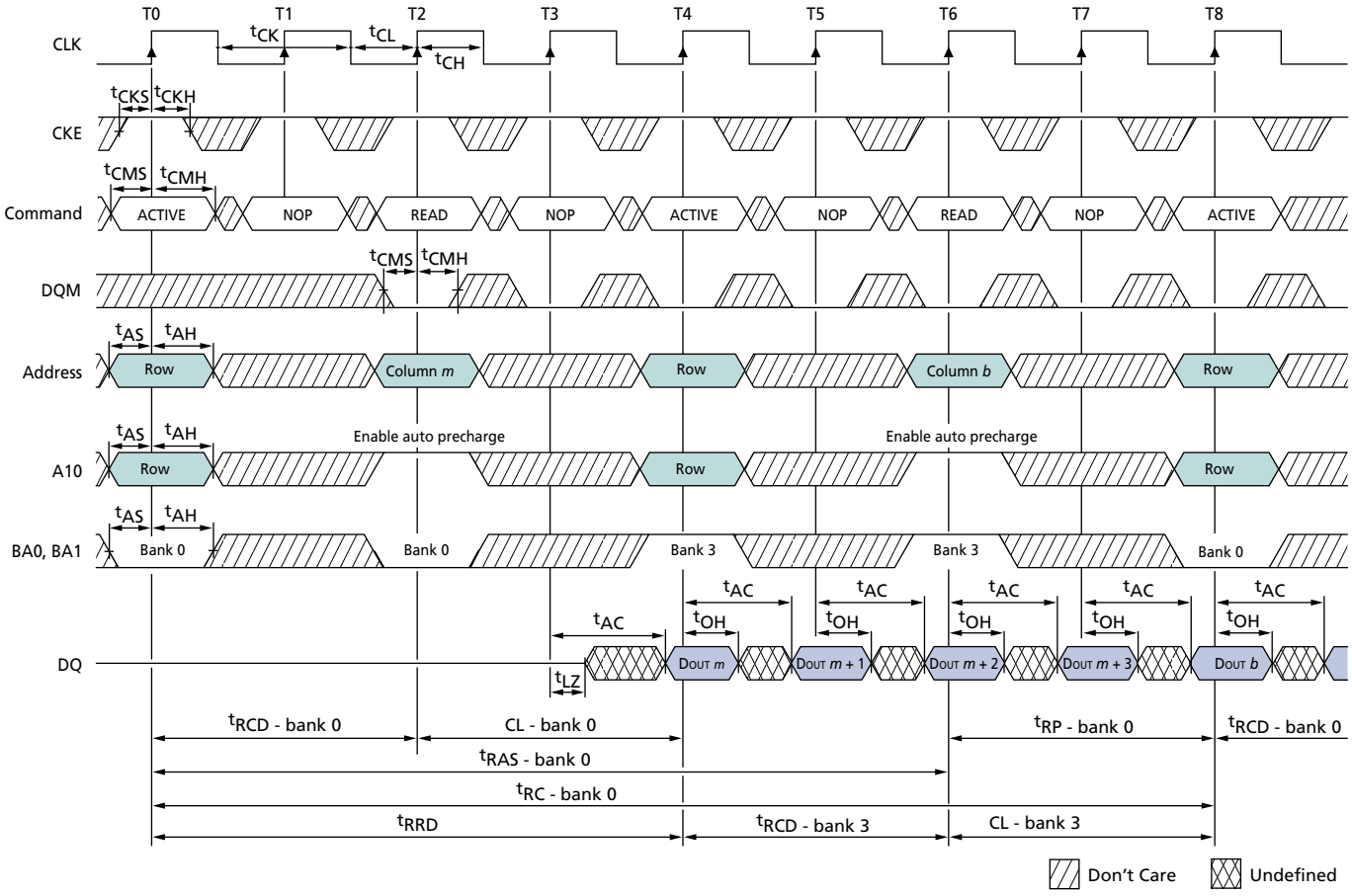
Continuous-page READ bursts may be truncated with a BURST TERMINATE command and fixed -length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 23 for each possible CL; data element *n* + 3 is the last desired data element of a longer burst.

Figure 23: Terminating a READ Burst



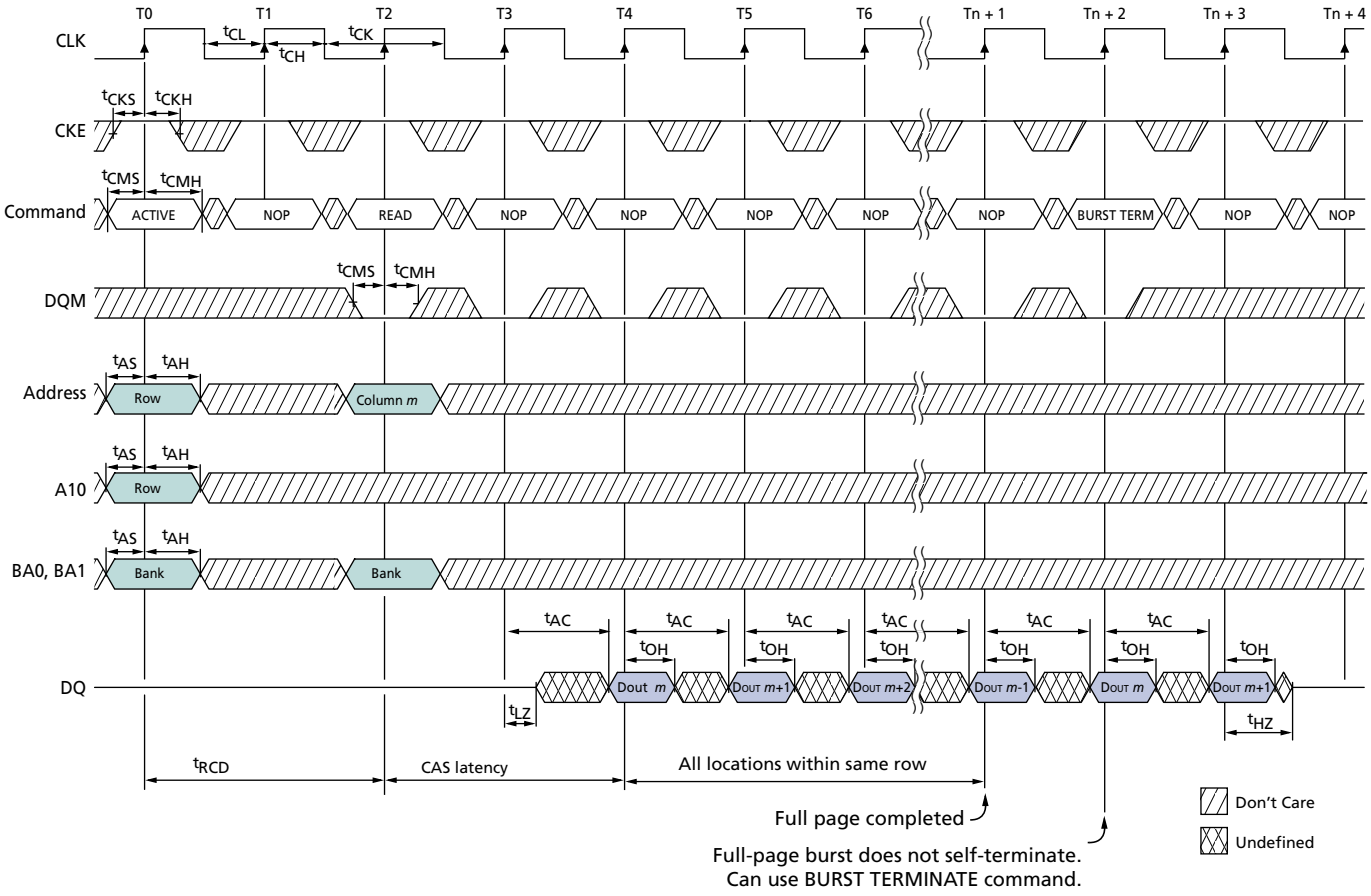
Notes: 1. DQM is LOW.

Figure 24: Alternating Bank Read Accesses



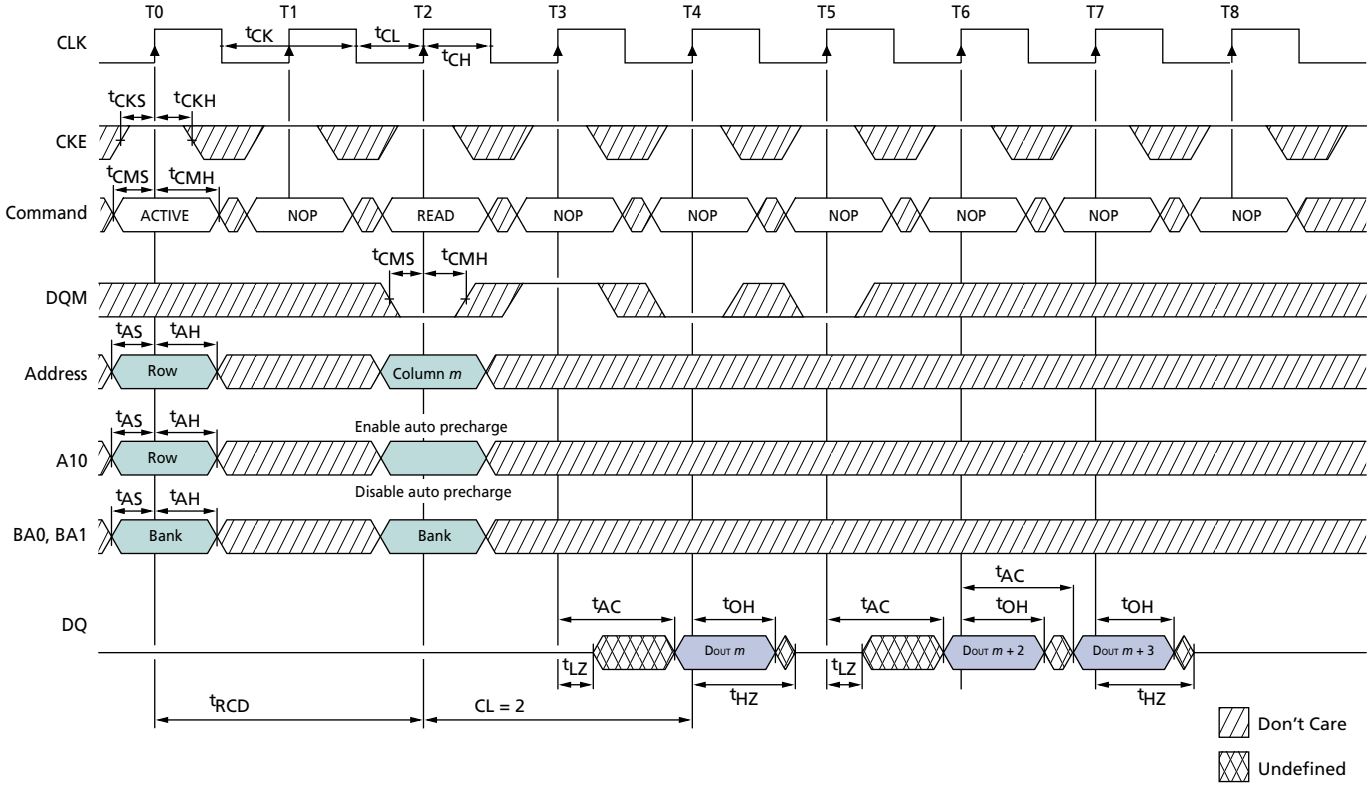
Notes: 1. For this example, BL = 4 and CL = 2.

Figure 25: READ Continuous Page Burst



Notes: 1. For this example, CL = 2.

Figure 26: READ – DQM Operation



Notes: 1. For this example, BL = 4 and CL = 2.

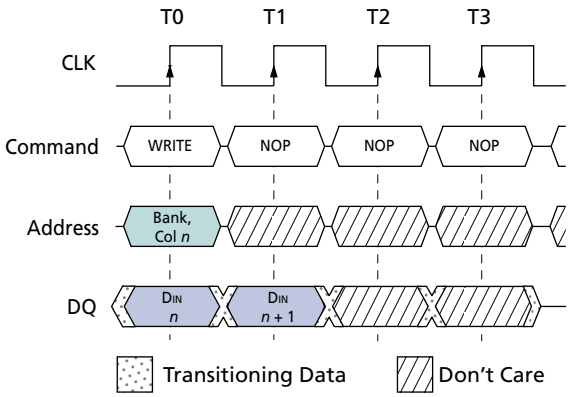
WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 11 on page 28. The starting column and bank addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered coincident with the WRITE command. Subsequent data elements are registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 27 on page 51). A continuous page burst continues until terminated; at the end of the page, it wraps to column 0 and continues.

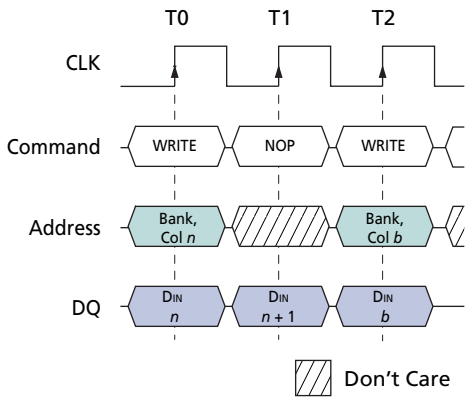
Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 28 on page 52. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Mobile SDRAMs use a pipelined architecture and therefore do not require the 2*n* rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 29 on page 53, or each subsequent WRITE may be performed to a different bank.

Figure 27: WRITE Burst



Notes: 1. BL = 2. DQM is LOW.

Figure 28: WRITE-to-WRITE



Notes: 1. DQM is LOW. Each WRITE command may be to any bank.

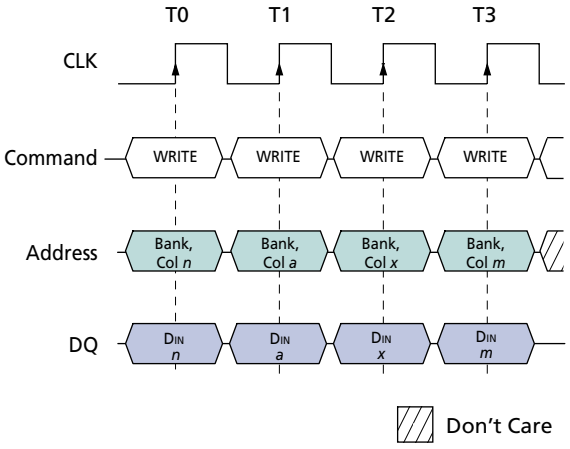
Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. After the READ command is registered, the data inputs is ignored, and WRITEs will not be executed. An example is shown in Figure 30 on page 53. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated) and a continuous-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock plus time, regardless of frequency.

In addition, when truncating a WRITE burst at high clock frequencies (^{t}CK < 15ns), the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 31 on page 54. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

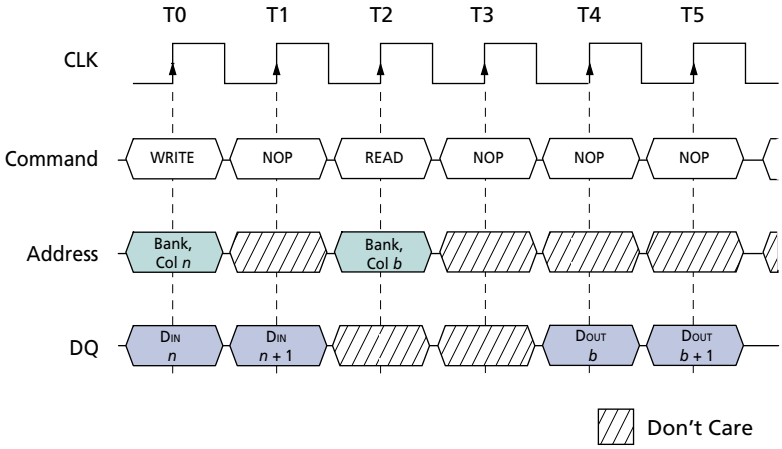
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts or continuous page bursts.

Figure 29: Random WRITE Cycles



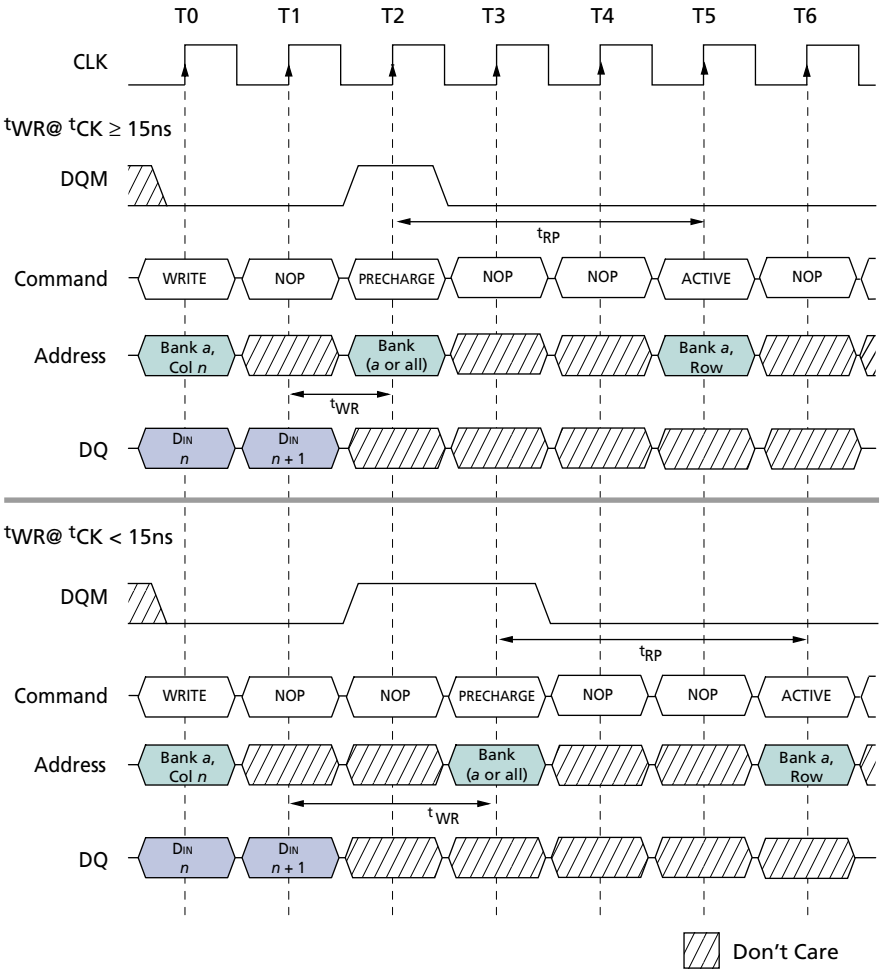
Notes: 1. Each WRITE command may be to any bank. DQM is LOW.

Figure 30: WRITE-to-READ



Notes: 1. The WRITE command may be to any bank, and the READ command may be to any bank. DQM is LOW. CL = 2 for illustration.

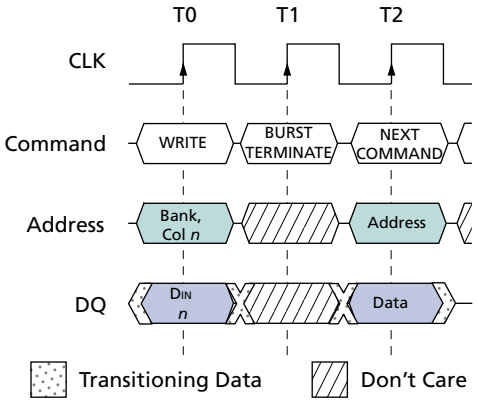
Figure 31: WRITE-to-PRECHARGE



Notes: 1. DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

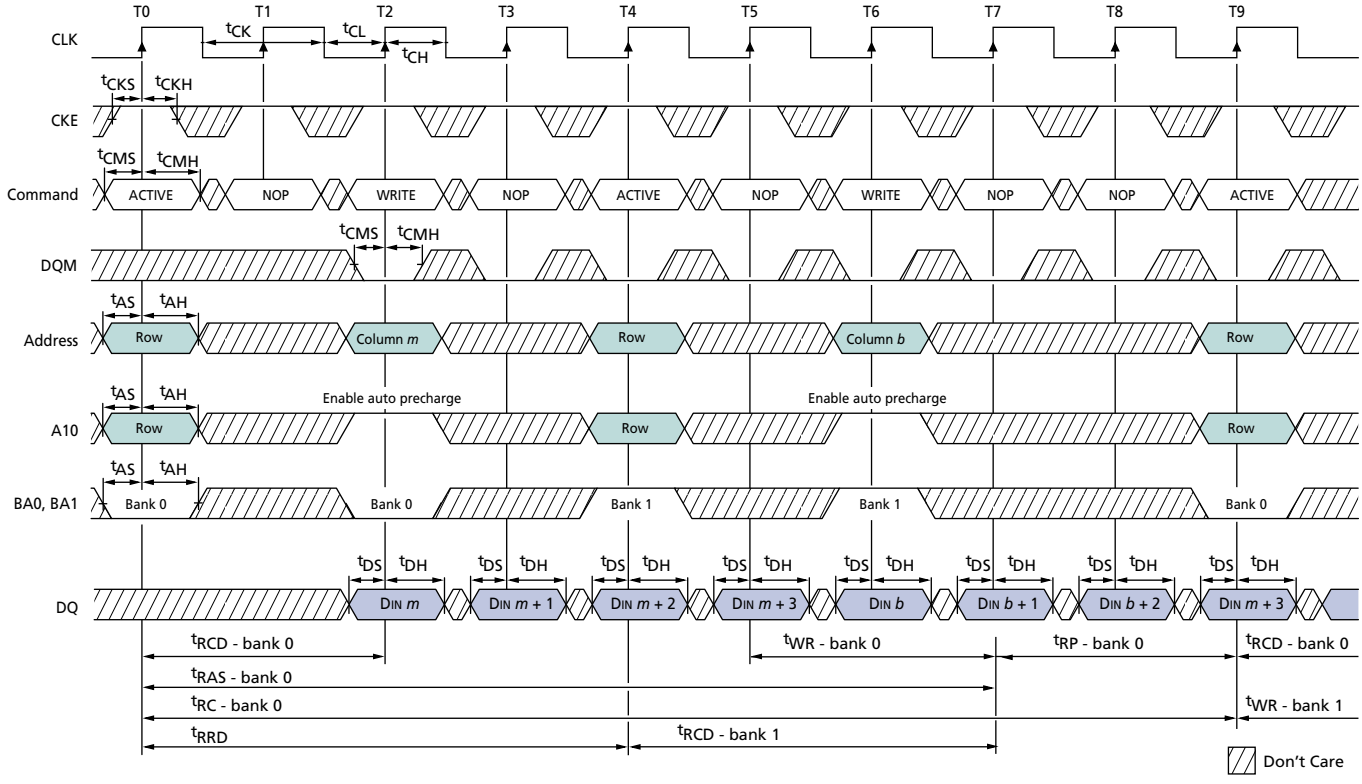
Fixed-length WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command is ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 32 on page 55, where data *n* is the last desired data element of a longer burst.

Figure 32: Terminating a WRITE Burst



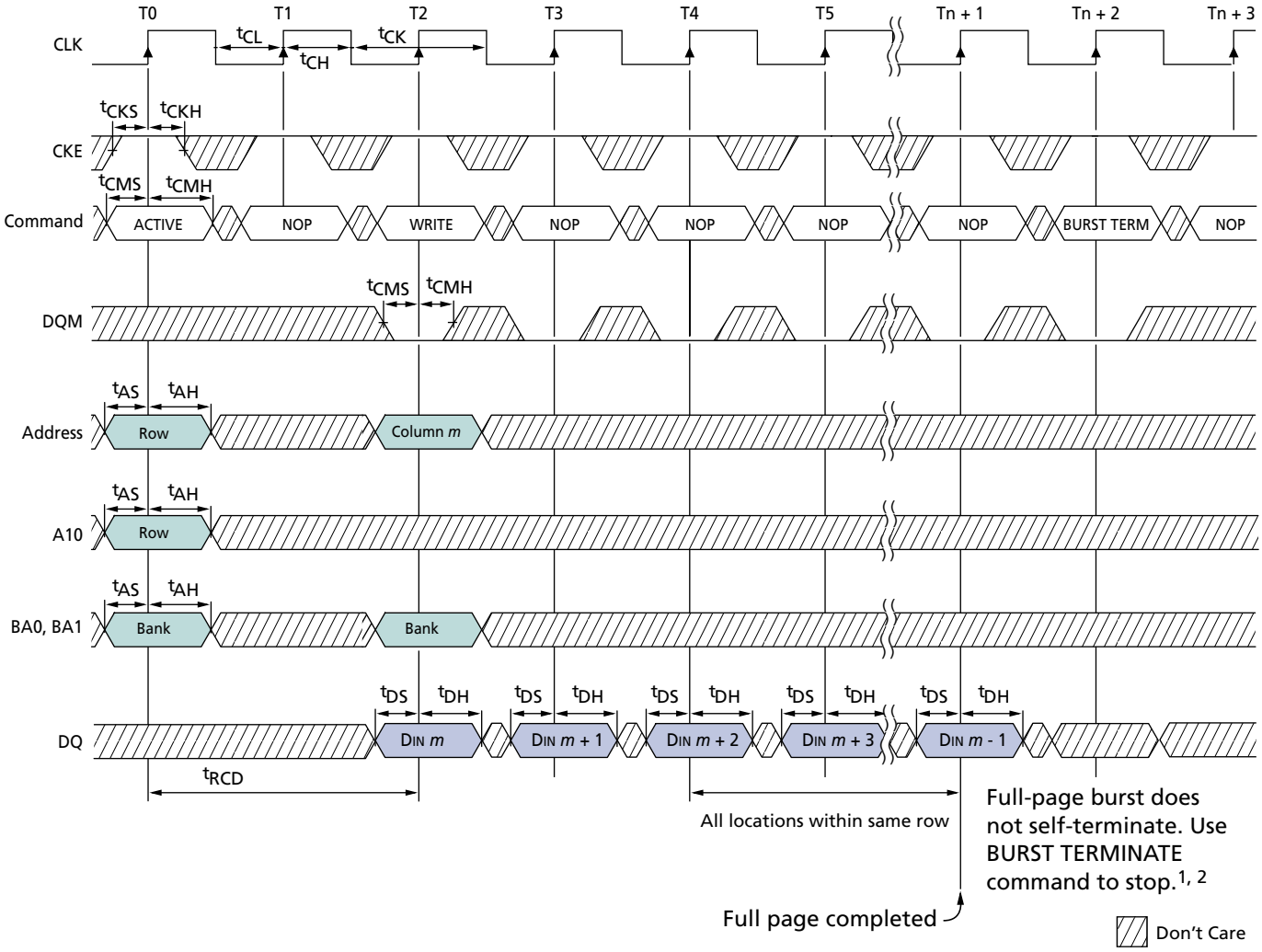
Notes: 1. DQM is LOW.

Figure 33: Alternating Bank Write Accesses



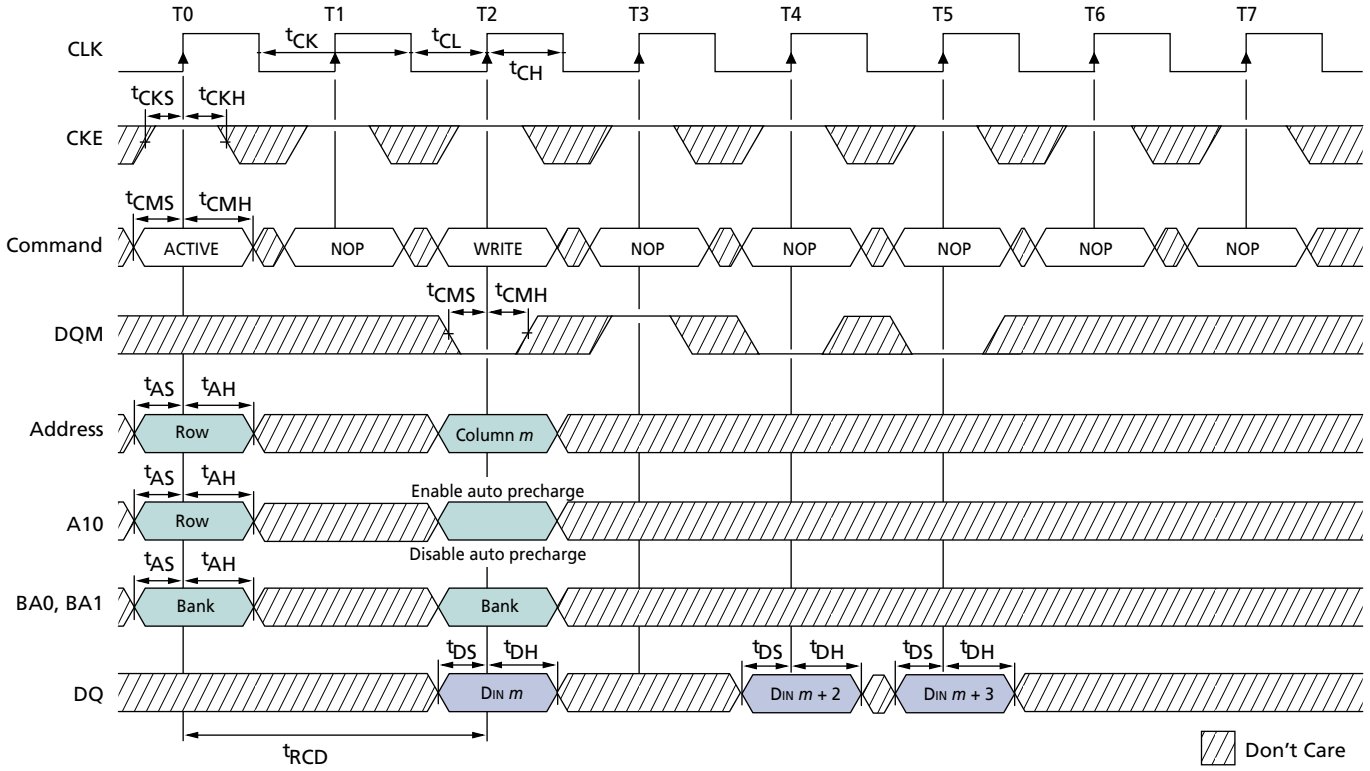
Notes: 1. For this example, BL = 4.

Figure 34: WRITE – Continuous Page Burst



Notes:
1. tWR must be satisfied prior to PRECHARGE command.
2. Page left open; no tRP

Figure 35: WRITE – DQM Operation



Notes: 1. For this example, BL = 4.

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed BL. READ commands access columns according to the programmed BL and sequence, just as in the normal mode of operation (M9 = 0).

PRECHARGE

The PRECHARGE command (see Figure 12 on page 29) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE

command is automatically performed upon completion of the READ or WRITE burst, except in the continuous page burst mode, where auto precharge does not apply. In the specific case of write burst mode set to single location access with burst length set to continuous, the burst length setting is the overriding setting and auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Burst Type section on page 38.

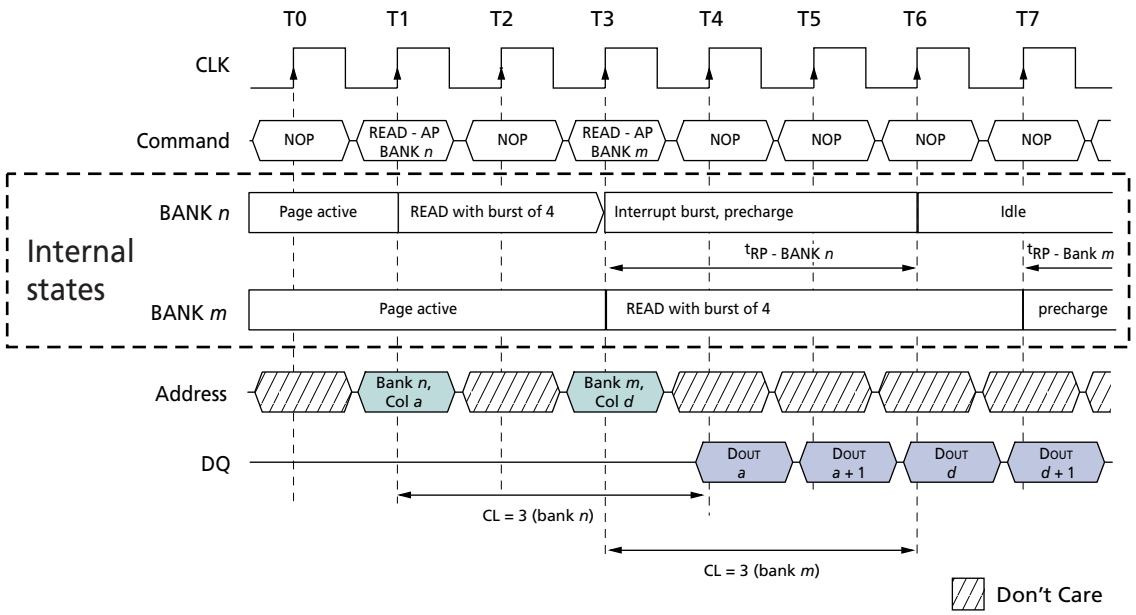
Concurrent Auto Precharge

Initiating an access command (READ or WRITE) to a second bank while an access command with auto precharge enabled on a first bank is executing is not supported by SDRAMs, unless the SDRAM supports concurrent auto precharge. Micron SDRAMs support concurrent auto precharge. Four cases where concurrent auto precharge occurs are defined below; two are for READ with auto precharge, two are for WRITE with auto precharge.

READ with Auto Precharge

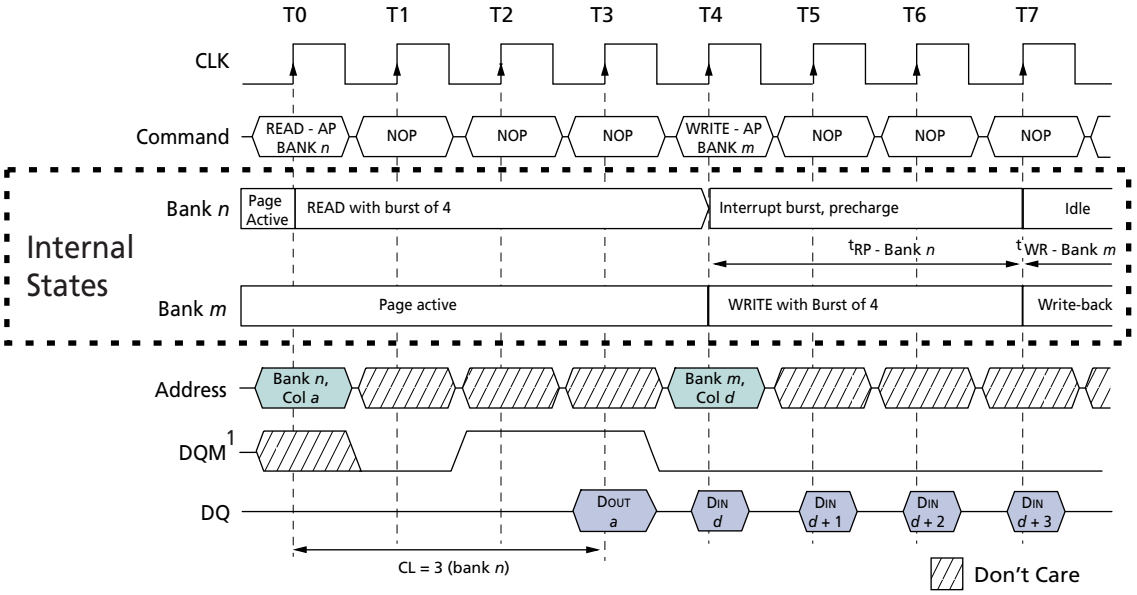
1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n*, CL later. The precharge to bank *n* begins when the READ to bank *m* is registered (see Figure 36).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* begins when the WRITE to bank *m* is registered (see Figure 37 on page 59).

Figure 36: READ with Auto Precharge Interrupted by a READ



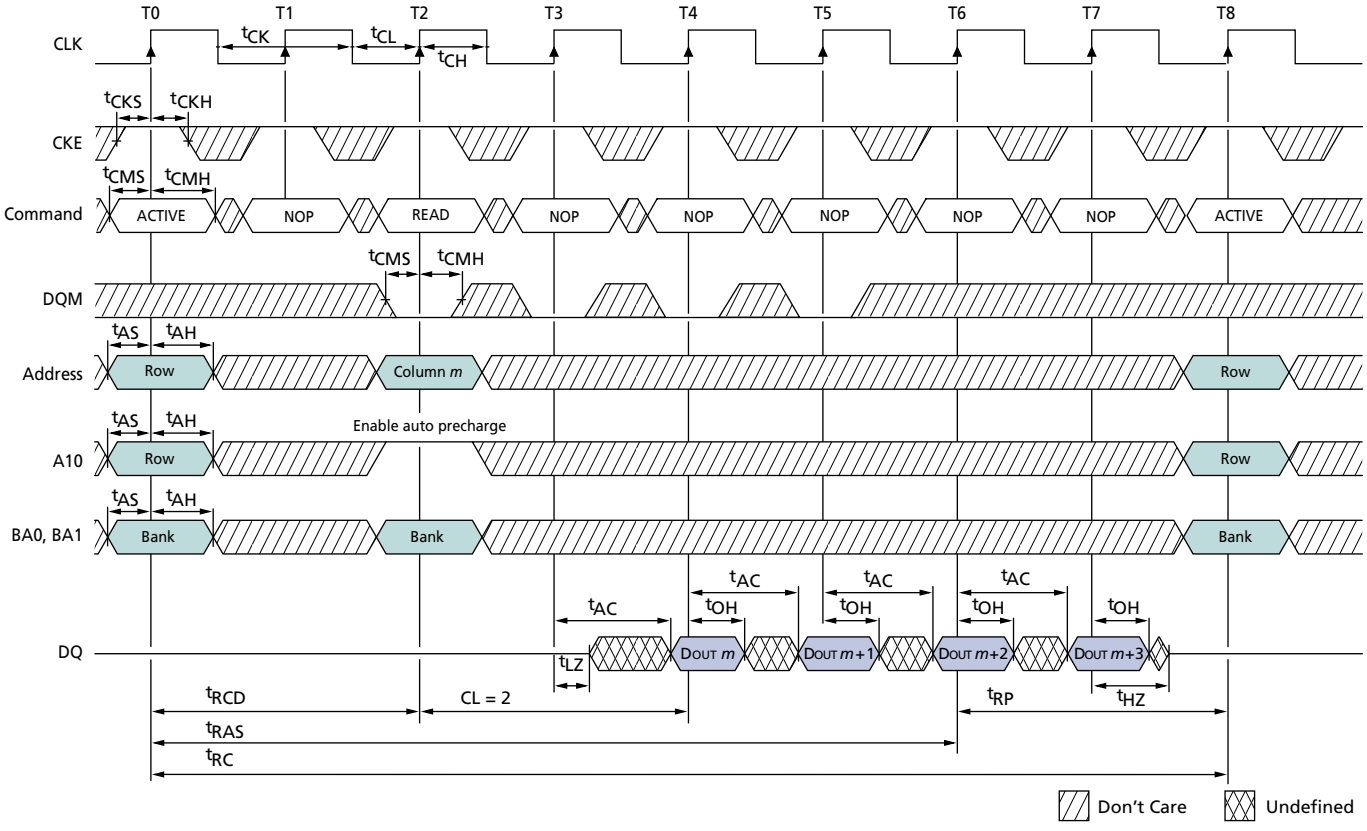
Notes: 1. DQM is LOW.

Figure 37: READ with Auto Precharge Interrupted by a WRITE



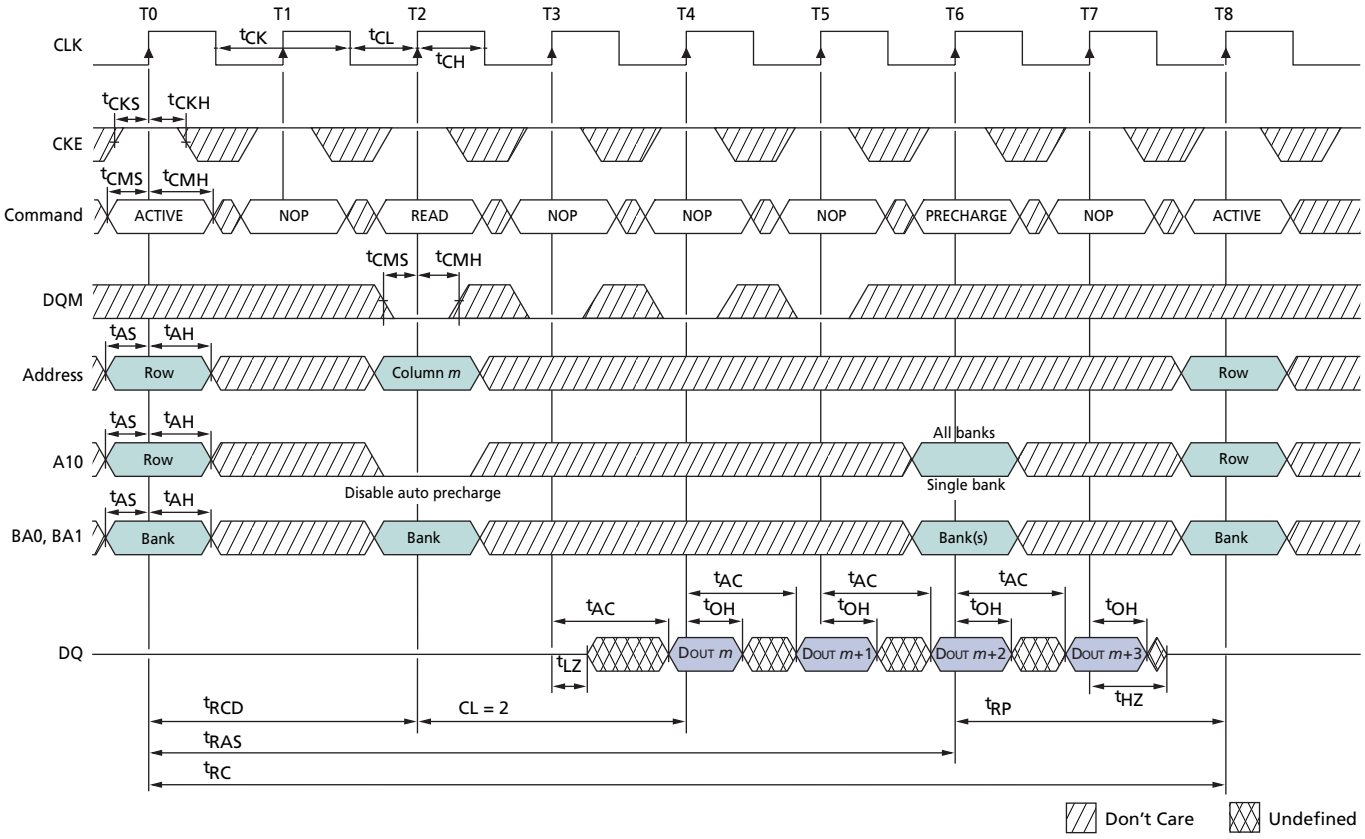
Notes: 1. DQM is HIGH at T2 to prevent DOUT *a* + 1 from contending with DIN *d* at T4.

Figure 38: READ with Auto Precharge



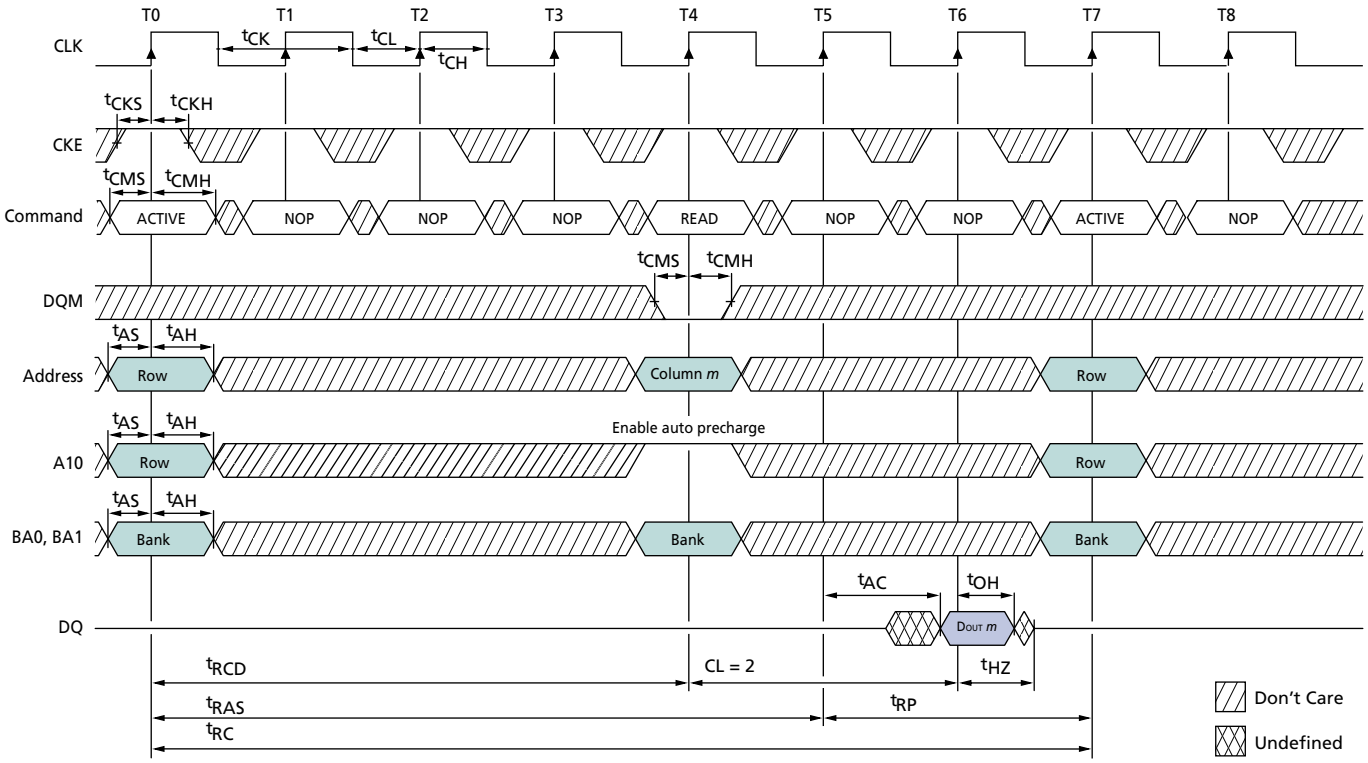
Notes: 1. For this example, BL = 4 and CL = 2.

Figure 39: READ without Auto Precharge



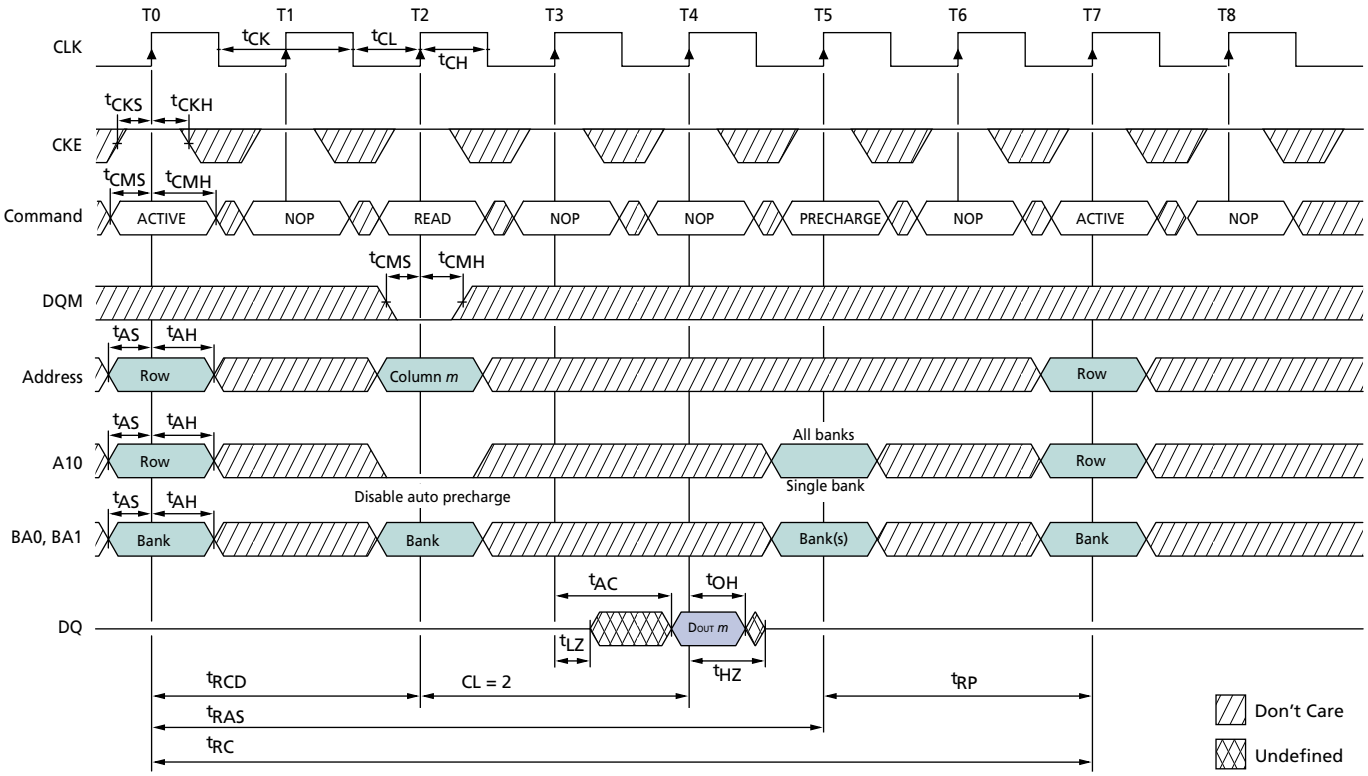
Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 40: Single READ with Auto Precharge



Notes: 1. For this example, BL = 1 and CL = 2.

Figure 41: Single READ without Auto Precharge

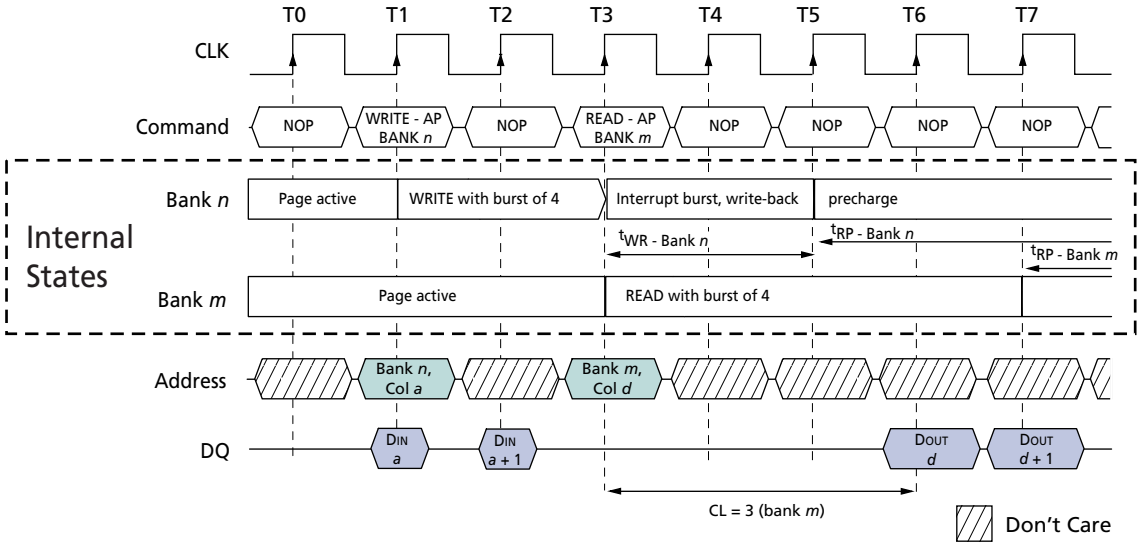


Notes: 1. For this example, BL = 1, CL = 2, and the READ burst is followed by a manual PRECHARGE.

WRITE with Auto Precharge

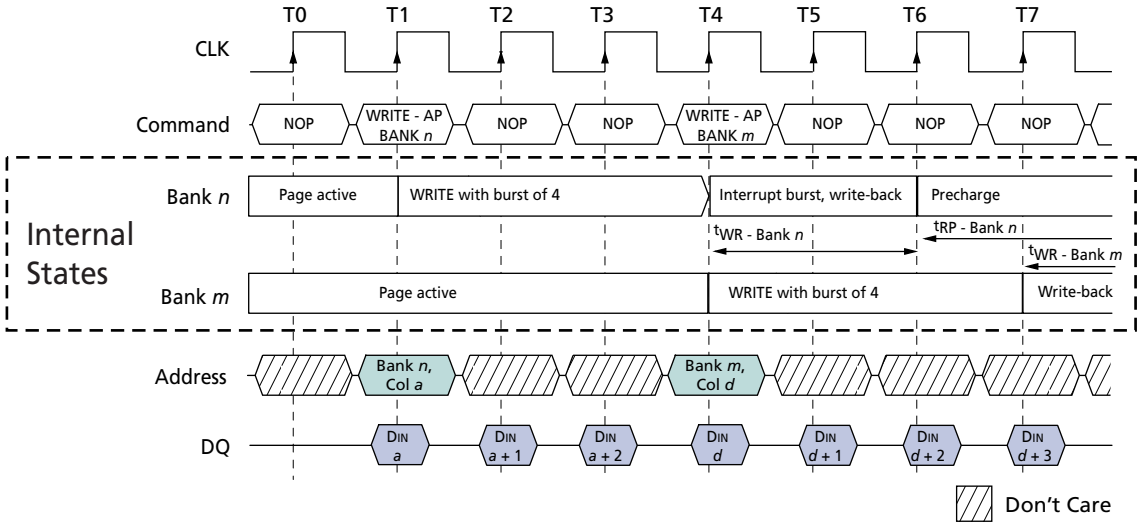
1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CL later. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (see Figure 42).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (see Figure 43).

Figure 42: WRITE with Auto Precharge Interrupted by a READ



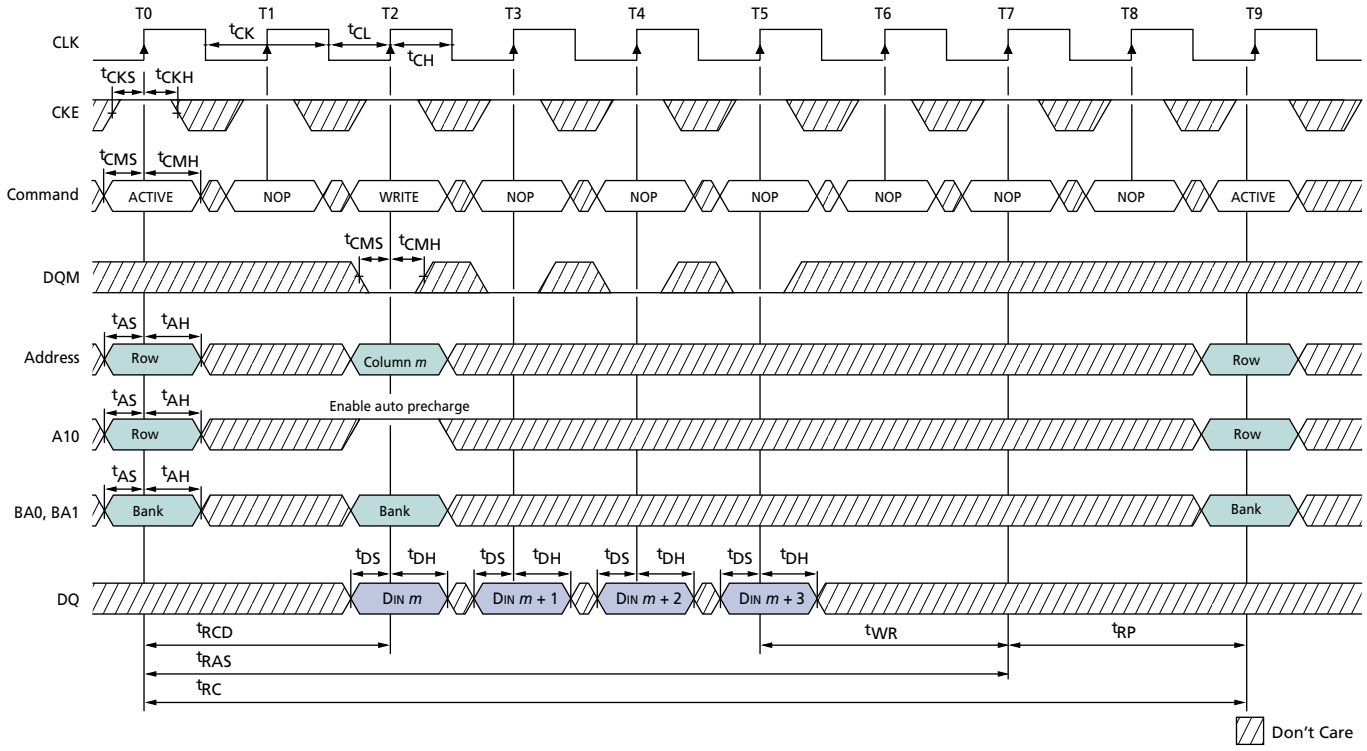
Notes: 1. DQM is LOW.

Figure 43: WRITE with Auto Precharge Interrupted by a WRITE



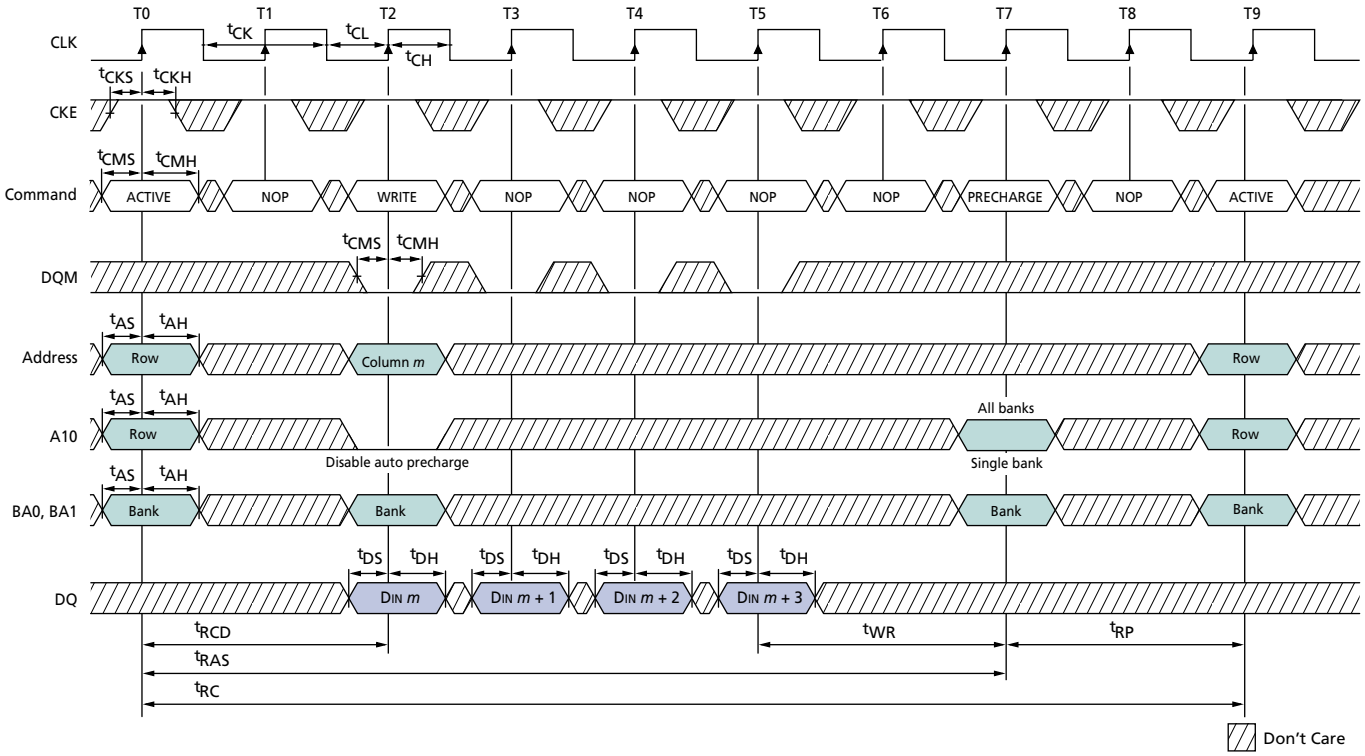
Notes: 1. DQM is LOW.

Figure 44: WRITE with Auto Precharge



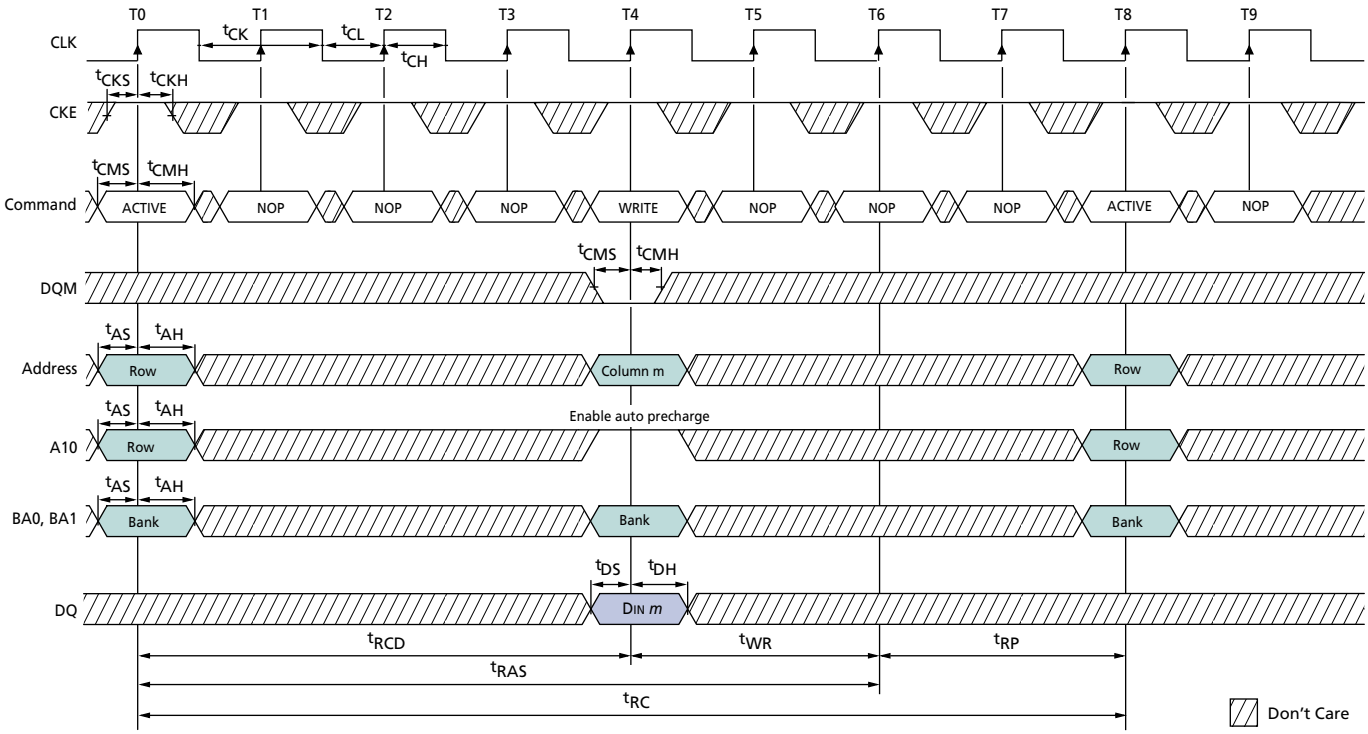
Notes: 1. For this example, BL = 4.

Figure 45: WRITE without Auto Precharge



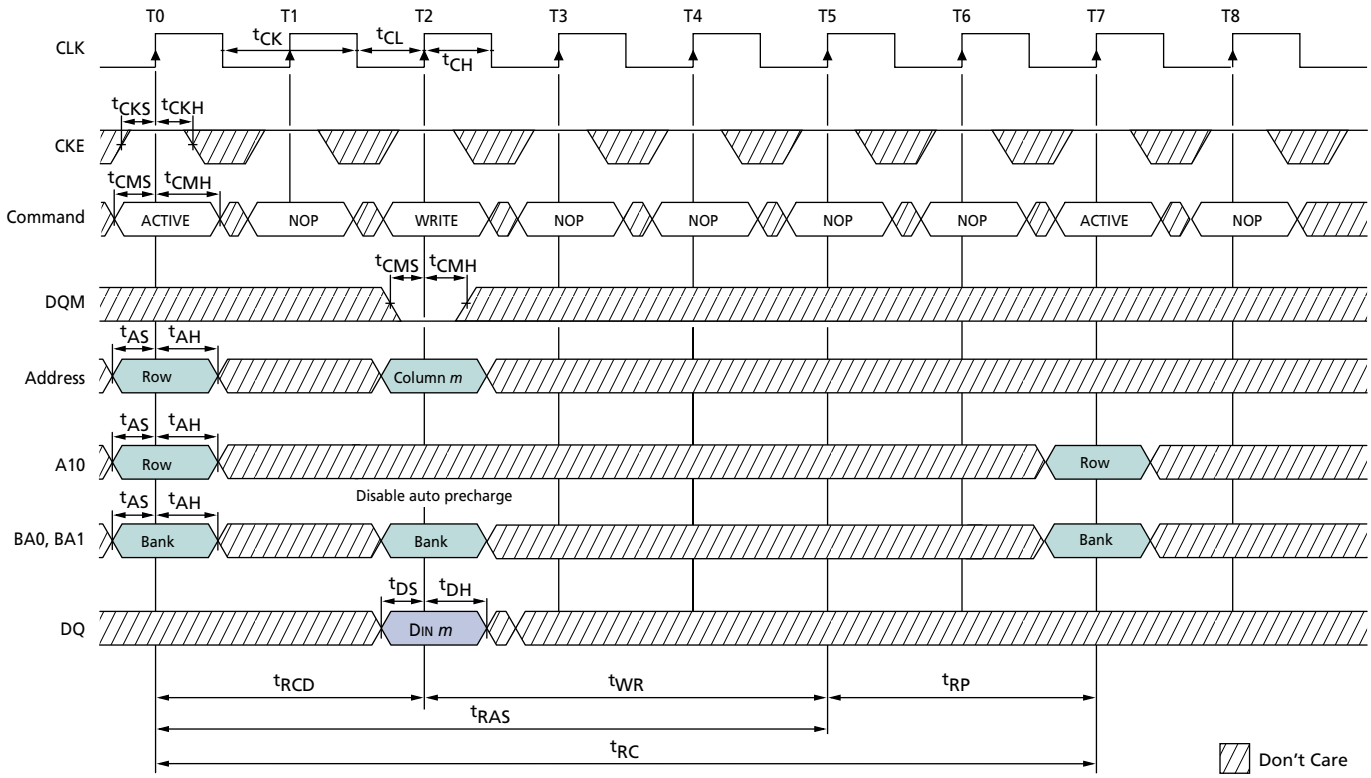
Notes: 1. For this example, BL = 1 and the WRITE burst is followed by an auto precharge.

Figure 46: Single WRITE with Auto Precharge



Notes: 1. For this example, BL = 1.

Figure 47: Single WRITE without Auto Precharge

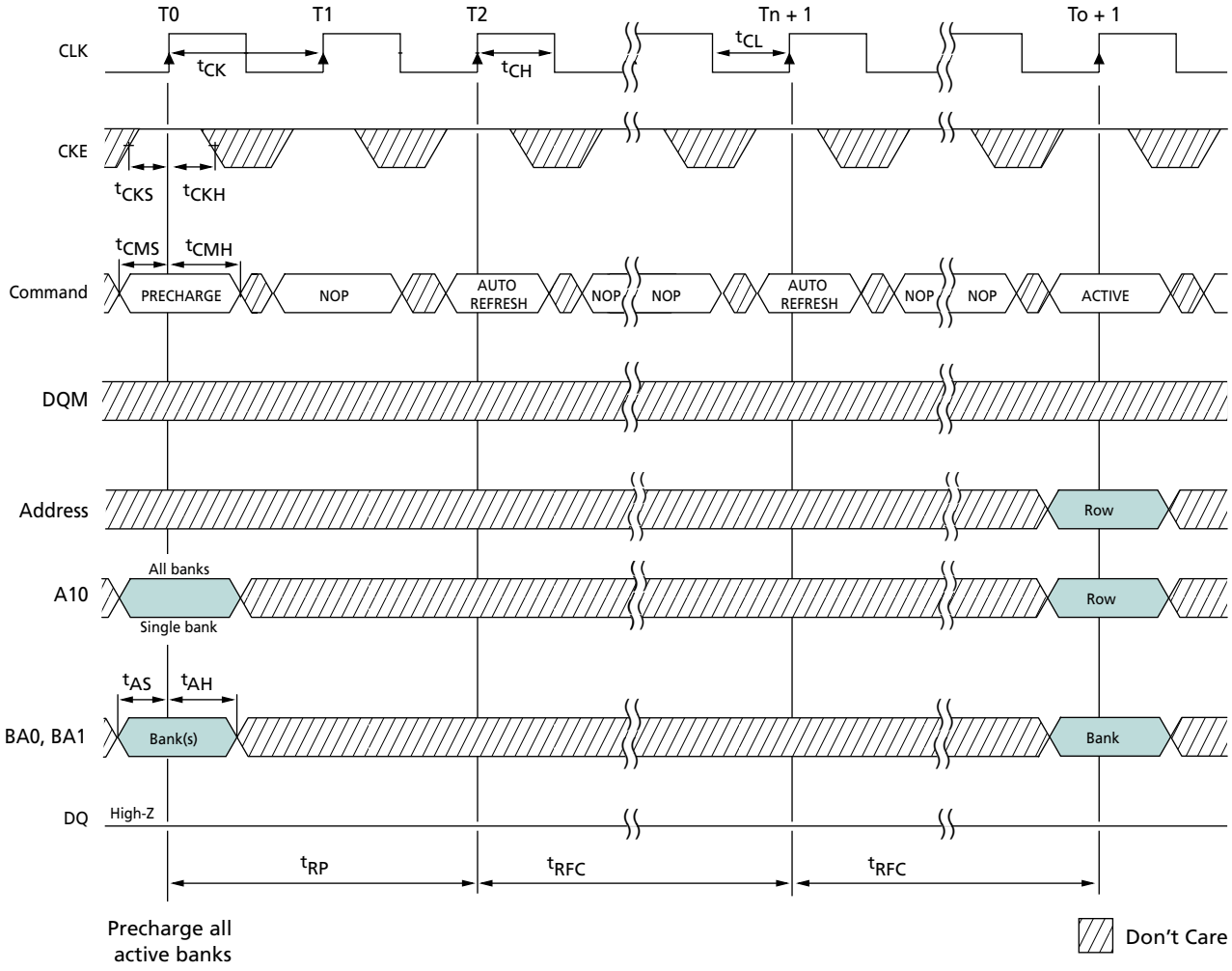


Notes: 1. For this example, BL = 1 and the WRITE burst is followed by a manual PRECHARGE.

AUTO REFRESH

The AUTO REFRESH command is used during normal operation of the SDRAM to refresh the contents of the SDRAM array. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP is met after the PRECHARGE command. Addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. After the AUTO REFRESH command is initiated, it must not be interrupted by any executable command until ^{t}RFC has been met. During ^{t}RFC time, COMMAND INHIBIT or NOP commands must be issued on each positive edge of the clock. The LP-SDRAM requires that every row be refreshed each ^{t}REF period. Providing a distributed AUTO REFRESH command calculated by dividing the refresh period (^{t}REF) by the number of rows to be refreshed, meets the timing requirement and ensure that each row is refreshed. Alternatively, a burst refresh can be employed after every ^{t}REF period, by issuing consecutive AUTO REFRESH commands for the number of rows to be refreshed at the minimum cycle rate (^{t}RFC), to satisfy the refresh requirement.

Figure 48: Auto Refresh Mode



Notes: 1. Back-to-back AUTO REFRESH commands are not required.

Self Refresh

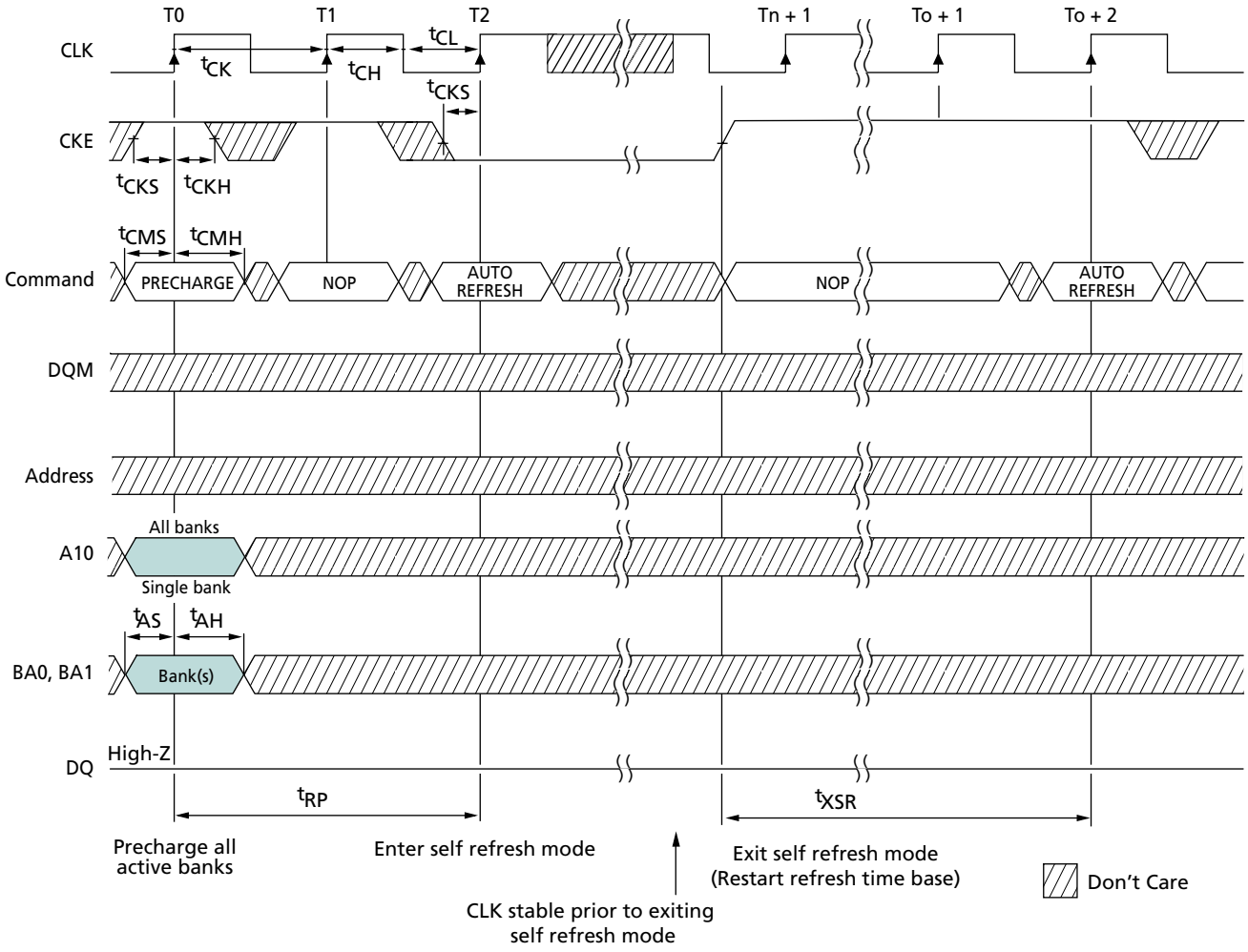
The self refresh mode can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) prior to CKE going back HIGH. After CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued according to the distributed refresh rate (^{t}REF/refresh row count) as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Figure 49: Self Refresh Mode



Notes: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required.

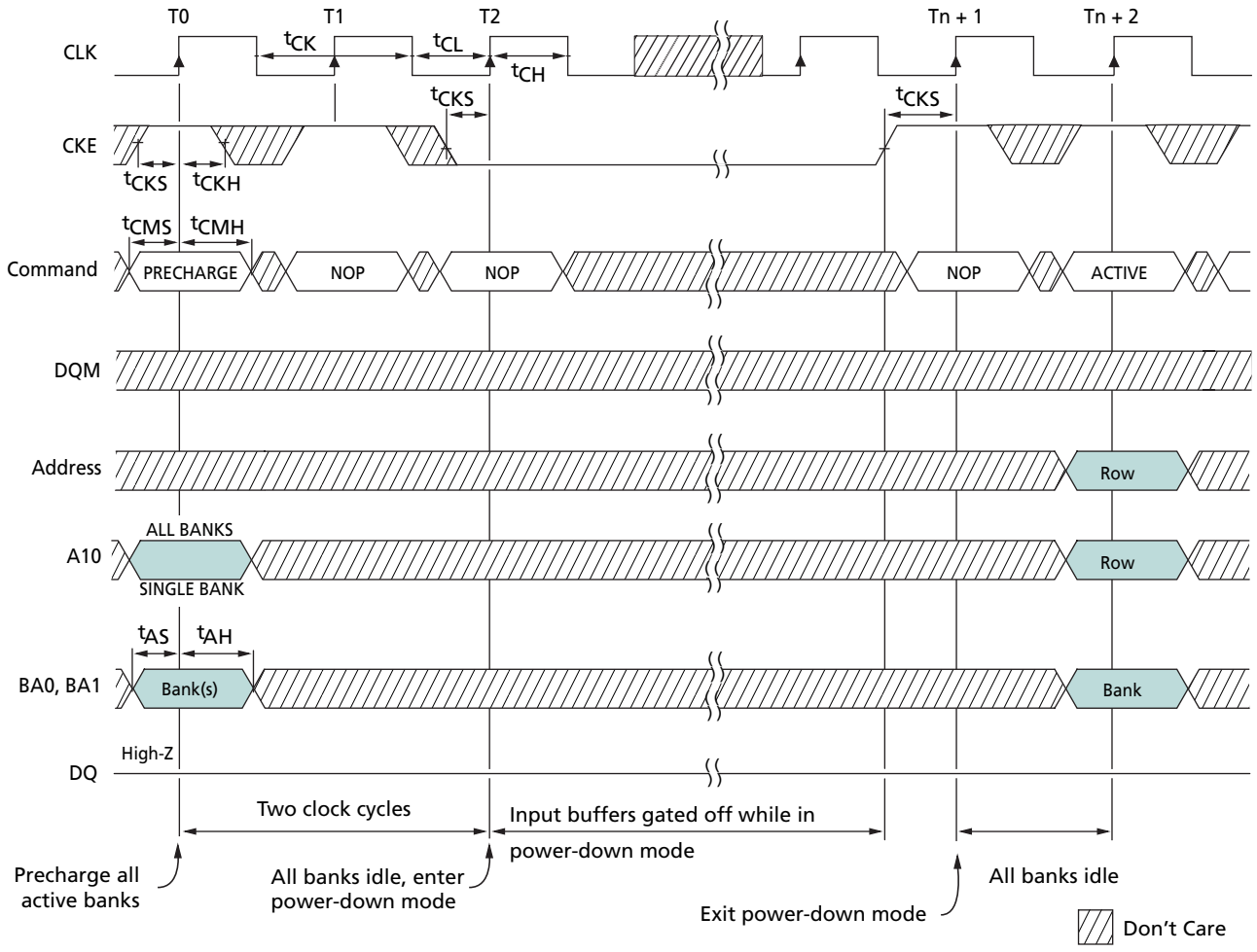
Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering

power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no REFRESH operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting ^{t}CKS) (see Figure 50 on page 70).

Figure 50: Power-Down Mode



Notes: 1. Violating refresh requirements during power-down may result in a loss of data.

Deep Power-Down

Deep power-down mode is a maximum power-saving feature achieved by shutting off the power to the entire memory array of the device. Data on the memory array will not be retained after deep power-down mode is executed. Deep power-down mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power-down.

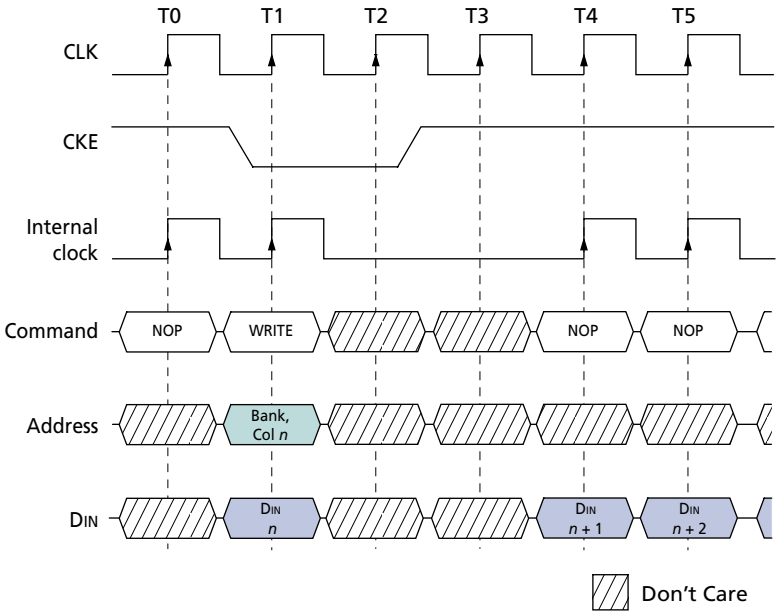
Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls at the time of a suspended internal clock edge is ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended (see examples in Figure 51 and Figure 52 on page 72).

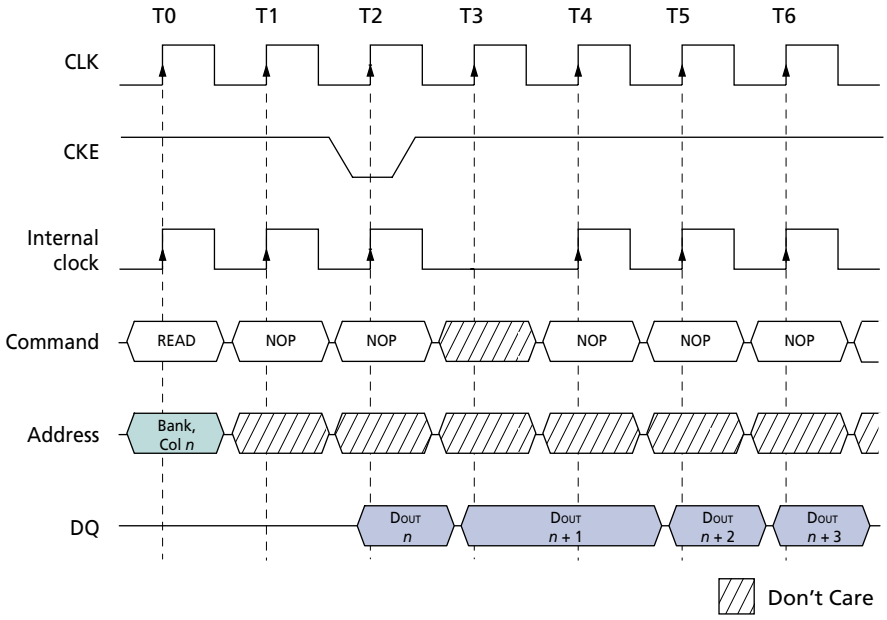
Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

Figure 51: Clock Suspend During WRITE Burst



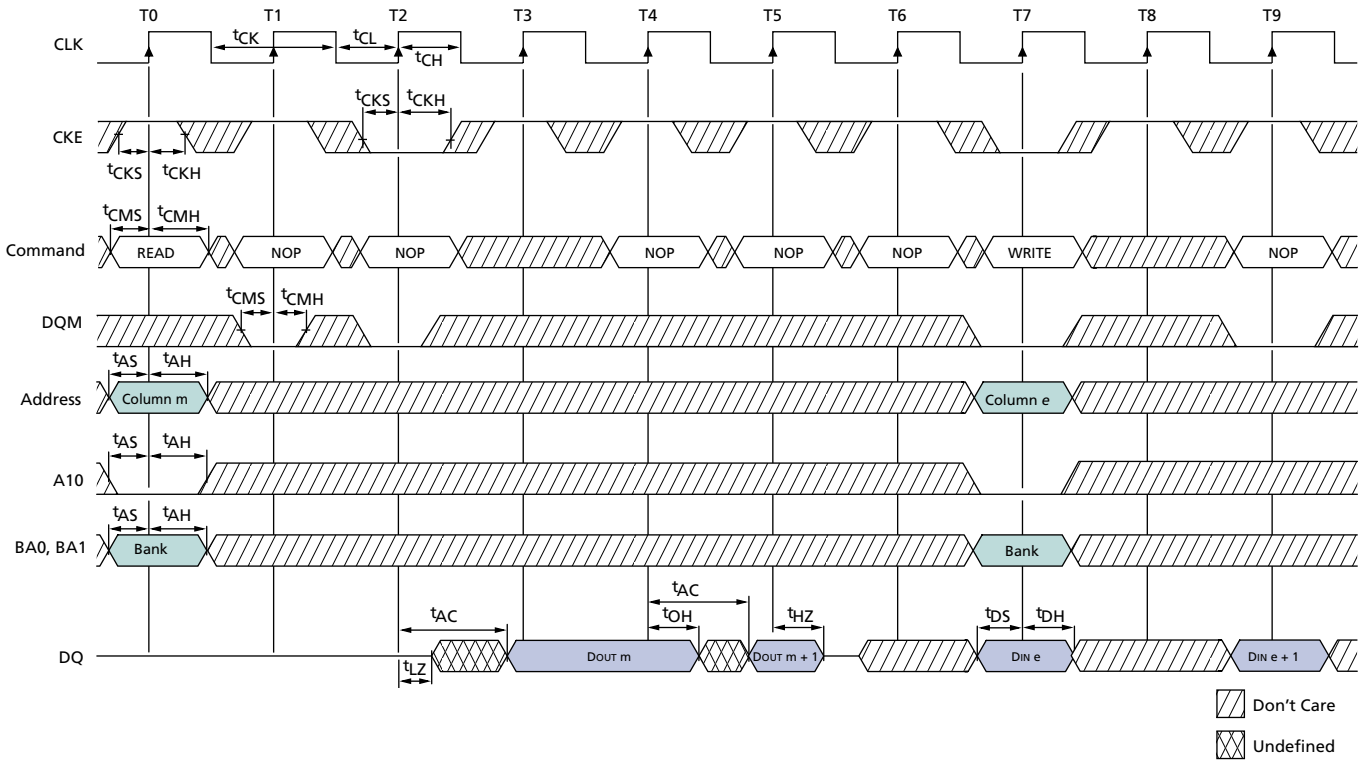
Notes: 1. For this example, BL = 4 or greater, and DQM is LOW.

Figure 52: Clock Suspend During READ Burst



Notes: 1. For this example, CL = 2, BL = 4 or greater, and DQM is LOW.

Figure 53: Clock Suspend Mode



Notes: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.

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Revision History: Device

Rev. B, Preliminary 4/08

- Table 7, Idd Specifications and Conditions (x16), on page 15: Updated IDD values and changed IDD5 auto refresh current to ^{t}RFC = 110ns.
- Table 8, Idd Specifications and Conditions (x32), on page 15: Updated IDD values and changed IDD5 auto refresh current to ^{t}RFC = 110ns
- Figure 8, Typical Idd7 Curves, on page 17: Added figure.
- Table 10, Electrical Characteristics and Recommended AC Operating Conditions, on page 18: Updated values for ^{t}CH, ^{t}CL.
- Table 12, Target Output Drive Characteristics (Full Strength), on page 21, Table 13, Target Output Drive Characteristics (Three-Quarter Strength), on page 22, and Table 14, Target Output Drive Characteristics (One-Half Strength), on page 23: Added drive-strength tables.

Rev. A, Advance 10/07

- Initial release.

Revision History: Commands, Operations, and Timing Diagrams

Update 4/08

- Added three-quarter drive strength content.
- Figure 16, Extended Mode Register, on page 40: Changed second definition to "Reserved."
- Figure 46, Single WRITE with Auto Precharge, on page 66: Relocated ^{t}RAS, ^{t}WR, and ^{t}RP parameter endpoints to align correctly with T6.