NEC

3 V SILICON MMIC L-BAND FREQUENCY DOWN CONVERTER

UPC8112T

FEATURES

BROADBAND OPERATION:

RF Input: 800 - 2000 MHz IF Output: 100 - 300 MHz

INPUT IP3: -7 dBm

LOW VOLTAGE OPERATION: 2.7~3.3 V
 LOW CURRENT CONSUMPTION: 8.5 mA

POWER SAVE FUNCTION

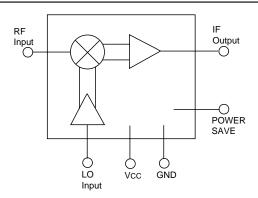
SUPER SMALL T06 PACKAGE

TAPE AND REEL PACKAGING OPTION AVAILABLE

DESCRIPTION

The UPC8112T is a silicon Monolithic Microwave Integrated Circuit which is manufactured using the NESAT III process. The NESAT III process produces transistors with ft approaching 20 GHz. This device consists of a double balance mixer, an IF amplifier, and a LO buffer amplifier. The device was designed to be used as the first down converter for GPS and

INTERNAL BLOCK DIAGRAM



wireless communications such as cellular, PCS, and 900 MHz cordless phones. Operating on a 3 volt supply, this IC is ideally suited for hand held portable designs.

NEC's stringent quality assurance and test procedures assure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (TA = 25 °C, Vcc = VPs = 3.0 V, PLoin = -10 dBm, ZL = Zs = 50 Ω unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPC8112T T06		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Icc	Circuit Current (no input signal)	mA	4.9	8.5	11.7
ICC (PS)	Circuit Current at Power Save Mode, Vcc = 3.0 V, Vps = 0.5 V	μΑ			0.1
fRFin	RF Frequency Response	GHz	0.8	1.9	2.0
fIFout	IF Frequency Response ¹	MHz	100	250	300
CG	Conversion Gain	dB dB dB	11.5 9.5	15 13 13	17.5 15.5
NF	Single Side Band Noise Figure (SSB) frein = 900 MHz, floin = 1000 MHz frein = 1.5 GHz, floin = 1.6 GHz frein = 1.9 GHz, floin = 1.66 GHz	dB dB dB		9.0 11 11.2	11 13.2
P _{1dB}	Output Power at 1 dB gain compression, fRFin = 1.9 GHz fLOin = 1.66 GHz	dBm		-5	
Psat	Saturated Output Power fRFin = 900 MHz, fLOin = 1000 MHz fRFin = 1.9 GHz, fLOin = 1.66 GHz (PRFin = -10 dBm)	dBm dBm	-6.5 -7	-2.5 -3	
IIP3	Input 3rd Order Intercept Point, frein = 900 MHz, floin = 1000 MHz frein = 1.5 GHz, floin = 1.6 GHz frein = 1.9 GHz, floin = 1.66 GHz	dBm dBm dBm		-10 -9 -7	
LORF	LO Leakage at RF pin, frrin = 900 MHz, fLoin = 1000 MHz frrin = 1.5 GHz, fLoin = 1.6 GHz frrin = 1.9 GHz, fLoin = 1.66 GHz	dBm dBm dBm		-45 -46 -45	
LOIF	LO Leakage at IF pin, frFin = 900 MHz, fLoin = 1000 MHz frFin = 1.5 GHz, fLoin = 1.6 GHz frFin = 1.9 GHz, fLoin = 1.66 GHz	dBm dBm dBm		-32 -33 -30	
RFLO	RF Leakage at LO Pin frfin = 900 MHz, fLoin = 1000 MHz 2 frfin = 1.5 GHz, fLoin = 1.6 GHz 2 frfin = 1.9 GHz, fLoin = 1.66 GHz 2	dBm dBm dBm		-80 -57 -55	

Notes:

1. External matching required.

2. PRFin = -30 dBm

California Eastern Laboratories

ABSOLUTE MAXIMUM RATINGS¹ (TA = 25°C)

SYMBOLS	SYMBOLS PARAMETERS		RATINGS	
Vcc	Vcc Supply Voltage		3.6	
Icc Circuit Current		mA	77.7	
PD Power Dissipation ²		mW	280	
Top Operating Temperature		°C	-40 to +85	
Tstg Storage Temperature		°C	-55 to +150	

Notes:

- Operation in excess of any one of these parameters may result in permanent damage.
- 2. Mounted on a 50 x 50 x 1.6 mm epoxy glass PWB ($TA = +85^{\circ}C$).

RECOMMENDED OPERATING CONDITIONS

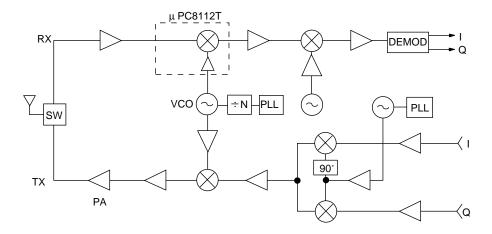
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
Vcc	Supply Voltage	V	2.7	3.0	3.3
Тор	Operating Temperature	°C	-40	+25	+85
PLOin	LO Input Level	dBm	-15	-10	0
fRFin	RF Input Frequency	GHz	0.8	1.9	2.0
fIFout	IF Output Frequency	MHz	100	250	300

PIN FUNCTIONS

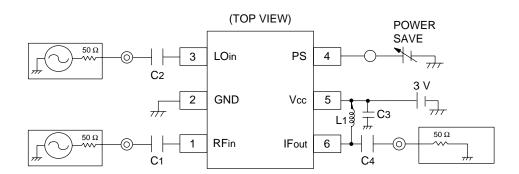
Pin No.	Symbol	Pin Voltage	Description	Internal Equivalent Circuit
5	Vcc	2.7 ~ 3.3	Supply Voltage pin. Connect a bypass capacitor (e.g., 1000 pF) to minimize ground impedance.	5
6	ІГоит	Same as Vcc voltage through external inductor	IF output pin is an open collector with high impedance. External LC matching circuit is required.	from LO AMP
1	RFIIN	1.2	RF input pin to mixer. Mixer is a double balanced Gilbert cell type. Input RF signal to the pin with a $50~\Omega$ source impedance through a coupling capacitor.	
2	GND	0	Ground pin. Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible to minimize ground impedance.	
3	LOIN	1.4	LO input pin to a differential buffer amplifier. Input LO signal through a coupling capacitor. Recommended input level: -15 to 0 dBm.	3 to mixer
4	PS	Vcc or GND	Power-save control pin. Voltage on this pin controls ON/OFF operation as follows: Operation VPS ON ⊕2.5 V OFF 0-0.5 V	(a) (b) (c) (c) (c) (c) (c) (c) (c) (c) (c) (c

TYPICAL APPLICATION EXAMPLE

PCS or DIGITAL CELLULAR



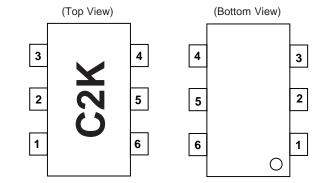
TEST CIRCUIT



Note: 1. C1, C2, C3 are 1,000 pF capacitors.
2. L1 and C4 are matching elements.
L1 = 100nH and C4 = 2.7 pF for fiF = 240 MHz

OUTLINE DIMENSIONS (Units in mm)

LEAD CONNECTIONS

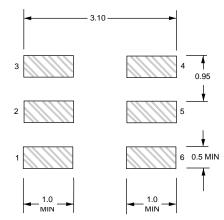


- 1. RFIN
- 2. GND
- 3. LOIN
- 4. PS
- 5. Vcc
- 6. IFout

RECOMMENDED P.C.B. LAYOUT (Units in mm)

Note:

All dimensions are typical unless otherwise specified.



ORDERING INFORMATION

PART NUMBER	QTY
UPC8112T-E3	3K/Reel