12-Bit, Monitor and Control System with Multichannel, ADC, DACs, Temperature Sensor and Current Sense

Preliminary Technical Data

AD7294

FEATURES

- 12-bit SAR ADC with 3 µs conversion time
  - 4 uncommitted analog inputs
    - Differential/single ended
    - Input range: 0 to V_{REF}, 0 to 2 V_{REF}
  - 2 high-side current sense inputs
    - 5 V to 59.4 V operating range
    - >±1% full-scale accuracy
    - ±200 mV input range
  - 2 external diode temperature sensor inputs
    - −55°C to +150°C measurement range
    - ±2°C accuracy
    - Series resistance cancellation
  - 1 internal temperature sensor
    - ±2°C accuracy
  - Built-in monitoring features
    - Minimum/maximum recorder for each channel
    - Programmable alert thresholds
    - Programmable hysteresis
  - 4-channel, 12-bit monotonic 15 V DACs
    - 5 V span, 0 V to 10 V offset
    - 10 µs settling time
    - 10 mA sink and source capability
    - Power-on resets (POR) to 0 V
  - Internal 2.5 V reference
  - 2-wire fast mode I^2C interface
  - Temperature range: −40°C to +105°C
  - Package types: 56-lead LFCSP and 64-lead TQFP

GENERAL DESCRIPTION

The AD7294 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature integrated into a single-chip solution. The part includes low voltage (±200 mV) analog input sense amplifiers for current monitoring across shunt resistors, temperature sense inputs, and four uncommitted analog input channels multiplexed into a 200 kSPS SAR analog-to-digital converter (ADC). An internal low ppm reference is provided to drive both the digital-to-analog converter (DAC) and ADC. Four 12-bit DACs provide the outputs for voltage control. The AD7294 also includes limit registers for alarm functions. The part is designed on a high voltage DMOS process for high voltage compliance, 59.4 V on the current sense inputs, and up to 15 V DAC output voltage.

The DACs provide digital control with 1.2 mV resolution to control the bias currents of the power transistors. Thermal diode based temperature sensors are incorporated to compensate for temperature effects. The ADC monitors the high-side current and temperature. All this functionality is provided in a 56-lead LFCSP and a 64-lead TQFP operating over a temperature range of −40°C to +105°C.

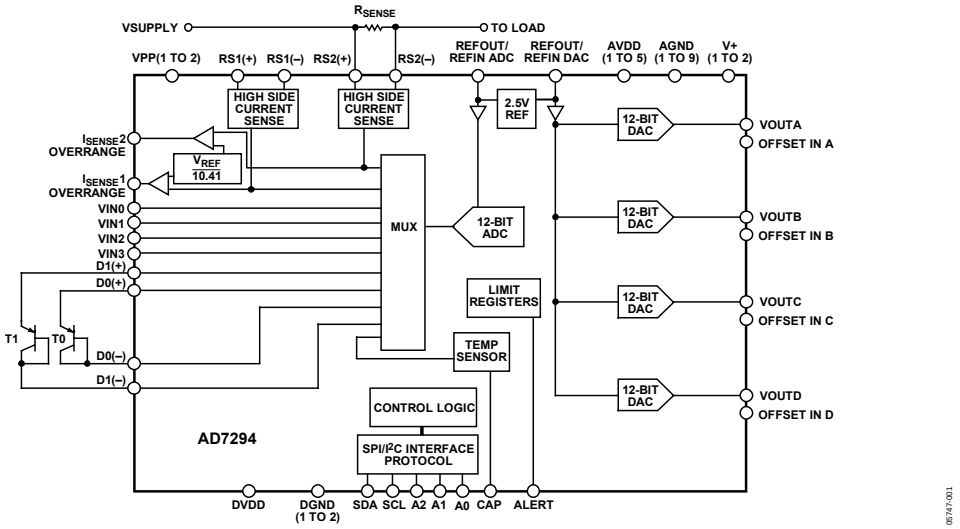

Figure 1. Typical Configuration for AD7294 in Cellular Base Station RF LDMOS Power Amplifier Control

Rev. PrD

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DAC SPECIFICATIONS

AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, AGND = DGND = 0 V, internal 2.5 V reference. V_{DRIVE} range from 2.7 V to 5.5 V. Temperature range for B version: −40°C to +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Offset pin is open, therefore, DAC output span is from 0 V to 5 V. DAC OUT V+ is set at 5.5V Specifications guaranteed by design and characterization, not subject to production testing.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					
Resolution	12			Bits	
Relative Accuracy (INL)			±4	LSB	
Differential Nonlinearity (DNL)			±1	LSB	Guaranteed monotonic
Zero-Scale Error			4	mV	
Full-Scale Error			TBD		
Offset Error			±4	mV	Measured in the linear region
Offset Error TC		±5		µV/°C	
Gain Error			±0.024	% FSR	
Gain Temperature Coefficient		2		ppm FSR/°C	
DC Crosstalk			0.5	LSB	
DAC OUTPUT CHARACTERISTICS					
Output Voltage Span	0		5	V	With a 2.5 V internal reference
Output Voltage Offset	0		10	V	The 5 V output voltage span can be positioned in the 0 V to 15 V range
Offset Input Span	0		5		$V_{OUT} = 3V_{OFFSET} - 2V_{REF} + V_{DAC}$
DC Input Impedance		75		kΩ	
Output Voltage Settling Time		10		µs	¼ to ¾ change within ½ LSB
Slew Rate		1		V/µs	
0.1Hz to 10Hz Noise		TBD			100nF capacitor to ground on Offset pin
Output Noise Spectral Density		TBD			100nF capacitor to ground on Offset pin
Short-Circuit Current			40	mA	FS current shorted to ground
Load Current			±10	mA	Source and/or sink within 200 mV of supply
Capacitive Load Stability					
$R_L = \infty$		1000		pF	
DC Output Impedance			0.5	Ω	
Power Supply Sensitivity					
DC Power Supply Rejection Ratio		–85		dB	ΔV_{DD} = ±10%
REFERENCE					
Reference Output Voltage	2.49		2.51	V	Minimum and maximum for 4.5V and 5.5V
Reference Input Voltage Range	0.1		2.5	V	
DC Leakage Current			±30	µA	
Input Current		100		µA	In external reference mode, resistor string draws current
Input Capacitance		20		pF	
V_{REF} Output Impedance		25		Ω	
Reference Temperature Coefficient		10	25	ppm/°C	10 ppm/°C typical

ADC SPECIFICATIONS

AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, AGND = DGND = 0 V, internal 2.5 V reference. V_{DRIVE} range from 2.7 V to 5.5 V. Temperature range for B version: −40°C to +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Specifications guaranteed by design and characterization, not subject to production test.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY					
Resolution		12		Bits	
Integral Nonlinearity (INL)		±0.5	±1	LSB	Differential mode
		TBD		LSB	Single-ended or pseudo differential mode
Differential Nonlinearity (DNL)			±1	LSB	Differential mode
		TBD		LSB	Single-ended or pseudo differential mode
Straight Binary Output Coding					
Offset Error			±7	LSB	
Offset Error Match		±2		LSB	
Gain Error			±2.5	LSB	
Gain Error Match		±0.5		LSB	
Twos Complement Output Coding					
Positive Gain Error			±2	LSB	
Positive Gain Error Match		±0.5		LSB	
Zero Code Error			±5	LSB	
Zero Code Error Match		±1		LSB	
Negative Gain Error			±2	LSB	
Negative Gain Error Match		±0.5		LSB	
Conversion Time			3	µs	
Autocycle Update Rate		50		µs	
Analog Input Range	0		V_{REF} or $2V_{REF}$	V	
Input Capacitance		30		pF	
DC Input Leakage Current			±1	µA	
DYNAMIC PERFORMANCE					
Signal-to-Noise Ratio (SNR)	71			dB	f_{IN} = 50 kHz sine wave; differential mode
	69			dB	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Signal-to-Noise + Distortion (SINAD) Ratio	70			dB	f_{IN} = 50 kHz sine wave; differential mode
	68			dB	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Total Harmonic Distortion (THD)			−77	dB	f_{IN} = 50 kHz sine wave; differential mode
			−73	dB	f_{IN} = 50 kHz sine wave; single-ended and pseudo differential modes
Spurious-Free Dynamic Range (SFDR)			−75	dB	f_{IN} = 50 kHz sine wave
Channel-to-Channel Isolation			−88	dB	
TEMPERATURE SENSOR—INTERNAL					
Operating Range	−40		+105	°C	
Accuracy			±2	°C	Internal temperature sensor, T_A = −10°C to +90°C
Resolution		0.25		°C	LSB size
Update Rate		5		ms	
TEMPERATURE SENSOR—EXTERNAL					External transistor = 2N3906
Operating Range	−55		+150	°C	Limited by external diode
Accuracy			±2	°C	T_A = T_{DIODE}= −10°C to +90°C
			±2	°C	T_{DIODE} = −10°C to +90°C, T_A = +25°C
Resolution		0.25		°C	LSB size
Low Level Output Current Source		8		µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Medium Level Output Current Source		32		µA	
High Level Output Current Source		128		µA	
Maximum Series Resistance for External Diode			100	Ω	For < ±0.25°C additional error
CURRENT SENSE					
Supply Range	AV_{DD}		59.4	V	Gives ±200 mV range with +2.5 V reference
Gain	12.375		12.625		
RS(+) and RS(–) Input Bias Current		25		µA	
CMRR/PSRR		80		dB	Pin connected to power supply
Accuracy		1		LSB @ 12 bits	
Offset Error		50		µV	
Offset Drift		1		µV/°C	
Amplifier Peak-To-Peak Noise		400		µV	
V_{PP} Supply Current		TBD			
I_{SENSE} V_{DD} Supply Current		TBD			
REFERENCE					
Reference Output Voltage	2.49		2.51	V	
Reference Input Voltage Range	0.1		2.5	V	
DC Leakage Current			±30	µA	
Input Capacitance		20		pF	
V_{REF} Output Impedance		25		Ω	
Reference Temperature Coefficient		10	25	ppm/°C	

GENERAL SPECIFICATIONS

AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, AGND = DGND= 0 V, internal 2.5 V reference. V_{DRIVE} range from 2.7 V to 5.5 V. Temperature range for B version: −40°C to +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Specifications guaranteed by design and characterization, not subject to production test.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL ONLY)					
Input High Voltage, V_{IH}	0.7 V_{DRIVE}			V	
Input Low Voltage, V_{IL}			0.3 V_{DRIVE}	V	
Input Leakage Current, I_{IN}			±1	µA	
Input Hysteresis, V_{HYST}	0.05 V_{DRIVE}			V	
Input Capacitance, C_{IN}		8		pF	
Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns
I^2C® Address Pins Maximum Capacitance if Floating			30	pF	Tristate input
DAC High-Z		TBD			Input with pull-down resistor
LOGIC OUTPUTS					
SDA, ALERT					SDA and ALERT are open-drain output
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3 mA for open-drain outputs
			0.6	V	I_{SINK} = 6 mA for open-drain outputs
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance		8		pF	
ISENSE OVERRANGE					ISENSE OVERRANGE is a push-pull output
Output High Voltage, V_{OH}			V_{DRIVE} − 0.2	V	I_{SOURCE} = 200 µA for push-pull outputs
Output Low Voltage, V_{OL}			0.2	V	I_{SINK} = 200 µA for push-pull outputs
POWER REQUIREMENTS					
V_{PP}	AV_{DD}		60	V	
AV_{DD}	4.5		5.5	V	
V(+)	4.5		16.5	V	
DV_{DD}	4.5		5.5	V	
V_{DRIVE}	3		5.5	V	
I_{PP}	TBD				
AI_{DD}	TBD			mA	Outputs unloaded
DI_{DD}			1	mA	V_{IH} = DV_{DD}, V_{IL} = DGND
AI_{DD} (Power-Down)			5	µA	
DI_{DD} (Power-Down)			5	µA	
V+ Supply	TBD	TBD	TBD	mA	
Power Dissipation			TBD	mW	

TIMING CHARACTERISTICS

I²C Serial Interface

AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, AGND = DGND = 0 V. V_{DRIVE} range from 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Specifications guaranteed by design and characterization, not subject to production test.

Table 2.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data set-up time
t_6[2]	0.9	µs max	$t_{HD,DAT}$, data hold time
	0	µs min	$t_{HD,DAT}$, data hold time
t_7	0.6	µs min	$t_{SU,STA}$, set-up time for repeated start
t_8	0.6	µs min	$t_{SU,STO}$, stop condition set-up time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_R, rise time of SCL and SDA when receiving
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	$20 + 0.1C_b$[3]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] See Figure 2.
[2] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} minimum of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[3] C_b is the total capacitance in pF of one bus line. t_R and t_F are measured between 0.3 DV_{DD} and 0.7 DV_{DD}.

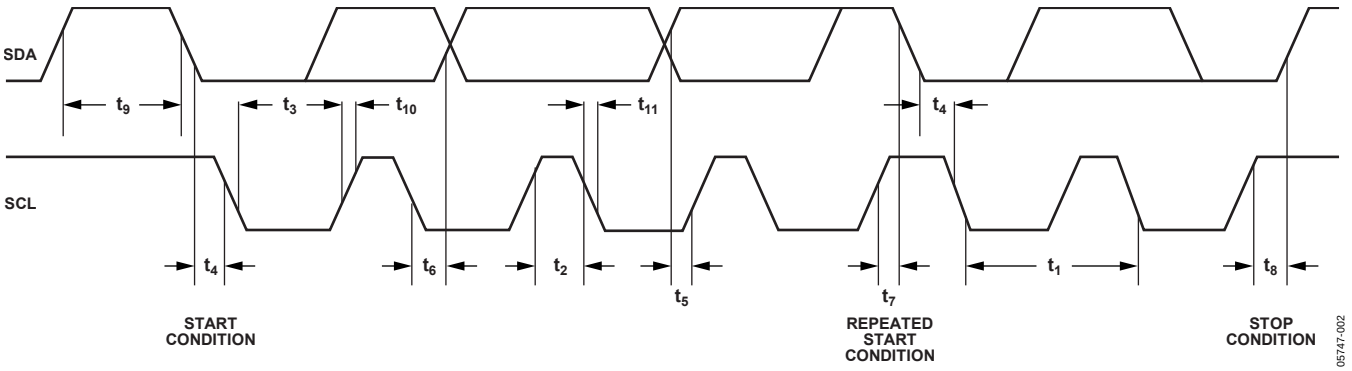


Figure 2. I²C-Compatible Serial Interface Timing Diagram

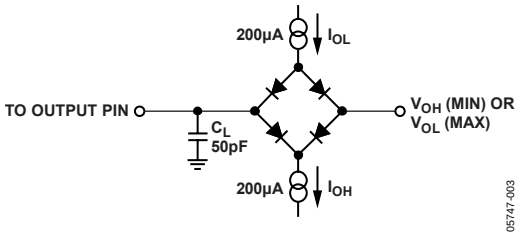


Figure 3. Load Circuit for Digital Output

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.[1]

Table 3.

Parameter	Rating
V_{PP} to AGND	−0.3 V to +70 V
AV_{DD} to AGND	−0.3 V to +7 V
V(+) to AGND	−0.3 V to +17 V
DV_{DD} to DGND	−0.3 V to +7 V
V_{DRIVE} to OPGND	−0.3 V to +7 V
Digital Inputs to OPGND	−0.3 V to DV_{DD} + 0.3 V
SDA/SCL to OPGND	−0.3 V to + 7 V
Digital Outputs to OPGND	−0.3 V to DV_{DD} + 0.3 V
RS(+)/RS(−) to V_{PP}	−0.3 V to V_{PP} + 0.3 V
REFIN to AGND	−0.3 V to AV_{DD} + 0.3 V
OPGND to AGND	−0.3 V to +0.3 V
OPGND to DGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
VOUTX to AGND	−0.3 V to DAC OUT V(+) + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	
B Version	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Max)	150°C
TQFP-64 Package	
θ_{JA} Thermal Impedance	54°C/W
θ_{JC} Thermal Impedance	16°C/W
LFCSP-56 Package	
θ_{JA} Thermal Impedance	30°C/W
θ_{JC} Thermal Impedance	2.9°C/W
ESD	1.5 kV HBM
Reflow Soldering Peak Temperature	230°C

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

To conform with IPC 2221 industrial standards, it is advisable to use conformal coating on the high voltage pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

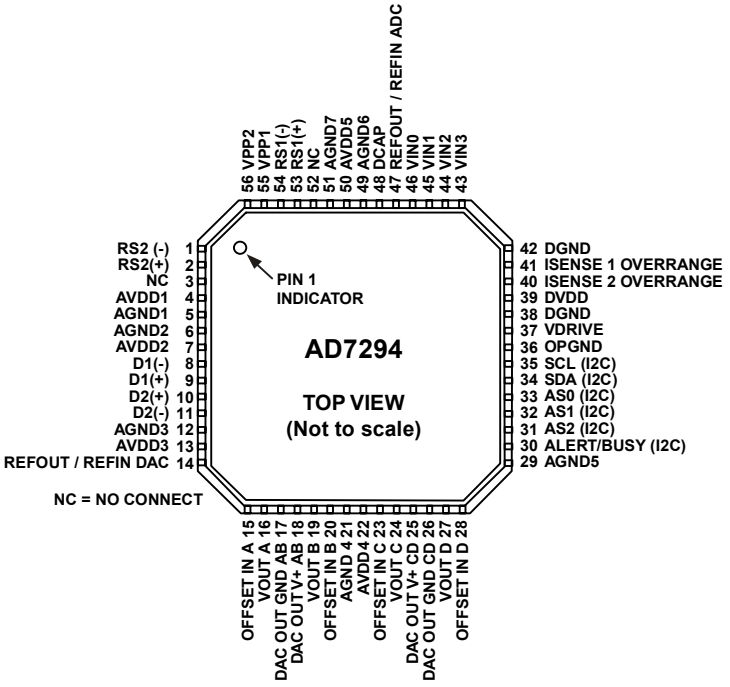


Figure 4. Pin Configuration, LFCSP Package

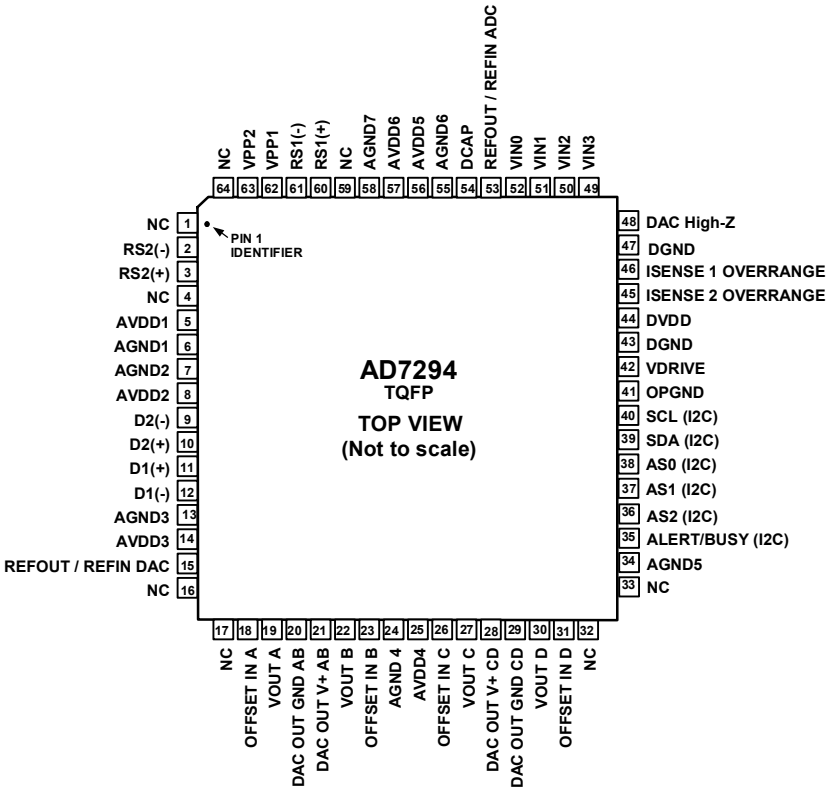


Figure 5. Pin Configuration, TQFP Package

Table 4. Pin Function Descriptions

LFCSP Pin No.	TQFP Pin No.	Mnemonic	Description
1, 54	2, 61	RS2(–), RS1(–)	Low-Side Connection for External Sense Resistor.
2, 53	3, 60	RS2(+), RS1(+)	High-Side Connection for External Sense Resistor.
3, 52	1, 4, 16, 17, 32, 33, 59, 64	NC	No Connection. Do not connect these pins.
4, 7, 13, 22, 50	5, 8, 14, 25, 56	AVDD1 to AVDD5	Analog Supply Pins. Connect these pins to DVDD. Decouple these pins with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. The operating range is 4.5 V to 5.5 V.
5, 6, 12, 21, 29, 49, 51	6, 7 13, 24, 34, 55, 58	AGND1 to AGND7	Analog Ground Reference Point.Connect all AGND pins externally to the AGND plane. Note that AGND5 is a DAC ground reference point.
8, 11	9, 12	D2(–), D1(–)	Analog Input. These pins are connected to the cathodes of the external temperature sensing diodes.
9, 10	10, 11	D2(+), D1(+)	Analog Input. These pins are connected to the anodes of the external temperature sensing diodes.
14	15	REFOUT/REFIN DAC	The AD7294 contains a REFOUT/REFIN DAC pin common to all four DAC channels. The default for this pin is a reference input. If an application requires an internal reference, it is enabled by the control register. At least a 220 nF capacitor to ground is required for noise reasons.
15, 20, 23, 28	18, 23, 26, 31	OFFSET IN A to OFFSET IN D	These pins set the desired output range for each DAC channel. Input range is 0 V to 5 V. Place 100nF capacitor to ground on these if they are not being driven.
16, 19, 24, 27	19, 22, 27, 30	VOUT A to VOUT D	Buffered Analog Outputs for DAC Channel A to DAC Channel D. Each analog output is driven by an output amplifier that can be offset using the OFFSET INx pin. DACs deliver 12-bit resolution in a 5 V range, providing an output voltage from 0 V to 15 V. Each output is capable of sourcing and sinking 10 mA and driving a 1000 pF load.
17, 18	20, 21	DAC OUT GND AB, DAC OUT V+ AB	Analog Supply Pins for Output Amplifiers on VOUTA and VOUTB.
25, 26	28, 29	DAC OUT V+ CD, DAC OUT GND CD	Analog Supply Pins for Output Amplifiers on VOUTC and VOUTD.
30	35	ALERT/BUSY (I2C)	Digital Output. Selectable as an alert or busy output function in the configuration register. Alert. When configured as an alert, this pin acts as an out-of-range indicator and, if enabled, becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the Alert Status Registers section. Busy. When configured as a busy output, this pin becomes active when a conversion is in progress. Open-drain output. An external pull-up resistor is required.
33	38	AS0 (I2C)	Logic Input. The AS0 logic input selects unique addresses for the AD7294. The device address depends on the voltage applied to this pin.
32	37	AS1 (I2C)	Logic Input. The AS1 logic input selects unique addresses for the AD7294. The device address depends on the voltage applied to this pin.
31	36	AS2 (I2C)	Logic Input. The AS2 logic input selects unique addresses for the AD7294. The device address depends on the voltage applied to this pin.
34	39	SDA	Digital Input/Output. Serial bus bidirectional data. This open-drain output needs pull-up resistors.
35	40	SCL	Serial I^2C Bus Clock. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes. This open-drain output needs pull-up resistors.
36	41	OPGND	Dedicated Ground Pin for I^2C Interface.
37	42	VDRIVE	To set the input and output thresholds, connect this pin to the supply to which the I^2C bus is pulled. The guaranteed operating range is 2.7 V to 5.5 V.
38, 42	43, 47	DGND	Ground for All Digital Circuitry.
39	44	DVDD	Logic Power Supply. Connect to AVDD. It is recommended that these pins be decoupled with 0.1 µF ceramic and 10 µF tantalum capacitors to DGND.
40, 41	46, 45	$I_{SENSE}1$ Overrange, $I_{SENSE}2$ Overrange	Outputs from Fault Comparators. These pins are connected to the high-side current sense amplifiers.

LFCSP Pin No.	TQFP Pin No.	Mnemonic	Description
N/A	48	DAC High-Z	High Impedance Control on DAC Outputs. When set high, it sets the DAC outputs to the voltage on the offset pin.
43 to 46	49, 50, 51, 52	VIN3 to VIN0	Uncommitted Analog Inputs.
47	53	REFOUT/REFIN ADC	The AD7294 contains an REFOUT/REFIN ADC pin for the ADC. Default for this pin is a reference input. If an application requires an internal reference, it is enabled by the control register. At least a 220 nF capacitor to ground is required for noise reasons.
48	54	DCAP	External Decoupling Capacitor Input for Internal Temperature Sensor. Connect a 0.1 µF capacitor to AGND to this pin.
55, 56	62, 63	VPP1, VPP2	Analog Supply Pins. Power supply pins for the high-side current sense amplifiers. Operating range is from AVDD to 54 V. For RF applications, it is advisable to place a 10 Ω series resistor and a 100 nF capacitor to ground on the VPP high supply pin.

TERMINOLOGY

DAC TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. See

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD7294 because the output of the DAC cannot go below 0 V. Zero-code error is expressed in mV. See

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in mV.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percent of the full-scale range.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error, taking all the various errors into account. code.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus—from all 0s to all 1s and vice versa.

ADC TERMINOLOGY

Signal-to-Noise and Distortion Ratio (SINAD)
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise and distortion ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(*Noise* + *Distortion*) = (6.02 *N* + 1.76) dB

Thus, the SINAD is 74 dB for a 12-bit converter.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7294, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+V_5^{\,2}+V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Channel-to-Channel Isolation
A measure of the level of crosstalk between channels, taken by applying a full-scale sine wave signal to the unselected input channels, and determining how much the 108 Hz signal is attenuated in the selected channel. The sine wave signal applied to the unselected channels is then varied from 1 kHz up to 2 MHz, each time determining how much the 108 Hz signal in the selected channel is attenuated. This figure represents the worst-case level across all channels.

Power Supply Rejection Ratio (PSRR)
The ratio of the power in the ADC output at the full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC V_{DD} supply of Frequency f_S:

PSRR (dB) = 10 log(*Pf*/*Pf*$_S$)

where *Pf* is the power at frequency *f* in the ADC output; *Pf*$_S$ is the power at frequency f_S coupled onto the ADC V_{DD} supply.

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, AGND + 1 LSB.

Offset Error Match
The difference in offset error between any two channels.

Gain Error
The deviation of the last code transition (111…110) to (111…111) from the ideal (that is, REF_{IN} − 1 LSB) after the offset error has been adjusted out.

Gain Error Match
The difference in gain error between any two channels.

THEORY OF OPERATION

ADC OVERVIEW

The AD7294 consists of a successive approximation ADC based around a capacitive DAC. The analog input range for the part can be selected as a 0 V to V_{REF} input or a 2 × V_{REF} input, configured with either single-ended or differential analog inputs. The AD7294 has an on-chip 2.5 V reference that can be disabled when an external reference is preferred. If the internal reference is to be used elsewhere in a system, the output must be buffered first.

The various monitored and uncommitted input signals are multiplexed into the ADC. Four uncommitted analog input channels are multiplexed to the ADC, VIN0 to VIN3. These four channels allow single-ended, differential, and pseudo differential mode measurements of various system signals.

ADC TRANSFER FUNCTIONS

The designed code transitions occur at successive integer LSB values (1 LSB, 2 LSB, and so on). In single-ended mode, the LSB size is V_{REF}/4096 when the 0 V to V_{REF} range is used and 2 × V_{REF}/4096 when the 0 V to 2 × V_{REF} range is used.

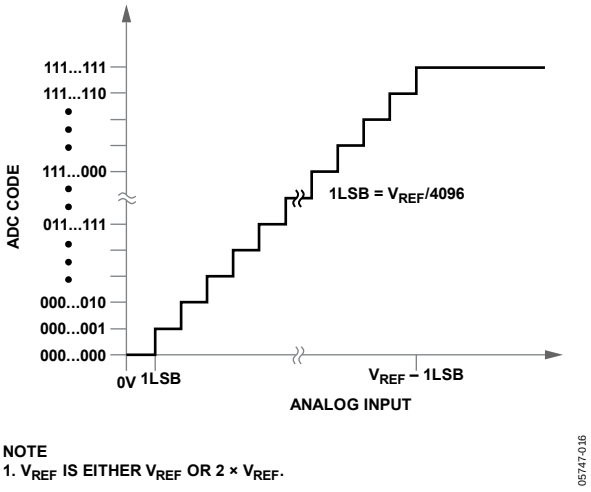


Figure 6. Single-Ended Transfer Characteristic

In differential mode, the LSB size is 2 × V_{REF}/4096 when the 0 V to V_{REF} range is used and 4 × V_{REF}/4096 when the 0 V to 2 × V_{REF} range is used. The ideal transfer characteristic for the ADC when outputting straight binary coding is shown in Figure 6, and the ideal transfer characteristic for the ADC when outputting twos complement coding is shown in Figure 7 (this is shown with the 2 × V_{REF} range).

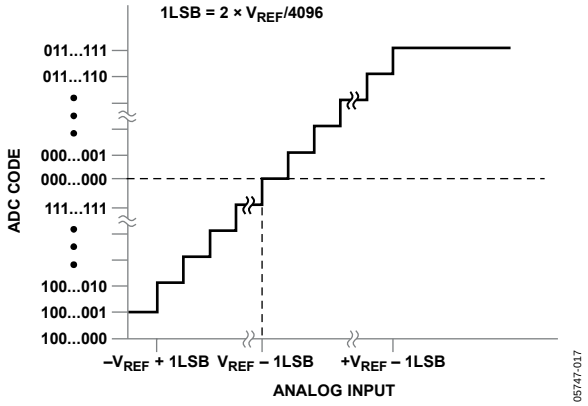


Figure 7. Differential Transfer Characteristic with V_{REF} ± V_{REF} Input Range

For Channel 1 to Channel4 in single-ended mode, the output code is straight binary, where 000 = 0 V, FFF = V_{REF}.

In differential mode, the code is twos complement, where 000 =0 V, 7FF = +V_{REF}, 800 = −V_{REF}, and FFF = 0 V − 1 LSB.

Channel 5 and Channel 6 are twos complement, where 000 = 0 mV, 7FF = +200 mV, 800 = −200 mV, and FFF = 0 V − 1 LSB.

Channel 7 to Channel 9 are twos complement with LSB = 0.25°C, where 000 = 0°C, 7FF = +255.75°C, 800 = −256°C, and FFF = −0.25°C.

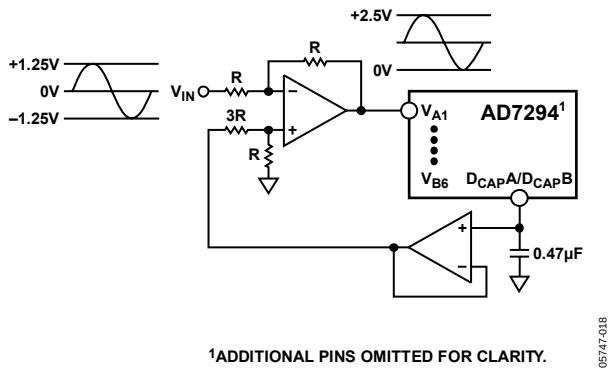
ANALOG INPUTS

The AD7294 has a total of four analog inputs. Depending on the configuration register setup, they can be configured as two single-ended inputs, two pseudo differential channels or two fully differential channels. See the Register Setting section for further details.

Single-Ended Mode

The AD7294 can have four single-ended analog input channels. In applications where the signal source has high impedance, it is recommended to buffer the analog input before applying it to the ADC. The analog input range can be programmed to be either 0 to V_{REF} or 0 to 2 × V_{REF}. In 2 × V_{REF} mode, the input is effectively divided by 2 before the conversion takes place, therefore, the input range becomes 0 to 2 × V_{REF}. Note that the voltage on the input channel pins with respect to GND cannot exceed VDD.

If the analog input signal to be sampled is bipolar, the internal reference of the ADC can be used to externally bias up this signal so that it is correctly formatted for the ADC. Figure 8 shows a typical connection diagram when operating the ADC in single-ended mode.

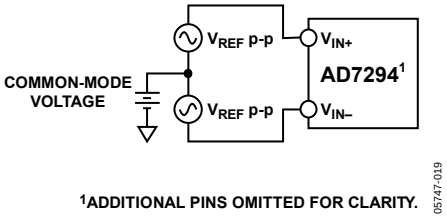


[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 8. Single-Ended Mode Connection Diagram

Differential Mode

The AD7294 can have two differential analog input pairs. Differential signals have some benefits over single-ended signals, including noise immunity based on the common-mode rejection of the device and improvements in distortion performance. Figure 9 defines the fully differential analog input of the AD7294.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 9. Differential Input Definition

The amplitude of the differential signal is the difference between the signals applied to the V_{IN+} and V_{IN-} pins in each differential pair ($V_{IN+} - V_{IN-}$). The resulting converted data is stored in twos complement format in the result register. Simultaneously drive V_{IN+} and V_{IN-} by two signals, each of amplitude V_{REF} (or $2 \times V_{REF}$, depending on the range chosen), that are 180° out of phase. Assuming the 0 to V_{REF} range is selected, the amplitude of the differential signal is, therefore, $-V_{REF}$ to $+V_{REF}$ peak-to-peak ($2 \times V_{REF}$), regardless of the common mode (VCM).

The common mode is the average of the two signals

$$(V_{IN+} + V_{IN-})/2$$

And is, therefore, the voltage on which the two inputs are centered.

This results in the span of each input being VCM ± $V_{REF}/2$. This voltage has to be set up externally, and its range varies with the reference value, V_{REF}. As the value of V_{REF} increases, the common-mode range decreases. When driving the inputs with an amplifier, the actual common-mode range is determined by the output voltage swing of the amplifier.

Figure 10 and Figure 11 show how the common-mode range typically varies with V_{REF} for a 5 V power supply using the 0 to V_{REF} range or $2 \times V_{REF}$ range, respectively. The common mode must be in this range to guarantee the functionality of the AD7294.

When a conversion takes place, the common mode is rejected, resulting in a virtually noise-free signal of amplitude $-V_{REF}$ to $+V_{REF}$, corresponding to the digital codes of 0 to 4095.

If the $2 \times V_{REF}$ range is used, the input signal amplitude extends from $-2\ V_{REF}$ ($V_{IN}0 = 0$ V, $V_{IN}1 = V_{REF}$) to $+2\ V_{REF}$ ($V_{IN}1 = 0$ V, $V_{IN}0 = V_{REF}$).

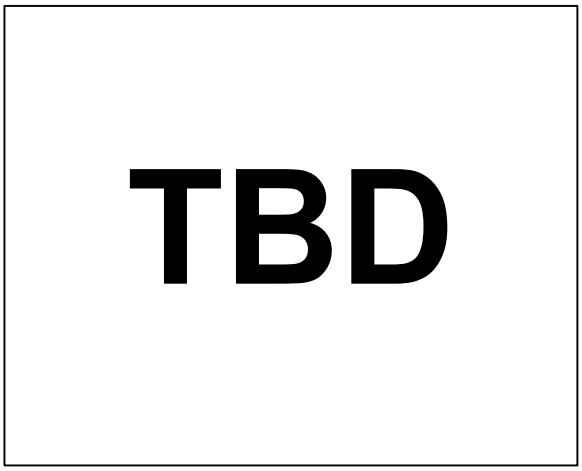


Figure 10. Input Common-Mode Range vs. V_{REF} (0 to V_{REF} Range, V_{DD} = 5 V)

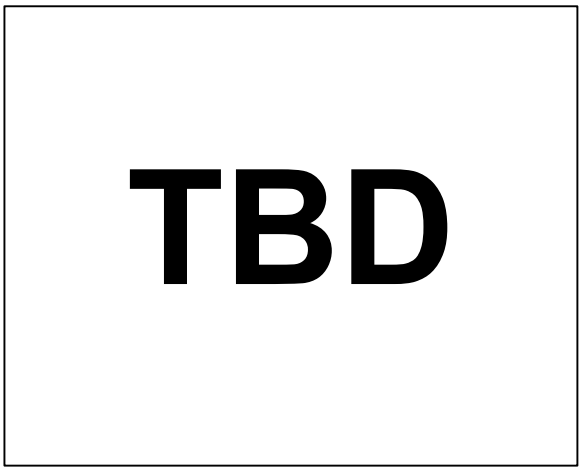


Figure 11. Input Common-Mode Range vs. V_{REF} ($2 \times V_{REF}$ Range, V_{DD} = 5 V)

Driving Differential Inputs

The differential modes available on Channel 1 to Channel 4 in Table 11 require that V_{IN+} and V_{IN-} be driven simultaneously with two equal signals that are 180° out of phase. The common mode must be set up externally. The common-mode range is determined by V_{REF}, the power supply, and the particular amplifier used to drive the analog inputs. Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion.

Using an Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7294. The circuit configurations illustrated in Figure 12 and Figure 13 show how a dual op amp can be used to convert a single-ended signal into a differential signal for both a bipolar and unipolar input signal, respectively.

The voltage applied to Point A sets up the common-mode voltage. In both diagrams, Point A is connected to the reference, but any value in the common-mode range can be input here to set up the common mode. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the AD7294.

Take care when choosing the op amp; the selection depends on the required power supply and system performance objectives. The driver circuits in Figure 12 and Figure 13 are optimized for dc coupling applications requiring best distortion performance. The circuit configuration shown in Figure 12 converts a unipolar, single-ended signal into a differential signal. The differential op amp driver circuit shown in Figure 13 is configured to convert and level shift a single-ended, ground referenced (bipolar) signal to a differential signal centered at the V_{REF} level of the ADC.

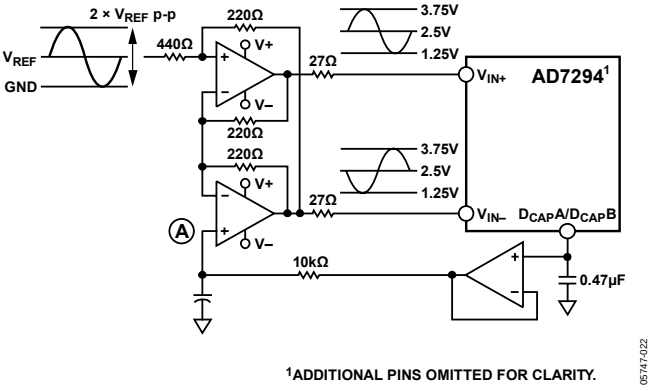


Figure 12. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal

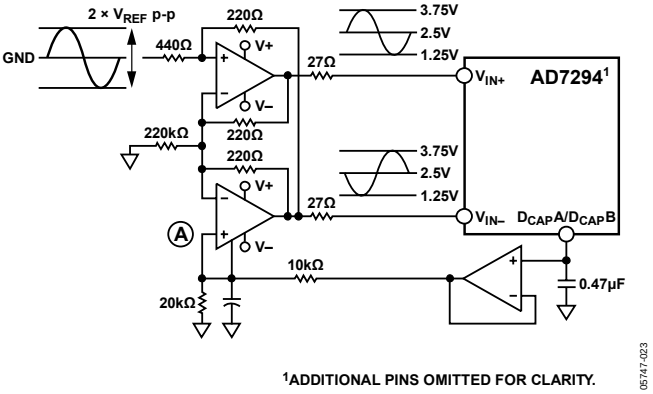


Figure 13. Dual Op Amp Circuit to Convert a Single-Ended Bipolar Signal into a Differential Unipolar Signal

Pseudo Differential Mode

The AD7294 can have two pseudo differential pairs. Uncommitted input Channel 1 and Channel 2 are a pseudo differential pair, as are Channel 3 and Channel 4. In this mode, V_{IN+} is connected to the signal source, which must have an amplitude of V_{REF} (or 2 × V_{REF}, depending on the range chosen) to make use of the full dynamic range of the part. A dc input is applied to the V_{IN-} pin. The voltage applied to this input provides an offset from ground or a pseudo ground for the V_{IN+} input. Which channel is VIN+ is determined by the ADC channel allocation. The differential mode must be selected to operate in the pseudo differential mode. The resulting converted pseudo differential data is stored in twos complement format in the result register.

The governing equation for the pseudo differential mode, for Channel 1 is

$$V_{OUT} = 2(V_{IN}0 - V_{IN}1) - V_{REF\_ADC}$$

where $V_{IN}0$ is the single-ended signal on Channel 1 and $V_{IN}1$ is the single-ended signal on Channel 2.

The benefit of pseudo differential inputs is that they separate the analog input signal ground from the ADC ground, allowing dc common-mode voltages to be cancelled. The typical voltage range for the V_{IN-} pin while in pseudo differential mode is shown in Figure 14 and Figure 15. Figure 16 shows a connection diagram for pseudo differential mode.

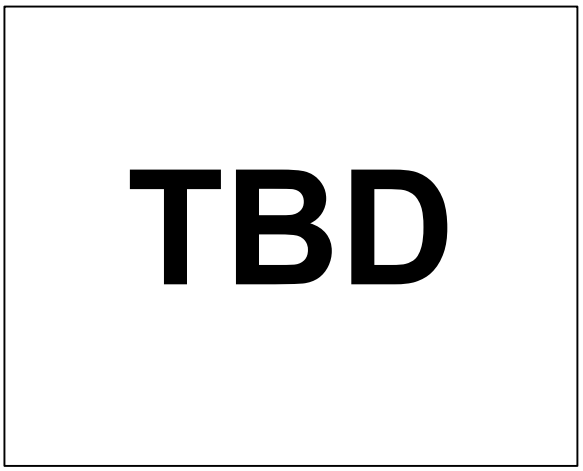


Figure 14. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 3 V

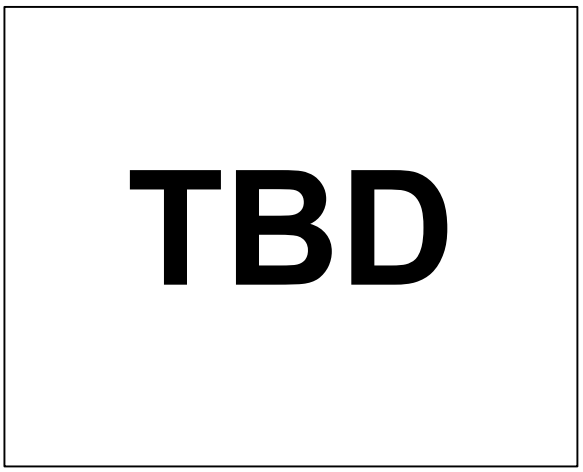


Figure 15. V_{IN-} Input Voltage Range vs. V_{REF} in Pseudo Differential Mode with V_{DD} = 5 V

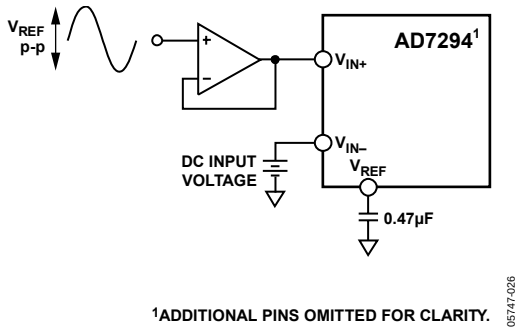


Figure 16. Pseudo Differential Mode Connection Diagram

CURRENT SENSOR

Two bidirectional high-side current sense amplifiers are provided, which can accurately amplify small differential current shunt voltages in the presence of large common-mode voltages (from AVDD up to +59.4V). Each amplifier has a gain of 12.5, giving a ±200 mV differential input range with a 2.5 V reference.

An analog comparator is also provided with each amplifier for fault detection. The threshold is defined as 1.2 × full scale, and once this limit is reached the output is latched onto a dedicated pin. This output remains high until the latch is cleared by writing to the appropriate register.

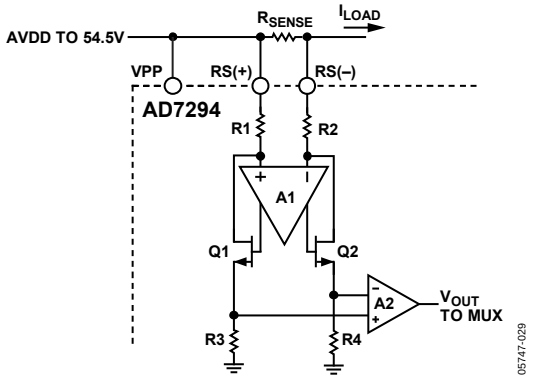


Figure 17. High-Side Current Sense

The AD7294 current sense is comprised of two main blocks, a differential and an instrumentation amplifier. A load current flowing through the external shunt resistor produces a voltage at the input terminals of the AD7294. Resistors R1 and R2 connect the input terminals to the differential amplifier (A1). A1 nulls the voltage appearing across its own input terminals by adjusting the current through R1 and R2 with Transistor Q1 and Transistor Q2. Common-mode feedback maintains the sum of these currents at approximately 50 µA. When the input signal to the AD7294 is zero, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal.

The differential currents through Q1 and Q2 are converted into a differential voltage by R3 and R4. A2 is configured as an instrumentation amplifier, buffering this voltage and providing additional gain. Hence, for an input voltage of ± 200 mV at the pins, an output span of ± 2.5 V is generated.

To remove any offsets that may be present, switches at the input pins allow the inputs to be reversed. When a current sense reading is requested, two ADC readings are taken, 6 µs apart, one for each switch position. Any offset voltage is then digitally removed before the final result is returned.

Choosing R_{SENSE}

An example calculation follows:

The AD7294 current sense has a specified full-scale sense range of 200 mV. With a VPP of 48 V and a R_{LOAD} of 50 Ω, the I_{LOAD} is

$$I_{LOAD} = VPP/R_{LOAD} = 48\ V/50\ \Omega = 0.96\ A$$

With a full-scale sense range of 200 mV, sense resistor value is

$$R_{SENSE} = FSV_{SENSE}/I_{LOAD} = 200\ mV/0.96\ A = 208.3\ m\Omega$$

In applications monitoring very high currents, R_{SENSE} must be able to dissipate the I^2R losses. If the rated power dissipation of the resistor is exceeded, its value may drift or it may fail altogether, causing a differential voltage across the terminals in excess of the absolute maximum ratings. If I_{SENSE} has a large high frequency component, take care to choose a resistor with low inductance. Wire-wound resistors have the highest inductance, metal film resistors are somewhat better, and low inductance metal film resistors are best suited for these applications.

Current Sense Filtering

In some applications, it may be desirable to use external filtering to reduce the input bandwidth of the amplifier, see Figure 18. The −3dB differential bandwidth of this filter is equal to

$$BW_{DM} = 1/(4\pi RC)$$

Note that the maximum series resistance on the RS(+) and RS(−) (as shown in Figure 17) inputs is limited to a maximum of 1 kΩ because it effects the gain of R1 and R2.

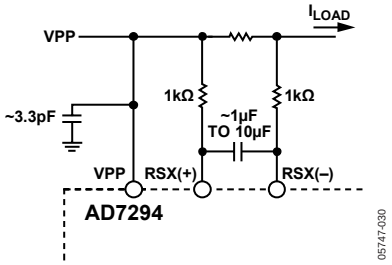


Figure 18. Current Sense Filtering

Kelvin Sense Resistor Connection

When using a low value sense resistor for high current measurement, the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length. Avoid this problem by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 19 shows the correct way to connect the sense resistor between the RS+ and RS− pins of the AD7294.

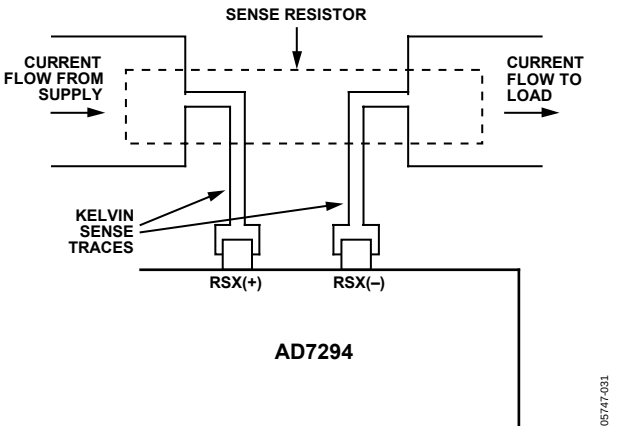


Figure 19. Kelvin Sense Connections

ANALOG COMPARATOR LOOP

The AD7294 consists of two setpoint comparators that are used for independent analog control. The advantage of using analog control for current sensing is the dynamic speed of the analog loop vs. the speed of the digital loop, in that the analog control loop does not have the digital delays inherent in ADC-to-DAC signal processing. The I_{SENSE}OVERRANGE pins signal whether the instrumentation amplifiers voltage from the current sense is greater then or less then the set point: [ADC V_{REF}/10.41] mV. This setpoint is the fixed threshold voltage of the overrange comparator and the current sense amplifier saturates above this. An alert also triggers if a voltage of less then V_{DD} is applied to the R_{SENSE} pins.

TEMPERATURE SENSOR

The AD7294 consists of one local and two remote temperature sensors. The analog input multiplexer can alternately select either the on-chip, band gap, temperature sensor to measure the temperature of the system, or one of the two remote diode temperature sensors.

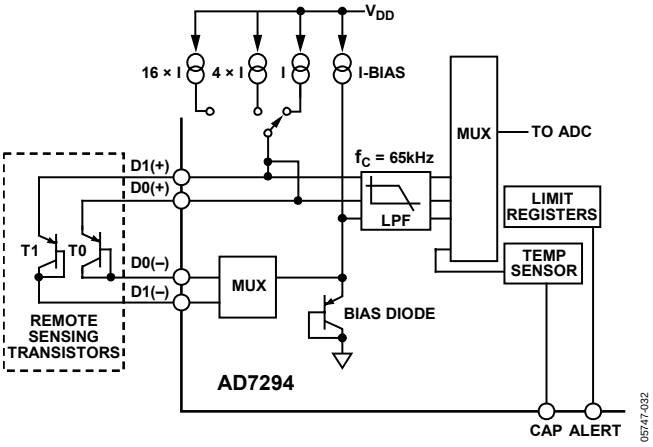


Figure 20. Internal and Remote Temperature Sensors

The temperature sensor module on the AD7294 is based on the three-current principle, see Figure 20, where three currents are passed through a diode and the forward voltage drop is measured at each diode, allowing the temperature to be calculated free of errors caused by series resistance.

Each input integrates, in turn, over a period of several hundred microseconds. This takes place continuously in the background, leaving the user free to perform conversions on the other channels. When integration is complete, a signal is passed to the control logic to automatically initiate a conversion. If the ADC is in command mode, the temperature conversion is performed as soon as the next conversion is completed. In autocycle mode, the conversion is inserted into an appropriate place in the current sequence; see the Register Setting section for further details. If the ADC is idle, the conversion takes place immediately.

Three registers store the result of the last conversion on each temperature channel; these can be read at any time. In addition, in command mode, one or both of the two external channel registers can be read out as part of the output sequence.

Remote Sensing Diode

The AD7294 is designed to work with discrete transistors, 2N3904 and 2N3906. If an alternative transistor is used, take the following factors into consideration to reduce measurement error:

Ideality Factor

The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The AD7294 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a Temperature T (°C), when using a transistor whose n_f does not equal 1.008. See the processor data sheet for the n_f values.

$$\Delta T = (n_f - 1.008) \times (273.15\ \text{K} + T)$$

To factor this in, the user can write the ΔT value to the offset register. The AD7294 automatically adds it to, or subtracts it from, the temperature measurement.

Base Emitter Voltage Factors

A base-emitter voltage greater than 0.25 V at 8 μA, at the highest operating temperature or a base-emitter voltage less than 0.95 V at 128 μA, at the lowest operating temperature.

Base Resistance Factor

A base resistance less than 100 Ω.

h_{FE} Variation Factor

Small variation in h_{FE} (approximately 50 to 150) that indicates tight control of V_{BE} characteristics.

It is suggested to use high Q capacitors to protect the external measurements from RF noise. The capacitor should be connected between the base and the emitter, as close to the external device as possible. For example, a Johanson 100 pF high Q capacitor: Reference Code 500R07S100JV45.

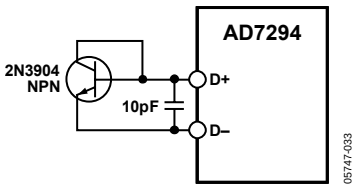


Figure 21. Measuring Temperature Using an NPN Transistor

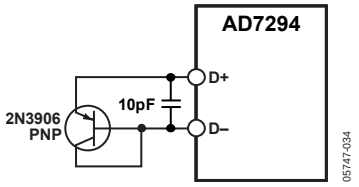


Figure 22. Measuring Temperature Using a PNP Transistor

Series Resistance Cancellation

Parasitic resistance to the D+ and D– inputs to the AD7294, seen in series with the remote diode, is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the temperature measurement of the remote sensor. This error typically causes a 0.5°C offset per ohm of parasitic resistance in series with the remote diode.

The AD7294 automatically cancels out the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The AD7294 is designed to automatically cancel typically up to 3 kΩ of resistance. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and D– pin to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF.

This capacitor reduces the noise, but does not eliminate it. Sometimes, this sensor noise is a problem in a very noisy environment. In most cases, a capacitor is not required as differential inputs, by their very nature, have a high immunity to noise. In certain cases where RF noise may be an issue it is advised to place a 10 pF to 100 pF capacitor as close as possible to the diode between the base and the emitter, such as the Johanson capacitor.

DAC OPERATION

The AD7294 contains four 12-bit DACs that provide digital control with 1.2 mV resolution to control the bias currents of the power transistors. They can also be used to provide control voltages for variable gain amplifiers or impedance match networks in the main signal chain. The DAC core is a thin film 12-bit string DAC with a 5 V internal buffer to drive the high voltage output stage. The DAC has a span of 0 V to 5 V with a 2.5 V reference input. The output range of the DAC, which is controlled by the offset input, can be positioned from 0 V to 15 V. Figure 23 is a block diagram of the DAC architecture.

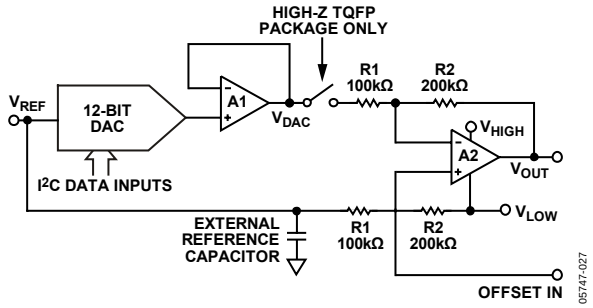


Figure 23. DAC Architecture

To improve functionality of the device, the DAC output is digitally inverted. V* in the equations below is the output of the DAC before digital inversion. Therefore, although the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{DAC} = V_{REF} - V_{DAC}^{*}$$

$$\text{and } V_{DAC}^{*} = \left[V_{REF} \times \left(\frac{D}{2^{n}} \right) \right]$$

where *D* is the decimal equivalent of the binary code that is loaded to the DAC register, and *n* is the bit resolution of the DAC.

Table 5. DAC Output Code Table

Digital Input	Analog Output (V)
0000 0000 0000	$V_{REF} - V_{REF}$ (0/4096) = V_{REF}
0000 0000 0001	$V_{REF} - V_{REF}$ (1/4096)
1000 0000 0000	$V_{REF} - V_{REF}$ (2048/4096) = $V_{REF}/2$
1111 1111 1111	$V_{REF} - V_{REF}$ (4095/4096)

Resistor String

The resistor string structure is shown in Figure 24. It is simply a string of 2^n resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture is inherently monotonic, voltage out, and low glitch. It is also linear because all of the resistors are of equal value.

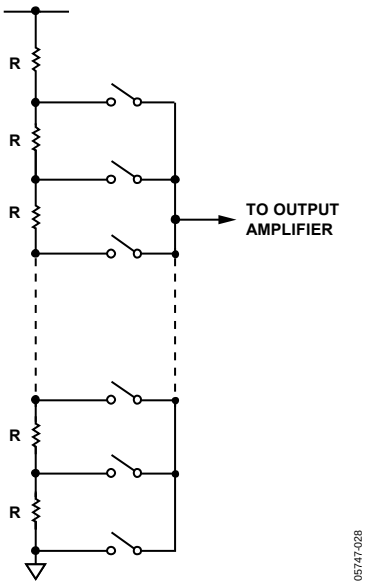


Figure 24. Resistor String Structure

Output Amplifier

Referring to Figure 23, the purpose of A1 is to buffer the DAC output range from 0 V to V_{REF}. The second amplifier, A2, is configured such that when an offset is applied to OFFSET IN, its output voltage is three times the offset voltage minus twice the DAC voltage.

$$V_{OUT} = 3V_{OFFSET} - 2V_{DAC}$$

The DAC word is digitally inverted on-chip such that

$$V_{OUT} = 3V_{OFFSET} + 2(V_{DAC}^{*} - V_{REF})$$

An example of the offset function is given in Table 6

Table 6. Offset Voltage Function Example

Offset Voltage	VOUT with 0x000	VOUT with 0xFFF
1.67 V	0 V	5 V – 1 LSB
3.33 V	5 V	10 V – 1 LSB
5.00 V	10 V	15 V – 1 LSB

The user has the option of leaving the offset pin open, in which case the voltage on the noninverting input of Op Amp A2 is set by the resistor divider, giving

$$V_{OUT} = 2V_{DAC}$$

This generates the 5 V output span from a 2.5 V reference. Digitally inverting the DAC allows the circuit to operate as a generic DAC when no offset is applied. If the offset pin is not being driven it is adviced placing a 100nF capacitor between the pin and ground to improve settling time of dac and the noise performance.

Note that a significant amount of power can be dissipated in the DAC outputs. In this regard, the LFCSP has superior thermal characteristics. A thermal shutdown circuit sets the DAC outputs to high impedance if a die temperature of >150°C is measured by the internal temperature sensor. Note that this feature is disabled if the temperature sensor is powered down.

High Impedance Pin (In TQFP package only)

When the high impedance pin (High-Z pin) is toggled high, see Figure 23, the offset pin voltage appears on the DAC output voltage pin. Essentially the internal amplifier, A2, acts as a voltage follower. This feature allows a fast change in the output when a fault occurs.

REFERENCE FOR ADC/DAC

Both internal references on the AD7294 are well regulated, low ppm 2.5 V reference with low drift voltage and a stable output. If the application requires an external reference, it can be applied to the REFOUT/REFIN DAC pin and/or to the REFOUT/REFIN ADC pin. If the reference is driving external nodes, a buffer is required to achieve a low impedance output. For noise reasons, the reference buffers each require at least 220 nF on the output pin when no external reference is being applied. Note that on power up, the ADC and DAC reference buffers switch off by default; note the power-down register for further power down information, in the Register Setting section.

When using an external reference to achieve the desired performance from the AD7294, give thought to the choice of a precision voltage reference. There are four possible sources of error to considerwhen choosing a voltage reference for high accuracy applications: initial accuracy, ppm drift, long-term drift, and output voltage noise. To minimize these errors, a reference with high initial accuracy is preferred. In addition, choosing a reference with an output trim adjustment, such as the ADR441, allows a system designer to trim system errors by setting a reference voltage to a voltage other than the nominal.

Long-term drift is a measure of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains stable during its entire lifetime. If choosing an external reference, consider a tight temperature coefficient specification to reduce the temperature dependence of the system output voltage on ambient conditions.

V_{DRIVE}

The AD7294 also has a V_{DRIVE} feature to control the voltage at which the I^2C interface operates. Because the I^2C pins are open-drain, there is not a corresponding V_{DD} pin. Connect the V_{DRIVE} pin to the supply that the I^2C bus is pulled up to. This is not a supply pin; it merely sets up the input and output threshold levels. V_{DRIVE} allows the ADC to easily interface to both 3 V and 5 V processors. For example, if the AD7294 is operated with a V_{DD} of 5 V, the V_{DRIVE} pin can be powered from a 3 V supply, allowing a large dynamic range with low voltage digital processors. Thus, the AD7294 can be used with the 2 × V_{REF} input range with a V_{DD} of 5 V while still being able to interface to 3 V digital parts.

REGISTER SETTING

The AD7294 contains internal registers (see Figure 25) that are used to store conversion results, high and low conversion limits, and information to configure and control the device.

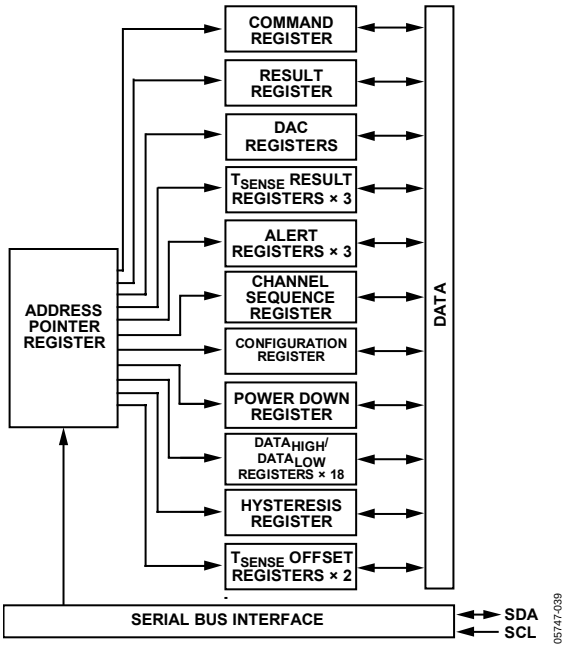


Figure 25. AD7294 Register Structure

Each data register has an address to which the address pointer register points when communicating with it. The command register is the only register that is a write-only register; the rest are read/write registers.

ADDRESS POINTER REGISTER

The address pointer register is an 8-bit register, in which the 6 LSBs are used as pointer bits to store an address that points to one of the AD7294 data registers, see Table 7.

Table 7. AD7294 Register Address

Address in Hex	Registers
00	Command Register (W)
01	Result Register (R)/DAC1 Value (W)
02	$T_{SENSE}1$ Result (R)/DAC2 Value (W)
03	$T_{SENSE}2$ Result (R)/DAC3 Value (W)
04	$T_{SENSE}INT$ Result (R)/DAC4 Value (W)
05	Alert Register A (R/W)
06	Alert Register B (R/W)
07	Alert Register C (R/W)
08	Channel Sequence Register (R/W)
09	Configuration Register (R/W)
0A	Power-Down Register (R/W)
0B	$DATA_{LOW}$ Register $V_{IN}0$ (R/W)
0C	$DATA_{HIGH}$ Register $V_{IN}0$ (R/W)
0D	Hysteresis Register $V_{IN}0$ (R/W)
0E	$DATA_{LOW}$ Register $V_{IN}1$ (R/W)
0F	$DATA_{HIGH}$ Register $V_{IN}1$ (R/W)
10	Hysteresis Register $V_{IN}1$ (R/W)
11	$DATA_{LOW}$ Register, $V_{IN}2$ (R/W)
12	$DATA_{HIGH}$ Register $V_{IN}2$ (R/W)
13	Hysteresis Register $V_{IN}2$ (R/W)
14	$DATA_{LOW}$ Register $V_{IN}3$ (R/W)
15	$DATA_{HIGH}$ Register $V_{IN}3$ (R/W)
16	Hysteresis Register $V_{IN}3$ (R/W)
17	$DATA_{LOW}$ Register $I_{SENSE}1$ (R/W)
18	$DATA_{HIGH}$ Register $I_{SENSE}1$ (R/W)
19	Hysteresis Register $I_{SENSE}1$ (R/W)
1A	$DATA_{LOW}$ Register $I_{SENSE}2$ (R/W)
1B	$DATA_{HIGH}$ Register $I_{SENSE}2$ (R/W)
1C	Hysteresis Register $I_{SENSE}2$ (R/W)
1D	$DATA_{LOW}$ Register $T_{SENSE}1$ (R/W)
1E	$DATA_{HIGH}$ Register $T_{SENSE}1$ (R/W)
1F	Hysteresis Register $T_{SENSE}1$ (R/W)
20	$DATA_{LOW}$ Register $T_{SENSE}2$ (R/W)
21	$DATA_{HIGH}$ Register $T_{SENSE}2$ (R/W)
22	Hysteresis Register $T_{SENSE}2$ (R/W)
23	$DATA_{LOW}$ Register $T_{SENSE}INT$ (R/W)
24	$DATA_{HIGH}$ Register $T_{SENSE}INT$ (R/W)
25	Hysteresis Register $T_{SENSE}INT$ (R/W)
26	$T_{SENSE}1$ Offset Register (R/W)
27	$T_{SENSE}2$ Offset Register (R/W)
40	Factory Test Mode
41	Factory Test Mode

COMMAND REGISTER (0x00)

Writing in the command register puts the part into command mode. When in command mode, the part cycles through the selected channels on each subsequent read. If the external T_{SENSE} channels are selected in the command word, it is not actually requesting a conversion, but the result of the last automatic conversion is output in sequence. See Channel Sequence Register (0X08), where the brackets denote differential or pseudo differential mode.

RESULT REGISTER (0x01)

The result register is a 16-bit read register. The four uncommitted input channels and the two I_{SENSE} channels converted results are stored in the result register for reading. The register consists of bits D14 to D12 to identify the ADC channel allocation. Bits D11 to D0, in the result register, are the data bits sent to DAC1. While the MSB, D15, is reserved as an Alert_Flag bit. Table 9 shows the contents of the first byte to read from the AD7294; Table 10 shows the contents of the second byte read.

Table 8. Command Register

	MSB							LSB
Bits	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Channel	Read out last result from $T_{SENSE}2$	Read out last result from $T_{SENSE}1$	$I_{SENSE}2$	$I_{SENSE}1$	$V_{IN}3$ or ($V_{IN}3 - V_{IN}2$)	$V_{IN}2$ or ($V_{IN}2 - V_{IN}3$)	$V_{IN}1$ or ($V_{IN}1 - V_{IN}0$)	$V_{IN}0$ or ($V_{IN}0 - V_{IN}1$)

Table 9. Result Register (First Read)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Alert_Flag	CH_{ID2}	CH_{ID1}	CH_{ID0}	B11	B10	B9	B8

Table 10. Result Register (Second Read)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

ADC Channel Allocation

These nine channel address bits select which analog input channel is to convert using the multiplexer, see Table 11. Choosing Channel 1 to Channel 4 selects the standard analog voltage inputs. Channel 5 and Channel 6 represent the analog input sense amplifiers for current monitoring. Channel 7 and Channel 8 designate the use of the external temperature sensing diodes, whereas Channel 9 represents the internal temperature sensor.

Table 11. ADC Channel Allocation

Function	Channel ID
$V_{IN}0$ or ($V_{IN}0 - V_{IN}1$)	000
$V_{IN}1$ or ($V_{IN}1 - V_{IN}0$)	001
$V_{IN}2$ or ($V_{IN}2 - V_{IN}3$)	010
$V_{IN}3$ or ($V_{IN}3 - V_{IN}2$)	011
$I_{SENSE}1$	100
$I_{SENSE}2$	101
$T_{SENSE}1$	110
$T_{SENSE}2$	111
$T_{SENSE}INT$	N/A

There are two modes of operation with respect to the ADC. In command mode, a sequence is written to the ADC and on subsequent reads, the next channel in the sequence is converted as the current sequence is read out. In autocycle mode, a sequence is programmed and then the ADC automatically cycles through the selected channels, outputting an alert if one of the channels goes outside its preset range.

DAC1 REGISTER (0x01)

Writing to this register address sets the DAC1 output code. Bits[D11:D0] in the result register are the data bits sent to DAC1. Bits[D14:D12] are ignored. The MSB, D15, is reserved as an Alert_Flag bit.

Table 12. DAC Register (First Write)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
x	x	x	x	B11	B10	B9	B8

Table 13. DAC Register (Second Write)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

$T_{SENSE}1$, $T_{SENSE}2$ RESULT REGISTERS (0x02 AND 0x03)

Register $T_{SENSE}1$ and Register $T_{SENSE}2$ are 16-bit read/write registers. General alert is flagged by the MSB, D15. Bits[D14:D12] are reserved for the ADC channel allocation. D11 is reserved for flagging diode open circuits. The temperature reading from the ADC is stored in a 10-bit twos complement format plus a sign bit, D10 to D0, see Table 14 and Table 15.

Table 14. T_{SENSE} Register (First Read)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Alert_Flag	CH_{ID2}	CH_{ID1}	CH_{ID0}	B11	B10	B9	B8

Table 15. Register (Second Read)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

DAC2 AND DAC3 REGISTERS (0x02 AND 0x03)

Writing to these register addresses sets the DAC2 and DAC3 output codes. Bits[D11:D0], in the register, are the data bits sent to DAC2 and DAC3. Bits[D14:D12] are ignored. The MSB, D15, is reserved as an Alert_Flag bit.

Table 16. DAC2 and DAC3 Register (First Write)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
x	x	x	x	B11	B10	B9	B8

Table 17. DAC2 and DAC3 Register (Second Write)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

T_{SENSE}INT RESULT REGISTER (0x04)

The T_{SENSE}INT register is a 16-bit read/write register used to store the ADC data generated from the internal temperature sensor. Similar to the $T_{SENSE}1$ and $T_{SENSE}2$ result registers, this register stores the temperature readings from the ADC in a 10-bit twos complement format and in a sign bit format, D10 to D0, and uses the MSB as a general alert flag. However, Bits D14 to D11 are not used. Conversions take place approximately every 5 ms. The temperature data format in Table 18 also applies to the internal temperature sensor data.

Temperature Value Format

The temperature reading from the ADC is stored in a 11-bit twos complement format including a sign bit, D10 to D0, to accommodate both positive and negative temperature measurements. The temperature data format is shown in Table 18, which shows the achievable temperature measurement range. The ADC can theoretically measure a 512°C temperature span, ranging from −256°C to +255.75°C with an LSB of 0.25°C.

Table 18. T_{SENSE} Data Format

	MSB										LSB
Input	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Value (°C)	−256	+128	+64	+32	+16	+8	+4	+2	+1	+0.5	+0.25

DAC4 REGISTER (0x04)

Writing to this register address sets the DAC4 output code. Bits[D11:D0] in the result register are the data bits sent to DAC4. Bits[D14:D12] are ignored and the MSB, D15, is reserved as an Alert_Flag bit.

Table 19. DAC4 Register (First Write)

MSB							LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
x	x	x	x	B11	B10	B9	B8

Table 20. DAC4 Register (Second Write)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

ALERT STATUS REGISTER A (0x05), REGISTER B (0x06), AND REGISTER C (0x07)

The alert status registers (A, B and C) are 8-bit read/write registers that provide information on an alert event. If a conversion results in activating the ALERT pin or the Alert_Flag bit in the result register or T_{SENSE} registers, the alert status register can be read to gain further information.

CHANNEL SEQUENCE REGISTER (0x08)

The channel sequence register is an 8-bit read/write register that allows the user to sequence the ADC conversions in autocycle mode. See the Alerts and Limits Theory section for more information.

CONFIGURATION REGISTER (0x09)

The configuration register is a 16-bit read/write register that sets the operating modes of the AD7294. The bit functions of the configuration register are outlined in

Table 25 and Table 26.

Sample Delay and Bit Trial Delay

It is recommended that no I^2C Bus activity occur when a conversion is taking place; however, this may not be possible, for example when operating in automatic cycle mode. To maintain the performance of the ADC in such cases, Bit D14 and Bit D13 in the configuration register are used to delay critical sample intervals and bit trials from occurring while there is activity on the I^2C bus. This may increase the conversion time. When Bit D14 and Bit D13 are both 1, the bit trial-and-sample interval delaying mechanism are implemented. The default setting of D14 and D13 is 0. If bit trial delays extend longer than 1 µs, the conversion terminates. When D14 is 1, the sampling instant delay is implemented. When D13 is 1, the bit trial delay is implemented. To turn off both the sample delay and bit trial delay, set D14 and D13 to 0.

Table 21. Alert Status Register A

Alert Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	$V_{IN}3$ high alert	$V_{IN}3$ low alert	$V_{IN}2$ high alert	$V_{IN}2$ low alert	$V_{IN}1$ high alert	$V_{IN}1$ low alert	$V_{IN}0$ high alert	$V_{IN}0$ low alert

Table 22. Alert Status Register B

Alert Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	Reserved	Reserved	$I_{SENSE}2$ over-range	$I_{SENSE}1$ over-range	$I_{SENSE}2$ high alert	$I_{SENSE}2$ low alert	$I_{SENSE}1$ high alert	$I_{SENSE}1$ low alert

Table 23. Alert Status Register C

Alert Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	Open-diode flag	Over-temp alert	T_{SENSE}INT high alert	T_{SENSE}INT low alert	$T_{SENSE}2$ high alert	$T_{SENSE}2$ low alert	$T_{SENSE}1$ high alert	$T_{SENSE}1$ low alert

Table 24. Channel Sequence Register

Channel Bit	D7	D6	D5	D4	D3	D2	D1	D0
Function	Reserved	Reserved	$I_{SENSE}2$	$I_{SENSE}1$	$V_{IN}3$	$V_{IN}3$	$V_{IN}1$	$V_{IN}0$

Table 25. Configuration Register Bit Function Description D15 to D8

Channel Bit	D15	D14	D13	D12	D11	D10	D9	D8
Function	Reserved	Enable noise-delayed sampling. Use to delay critical sample intervals from occurring when there is when there is activity on the I²C bus.	Enable noise-delayed bit trials. Use to delay critical bit trials from occurring when there is activity on the I²C bus.	Enable autocycle mode	Enable pseudo differential mode for $V_{IN}3/V_{IN}4$	Enable pseudo differential mode for $V_{IN}1/V_{IN}2$	Enable differential mode for $V_{IN}3/V_{IN}4$	Enable differential mode for $V_{IN}1/V_{IN}2$

Table 26. Configuration Register Bit Function Description D7 to D0

Channel Bit	D15	D14	D13	D12	D11	D10	D9	D8
Function	Enable $2V_{REF}$ range on $V_{IN}4$	Enable $2V_{REF}$ range on $V_{IN}3$	Enable $2V_{REF}$ range on $V_{IN}2$	Enable $2V_{REF}$ range on $V_{IN}1$	Enable I²C filters	Enable alert pin	Enable busy pin (D2 = 0), clear alerts (D2 = 1)	Sets polarity of alert pin (active high/active low)

Table 27. ALERT/BUSY Function

D2	D1	ALERT/BUSY Pin Configuration
0	0	Pin does not provide any interrupt signal.
0	1	Configures pin as a busy output.
1	0	Configures pin as an alert output.
1	1	Resets the alert output pin, the Alert_Flag bit in the conversion result register, and the entire alert status register (if any is active). If 1,1 is written to Bits[D2:D1] in the configuration register to reset the ALERT pin, the Alert_Flag bit, and the alert status register, the contents of the configuration register read 1,0 for Bit D2 and Bit D1, respectively, if read back.

Table 28. ADC Input Mode Example

D11	D10	D9	D8	Description
0	0	0	0	All Channels Single Ended
0	0	0	1	Differential Mode on $V_{IN}1/V_{IN}2$
0	1	0	1	Pseudo Differential Mode on $V_{IN}1/V_{IN}2$

POWER-DOWN REGISTER (0x0A)

The power-down register is an 8-bit read/write register that is used to power down various sections on the AD7294 device. On power up, the default value for the power down register is 0x30.

Table 29. Power-Down Register Description

Bit	Function
D7	Power-down full chip
D6	Reserved
D5	Power-down ADC reference buffer (to allow external reference, 1 at power-up)
D4	Power-down DAC reference buffer (to allow external reference, 1 at power-up)
D3	Power-down temperature sensor
D2	Power-Down $I_{SENSE}2$
D1	Power-Down $I_{SENSE}1$
D0	DAC outputs set to high impedance (set automatically if die temperature >150°C)

$DATA_{HIGH}/DATA_{LOW}$ REGISTER (0x0B AND 0x0C FOR $V_{IN}0$)

The $DATA_{HIGH}$ and $DATA_{LOW}$ registers for a channel are 16-bit, read/write registers, see Table 31 and Table 32. General alert is flagged by the MSB, D15. D14 to D12 are not used in the register and are read as 0s. The remaining 12-bits set the high and low limits for the relevant channel. With respect to Channel 1 to Channel 4, for single-ended mode, 000 and FFF are the default values. For differential mode on Channel 1 to Channel 4 ($V_{IN}0$ to $V_{IN}3$), the default values for $DATA_{HIGH}$ and $DATA_{LOW}$ are 7FF and 800. Note that if the part is configured in single-ended mode and the limits are changed, the user must re-program limits when changing to a different mode.

Channel 5 and Channel 6 ($I_{SENSE}1$ and $I_{SENSE}2$) are twos complement format and so the default limits will also be 7FF and 800. There is no differential mode for Channel 5 and Channel 6.

Channel 7 to Channel 9 ($T_{SENSE}1$, $T_{SENSE}2$ and $T_{SENSE}INT$), default to 3FF and 400 for the $DATA_{HIGH}$ and $DATA_{LOW}$ limits as they are in twos complement 10-bit format. Differential mode is not available for Channel 7 to Channel 9.

Table 30. Default Values for $DATA_{HIGH}$ and $DATA_{LOW}$ Registers

ADC Channel	Single Ended	Differential
$V_{IN}0$	000 and FFF	7FF and 800
$V_{IN}1$	000 and FFF	7FF and 800
$V_{IN}2$	000 and FFF	7FF and 800
$V_{IN}3$	000 and FFF	7FF and 800
$I_{SENSE}1$	7FF and 800 (twos complement)	N/A
$I_{SENSE}2$	7FF and 800 (twos complement)	N/A
$T_{SENSE}1$	3FF and 400 (twos complement)	N/A
$T_{SENSE}2$	3FF and 400 (twos complement)	N/A
$T_{SENSE}INT$	3FF and 400 (twos complement)	N/A

Table 31. AD7294 $DATA_{HIGH/LOW}$ Register (First R/W)

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

Table 32. AD7294 $DATA_{HIGH/LOW}$ Register (Second R/W)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

HYSTERESIS REGISTERS (0x0D FOR $V_{IN}0$)

Each hysteresis register is a 16-bit read/write register; only the 12 LSBs of the register are used, with the MSB signaling the alert event. If FFF is written to the hysteresis register, it enters minimum/maximum mode, see the Alerts and Limits Theory section for further details.

Table 33. Hysteresis Register (First Read/Write)

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8
Alert_Flag	0	0	0	B11	B10	B9	B8

Table 34. Hysteresis Register (Second Read/Write)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

T_{SENSE} OFFSET REGISTERS (0x26 AND 0x27)

The AD7294 has temperature offset 8-bit twos complement registers for both Remote Channel $T_{SENSE}1$ and Remote Channel $T_{SENSE}2$. It allows the user to add or subtract an offset to the temperature.

The offset registers for $T_{SENSE}1$ and $T_{SENSE}2$ are 8-bit read/write registers that store data in a twos complement format. This data is subtracted from the temperature readings taken by $T_{SENSE}1$ and $T_{SENSE}2$ temperature sensors. The offset is carried out before the values are stored in the T_{SENSE} result register.

One reason for using the offset registers is that the T_{SENSE} registers are based on the 2N3906 transistor ideality factor. If a different external transistor is used for the external temperature measurements, there is a slightly different ideality factor, which creates a slight offset.

Table 35. T_{SENSE} Offset Data Format

	MSB							LSB
Input	D7	D6	D5	D4	D3	D2	D1	D0
Value (°C)	−32	+16	+8	+4	+2	+1	+0.5	+0.25

I²C INTERFACE

GENERAL I²C TIMING

Figure 26 shows the timing diagram for general read and write operations using an I²C-compliant interface.

The I²C bus uses open-drain drivers, therefore, when no device is driving the bus, both SCL and SDA are high. This is known as idle state. When the bus is idle, the master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The master device is responsible for generating the clock.

Data is sent over the serial bus in groups of nine bits—eight bits of data from the transmitter followed by an acknowledge bit (ACK) from the receiver. Data transitions on the SDA line must occur during the low period of the clock signal and remain stable during the high period. The receiver should pull the SDA line low during the acknowledge bit to signal that the preceding byte has been received correctly. If this is not the case, cancel the transaction.

The first byte that the master sends must consist of a 7-bit slave address, followed by a data direction bit. Each device on the bus has a unique slave address, therefore, the first byte sets up communication with a single slave device for the duration of the transaction.

The transaction can be used either to write to a slave device (data direction bit = 0), or to read data from it (data direction bit = 1). In the case of a read transaction, it is often necessary first to write to the slave device (in a separate write transaction) to tell it from which register to read. Reading and writing cannot be combined in one transaction.

When the transaction is complete, the master can keep control of the bus, initiating a new transaction by generating another start bit (high-to-low transition on SDA while SCL is high). This is known as a repeated start (Sr). Alternatively, the bus can be relinquished by releasing the SCL line followed by the SDA line. This low-to-high transition on SDA while SCL is high is known as a stop bit (P), and it leaves the I²C bus in its idle state (where no current is consumed).

The following example in Figure 26 shows a simple write transaction with an AD7294 as the slave device. In this example, the AD7294 register pointer is being set up ready for a future read transaction.

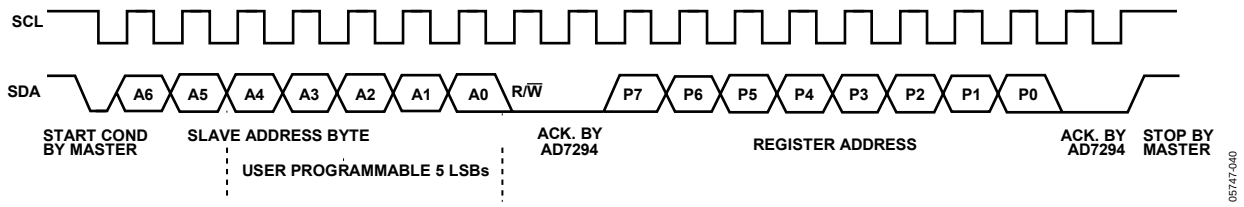


Figure 26. General I²C Timing

SERIAL BUS ADDRESS BYTE

The first byte the user writes to the device is the slave address byte. Similar to all I^2C-compatible devices, the AD7294 has a 7-bit serial address. The 5 LSBs are user programmable by the 3 three-state input pins as shown in

Table 36.

Table 36, H means tie the pin to VDRIVE, L means tie the pin to GND, and NC refers to a pin left floating. Note that in this final case, the stray capacitance on the pin must be less than 30 pF to allow correct detection of the floating state; therefore, any PCB trace must be kept as short as possible.

Table 36. Slave Address Control Using Three-State Input Pins

AS2	AS1	AS0	Slave Address (A6 to A0)
L	L	L	0x61
L	L	H	0x62
L	L	NC	0x63
L	H	L	0x64
L	H	H	0x65
L	H	NC	0x66
L	NC	L	0x67
L	NC	H	0x68
L	NC	NC	0x69
H	L	L	0x6A
H	L	H	0x6B
H	L	NC	0x6C
H	H	L	0x6D
H	H	H	0x6E
H	H	NC	0x6F
H	NC	L	0x7
H	NC	H	0x71
H	NC	NC	0x72
NC	L	L	0x73
NC	L	H	0x74
NC	L	NC	0x75
NC	H	L	0x76
NC	H	H	0x77
NC	H	NC	0x78
NC	NC	L	0x79
NC	NC	H	0x7A
NC	NC	NC	0x7B

INTERFACE PROTOCOL

The AD7294 uses the following I²C protocols.

Writing a Single Byte of Data to an 8-Bit Register

The alert registers (0x05, 0x06, 0x07), power down register (0x0A), channel sequence register (0x08), temperature offset registers (0x26, 0x27), and the command register (0x00) are 8-bit registers; therefore, only one byte of data can be written to each. In this operation, the master device sends a byte of data to the slave device, see Figure 27. To write data to the register, the command sequence is as follows:

1. The master device asserts a start condition.
2. The master sends the 7-bit slave address followed by a zero for the direction bit, indicating a write operation.
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition to end the transaction.

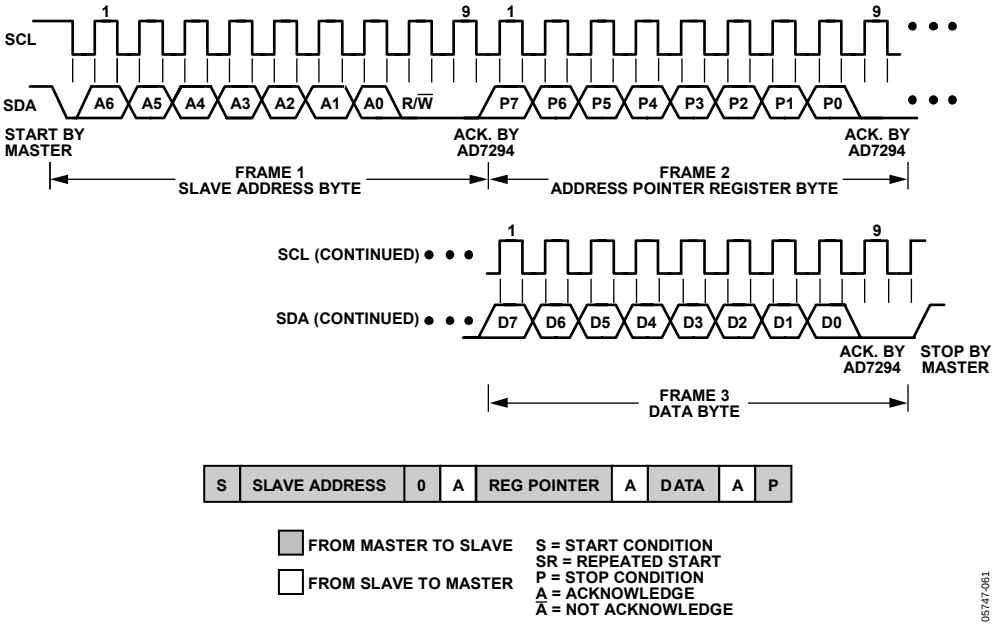


Figure 27. Single Byte Write Sequence

Writing Two Bytes of Data to a 16-Bit Register

The limit and hysteresis registers (0x0B to 0x25), the result registers (0x01 ~ 0x04), and the configuration register (0x09) are 16-bit registers; therefore, two bytes of data are required to write a value to any one of these registers. Writing two bytes of data to one of these registers consists of the following sequence:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address. The slave asserts an acknowldege on SDA.
5. The master sends the first data byte (most significant).
6. The slave asserts an acknowledge on SDA.
7. The master sends the second data byte (least significant).
8. The slave asserts an acknowledge on SDA.
9. The master asserts a stop condition on SDA to end the transaction.

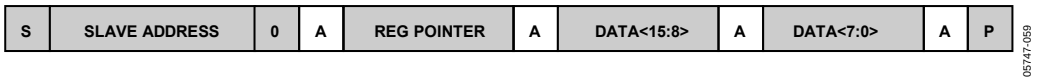


Figure 28. Writing Two Bytes of Data to a 16-Bit Register

Writing to Multiple Registers

Writing to multiple address registers consists of the following:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address, for example the power down register. The slave asserts an acknowledge on SDA.
5. The master sends the data byte.
6. The slave asserts an acknowledge on SDA.
7. The master sends a second register address, for example the configuration register. The slave asserts an acknowledge on SDA.
8. The master sends the first data byte.
9. The slave asserts an acknowledge on SDA.
10. The master sends the second data byte.
11. The slave asserts an acknowledge on SDA.
12. The master asserts a stop condition on SDA to end the transaction.

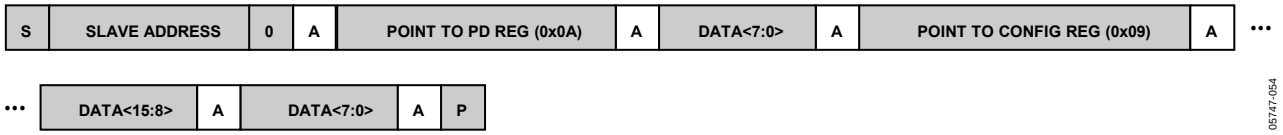


Figure 29. Writing Two Bytes of Data to a 16-Bit Register

Reading Data from an 8-Bit Register

Reading the contents from any of the 8-bit registers is a single-byte read operation, as shown in Figure 30. In this protocol, the first part of the transaction writes to the register pointer. When the register address has been set up, any number of reads can be performed from that particular register without having to write to the address pointer register again. When the required number of reads has been completed, the master should not acknowledge the final byte. This tells the slave to stop transmitting, allowing a stop condition to be asserted by the master. Further reads from this register could be performed in a future transaction without having to rewrite to the register pointer.

If a read from a different address is required, the relevant register address has to be written to the address pointer register, and again, any number of reads from this register can then be performed. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts an an acknowledge on SDA
6. The master receives another 8-bit data byte.
7. The master asserts a no acknolwedge (NACK) on SDA to inform the slave that the data transfer is complete.
8. The master asserts a stop condition on SDA, and the transaction ends.

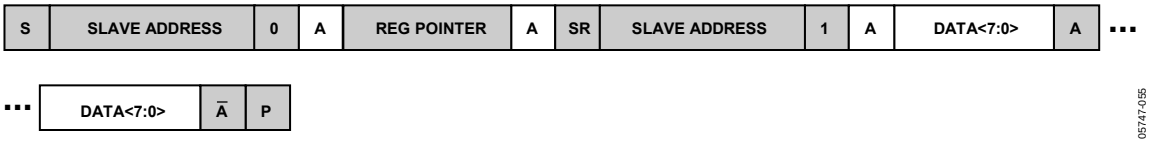


Figure 30. Reading Two Single Bytes of Data from a Selected Register

Reading Two Bytes of Data from a 16-Bit Register

In this example, the master device reads three lots of two-byte data from a slave device. This protocol assumes that the particular register address has been set up by a single-byte write operation to the address pointer register, see previous read example.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives a second data byte.
7. The master asserts an acknowledge on SDA.
8. The master receives a data byte.
9. The master asserts an acknowledge on SDA.
10. The master receives a second data byte.
11. The master asserts an acknowledge on SDA.
12. The master receives a data byte.
13. The master asserts an acknowledge on SDA.
14. The master receives a second data byte.
15. The master asserts a no acknowledge on SDA, so the slave knows that the data transfer is complete.
16. The master asserts a stop condition on SDA to end the transaction.

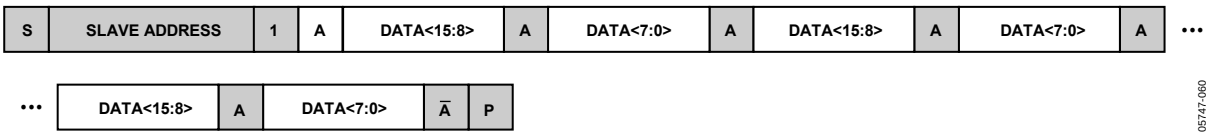


Figure 31. ReadingThree Lots of Two Bytes of Data from the Conversion Result Register

MODES OF OPERATION

There are two different methods of initiating a conversion on the AD7294.

COMMAND MODE

In command mode, the AD7294 ADC converts on demand on either a single channel or a sequence of channels. To enter this mode, the required combination of channels is simply written into the command register (0x00). The first conversion takes place at the end of this write operation, in time for the result to be read out in the next read operation. While this result is being read out, the next conversion in the sequence takes place, and so on. To exit the command mode, the master should not acknowledge the final byte of data. This stops the AD7294 transmitting, allowing the master to assert a stop condition on the bus. It is therefore important that after writing to the command register a repeated start (Sr) signal is used rather than a stop (P) followed by a start (S) when switching to read mode, otherwise the command mode exits after the first conversion.

After writing to the command register, the register pointer is returned to its previous value. If a new pointer value is required (typically the ADC Result Register 0x01), it can be written immediately following the command byte. This extra write operation does not affect the conversion sequence, because the second conversion is only triggered at the start of the first read operation.

The maximum throughput that can be achieved using this mode with a 400 kHz I^2C clock is (400kHz/18) = 22.2 kSPS.

The example in Figure 32 shows the command mode being used to convert on a sequence of channels including $V_{IN}0$, $V_{IN}1$, and $I_{SENSE}1$.

The AD7294 automatically exits command mode if no read occurs in a 5 ms period.

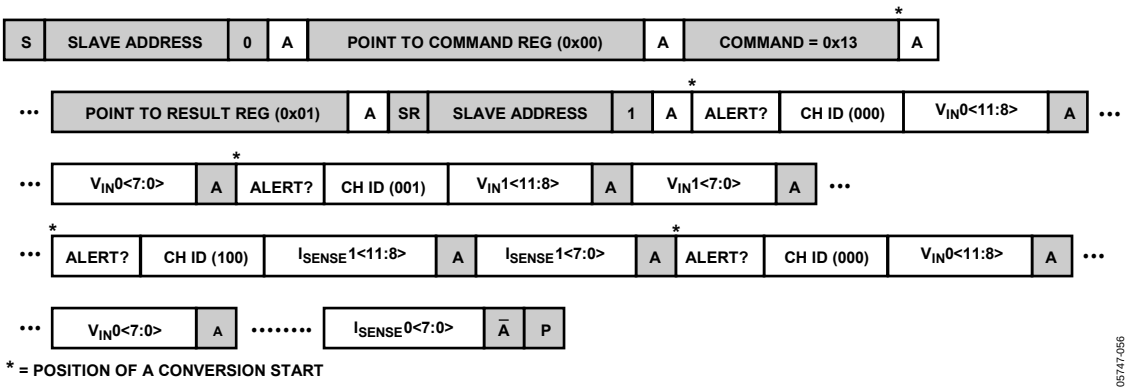


Figure 32. Command Mode Operation

AUTOCYCLE MODE

The AD7294 can be configured to convert continuously on a programmable sequence of channels. These conversions take place in the background approximately every 45 µs, and are transparent to the master. Reads and writes can still be performed at any time (the ADC Result Register 0x01 contains the most recent conversion result). This mode is typically used to automatically monitor a selection of channels with either the limit registers programmed to signal an out-of-range condition via the alert function or the minimum/maximum recorders tracking the variation over time of a particular channel.

Enable the autocycle function simply by setting the relevant bit (D12) in the configuration register (0x09). If the channel sequence register (0x08) is at its default value of 0x00, no automatic conversions occur.

The command mode can be used with autocycle enabled. In this case, the automatic conversion sequence pauses while the command mode is active and resumes when the command mode is exited (either by a stop bit or after 5 ms of idle time).

ALERTS AND LIMITS THEORY

ALERT_FLAG BIT

The Alert_Flag bit indicates whether the conversion result being read or any other channel result has violated the limit registers associated with it. If an alert occurs and the Alert_Flag bit is set, the master may wish to read the alert status register to obtain more information on where the alert occurred.

ALERT STATUS REGISTERS

The alert status registers are 8-bit read/write registers that provide information on an alert event. If a conversion results in activating the ALERT pin or Alert_Flag bit in the result register or T_{SENSE} registers, the alert status register can be read to gain further information. See Figure 33 for the alert register structure.

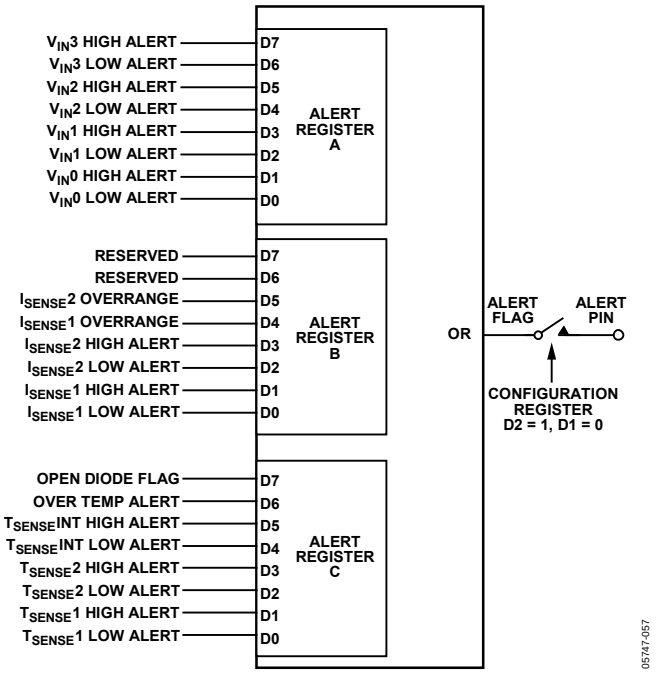


Figure 33. Alert Register Structure

Register A (see Table 21) consists of four channels with two status bits per channel, one corresponding to each of the $DATA_{HIGH}$ and $DATA_{LOW}$ limits. It stores the alert event data for $V_{IN}4$ to $V_{IN}0$, which are the standard voltage inputs. The bit with a status of 1 shows where the violation occurred—that is, on which channel—and whether the violation occurred on the upper or lower limit. If a second alert event occurs on another channel between receiving the first alert and interrogating the alert status register, the corresponding bit for that alert event is also set.

Register B (see Table 22) reserves two bits for user input. It also consists of three channels with two status bits per channel, representing the specified $DATA_{HIGH}$ and $DATA_{LOW}$ limits. Bits[D3:D0] correspond to the high and low limit alerts for the current sense inputs. Bit D4 and Bit D5 represent the I_{SENSE1} OVERRANGE and I_{SENSE2} OVERRANGE of $V_{REF}/10.41$. During power-up, it is possible for the fault outputs to be triggered depending on which supply comes up first. To prevent this, it is recommended to write a 0 to both I_{SENSE} overrange bits (D4 and D5) as part of the initialization routine.

The most significant bit of Register C (see Table 23) alerts the user when an open diode flag occurs on the external temperature sensors. An overtemperature alert for the external temperature sensor occupies D6. The remaining 6 bits in this register store alert event data for $T_{SENSE}1$, $T_{SENSE}2$, and $T_{SENSE}INT$ with two status bits per channel, one corresponding to each of the $DATA_{HIGH}$ and $DATA_{LOW}$ limits.

The entire contents of the alert status register can be cleared by writing 1 to Bit D1 and 1 to Bit D2 in the configuration register, as shown in Table 26. This can also be achieved by writing all 1s to the alert status register itself. Therefore, if the alert status register is addressed for a write operation, which is all 1s, the contents of the alert status register are cleared or reset to all 0s.

$DATA_{HIGH}$ AND $DATA_{LOW}$ MONITORING FEATURES

The AD7294 signals an alert (in either hardware, software, or both, depending on the configuration) if the result moves outside the upper or lower limit set by the user.

The $DATA_{HIGH}$ register stores the upper limit that activates the ALERT output pin and/or the Alert_Flag bit in the conversion result register. If the value in the conversion result register is greater than the value in the $DATA_{HIGH}$ register, an alert occurs. When the conversion result returns to a value of at least N LSB below the $DATA_{HIGH}$ register value, the ALERT output pin and Alert_Flag bit are reset. The value of N is taken from the 12-bit hysteresis register associated with that channel. For the T_{SENSE} limit registers, D11 is equal to 0 denoting the diode open-circuit flag in the T_{SENSE} registers.

The $DATA_{LOW}$ register stores the lower limit that activates the ALERT output pin and/or the Alert_Flag bit in the conversion result register. If the value in the conversion result register is less than the value in the $DATA_{LOW}$ register, an alert occurs. When the conversion result returns to a value of at least N LSB above the $DATA_{LOW}$ register value, the ALERT output pin and Alert_Flag bit are reset. The value of N derived from the hysteresis register associated with that channel.

The ALERT pin can also be reset by writing to Bit D2 and Bit D1 in the configuration register.

HYSTERESIS

The hysteresis register stores the hysteresis value, N, when using the limit registers. Each pair of limit registers has a dedicated hysteresis register. The hysteresis value determines the reset point for the ALERT pin/Alert_Flag bit if a violation of the limits occurs. For example, if a hysteresis value of 8 LSB is required on the upper and lower limits of $V_{IN}0$, the 16-bit word 0000 0000 0000 1000 should be written to the hysteresis register of $V_{IN}0$ (see Table 7). On power-up, the hysteresis registers

contain a value of 8 LSB for nontemperature result registers and 8°C, or 32 LSB, for the T_{SENSE} registers. If a different hysteresis value is required, that value must be written to the hysteresis register for the channel in question.

The advantage of having hysteresis registers associated with each of the limit registers is that it prevents a noisy environment setting and resetting the high and low alert bits associated with each ADC channel. **Error! Reference source not found.** shows the limit checking operation.

Using the Limit Registers to Store Minimum/Maximum Conversion Results

If full scale—that is, all 1s—is written to the hysteresis register for a particular channel, the $DATA_{HIGH}$ and $DATA_{LOW}$ registers for that channel no longer act as limit registers as previously described, but act as storage registers for the maximum and minimum conversion results returned from conversions on a channel over any given period of time. This function is useful in applications where the widest span of actual conversion results is required rather than using any of the ALERT functions to signal that an intervention is necessary. Note that on power-up, the contents of the $DATA_{HIGH}$ register for each channel are full scale, whereas the contents of the $DATA_{LOW}$ registers are zero scale by default. Therefore, minimum and maximum conversion values being stored in this way are lost if power is removed or cycled.

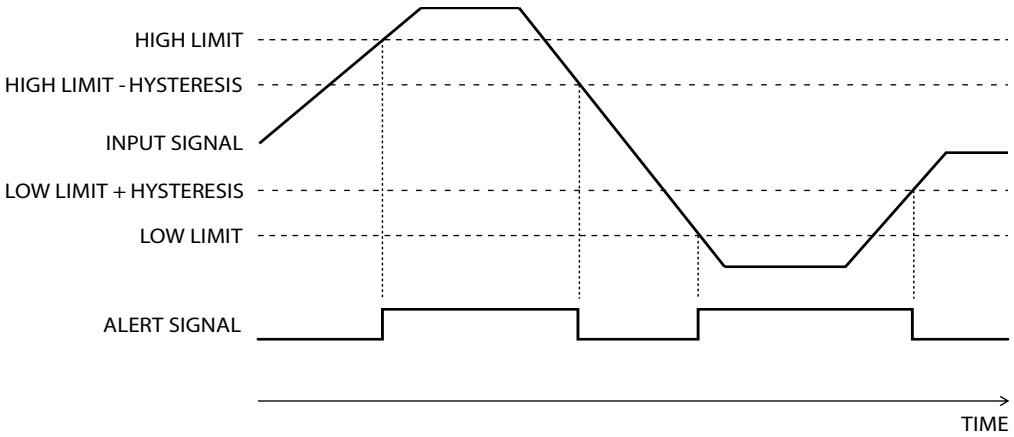


Figure 34. Limit Checking

APPLICATIONS

The AD7294 contains all the functions required for general-purpose monitoring and control of current, voltage, and temperature systems. With its 60 V maximum common-mode range, the device is useful in industrial and automotive applications where high voltage level current measurements are required. The part is also ideally suited to address the monitoring and controlling requirements of a power amplifier in a cellular base station.

BASE STATION POWER AMPLIFIER MONITOR AND CONTROL

The AD7294 is used in a power amplifier signal chain to achieve the optimal bias condition for the LDMOS transistor. The main factors influencing the bias conditions are temperature, supply voltage, gate voltage drift, and general processing parameters. The overall performance of a power amplifier configuration is determined by the inherent tradeoffs required in efficiency, gain, and linearity. Dynamically controlling the drain bias current to maintain a constant value over temperature and time can significantly improve the overall performance of the power amplifier.

The circuit in Figure 35 is a typical application for the AD7294. The device monitors and controls the overall performance of two final stage amplifiers. The gain control and phase adjustment of the driver stage are incorporated in the application and are carried out by the two available uncommitted outputs of the AD7294. Both high-side current senses measure the amount of current on the respective final stage amplifiers. The comparator outputs, $I_{SENSE}1$ OVERRANGE and $I_{SENSE}2$ OVERRANGE pins, are the controlling signals for switches on the RF inputs of the LDMOS power FETs. If the high-side current sense reads a value above a specified limit compared with the setpoint, the RF IN signal is switched off by the comparator.

By measuring the transmitted power (Tx) and the received power (Rx), the device can dynamically change the drivers and PA signal to optimize performance. This application requires a logarithmic detector/controller, such as Analog Devices, Inc. AD8317.

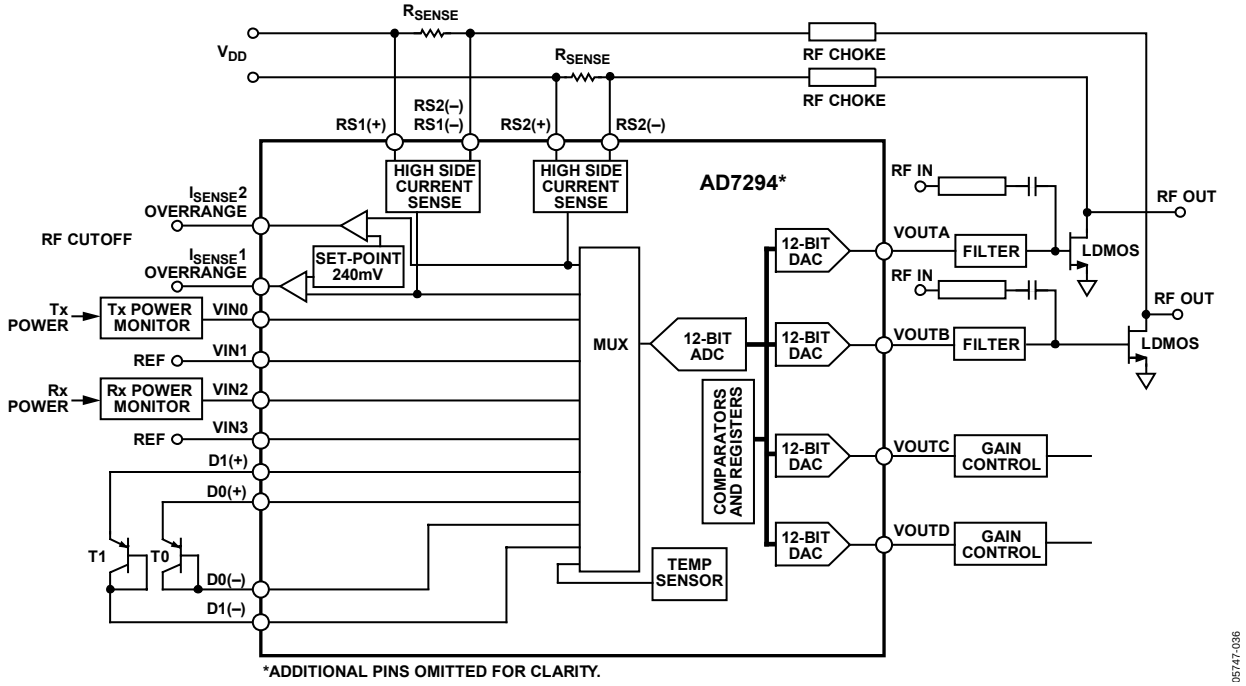


Figure 35. Typical HPA Monitor and Control Application

GAIN CONTROL OF POWER AMPLIFIER

In gain control mode, a setpoint voltage, proportional in dB to the desired output power, is applied to a power detector such as the AD8362. A sample of the output power from the power amplifier (PA), through a directional coupler and attenuator (or by other means), is fed to the input of the AD8362. The V_{OUT} is connected to the gain control terminal of the PA, see Figure 36. Based on the defined relationship between V_{OUT} and the RF input signal, the AD8362 adjusts the voltage on V_{OUT} (V_{OUT} is now an error amplifier output) until the level at the RF input corresponds to the applied V_{SET}. The AD7294 completes a feedback loop that tracks the output of the AD8362 and adjusts the V_{SET} input of the AD8362 accordingly.

V_{OUT} of the AD8362 is applied to the gain control terminal of the power amplifier. For this output power control loop to be stable, a ground referenced capacitor must be connected to the CLPF pin . This capacitor integrates the error signal (which is actually a current) that is present when the loop is not balanced. In a system where a variable gain amplifier (VGA) or variable voltage attenuator (VVA) feeds the power amp, only one AD8362 is required. In such a case, the gain on one of the parts (VVA, PA) is fixed and V_{OUT} feeds the control input of the other.

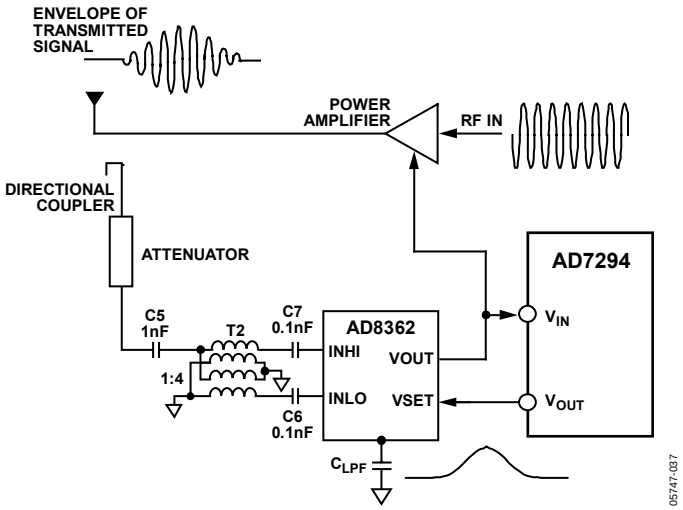


Figure 36. Setpoint Controller Operation

LAYOUT AND CONFIGURATION

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD7294 should have separate analog and digital sections, each having its own area of the board. If the AD7294 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD7294.

Bypass the power supply to the AD7294 s with 10 µF and 0.1 µF capacitors. Place the capacitors as physically close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and low effective series inductance (ESI); common ceramic types of capacitors are suitable. The 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching. The 10 µF capacitors are the tantalum bead type.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Shield clocks and other components with fast switching digital signals from other parts of the board by a digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side; however, this is not always possible with a 2-layer board.

Layout Considerations for External Temperature Sensors

Power Amplifier boards can be electrically noisy environments and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. Take the following precautions:

- Place the remote sensing diode as close as possible to the AD7294. If the worst noise sources are avoided, this distance can be 4 inches to 8 inches.
- Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks, if possible.
- Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended as shown in Figure 37.

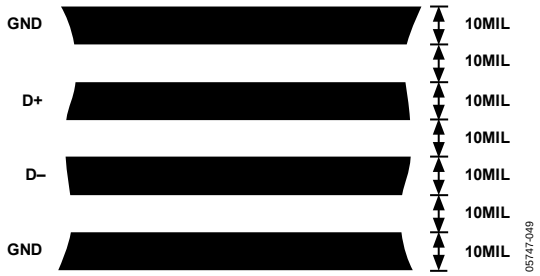


Figure 37. Arrangement of Signal Tracks

- Try to minimize the number of copper/solder joints because they can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D– path and are at the same temperature.
- Place a 10 pF capacitor between the base and emitter of the discrete diode, as close as possible to the diode.
- If the distance to the remote sensor is more than 8 inches, the use of twisted-pair cable is recommended.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor can be reduced or removed.

EVALUATION BOARD FOR THE AD7294

The AD7294 evaluation board consists of the AD7294 LFCSP package along with two R_{SENSE} resistors and a number of SMB sockets and jumpers to allow access to the various on-chip functionalities of the AD7294. Other on-board components interface the part to the PC, such as an EEPROM, a USB microcontroller, and a voltage regulator. More information regarding the AD7294 evaluation board is available in the EVAL-AD7294EB application note and should be consulted when evaluating the board.

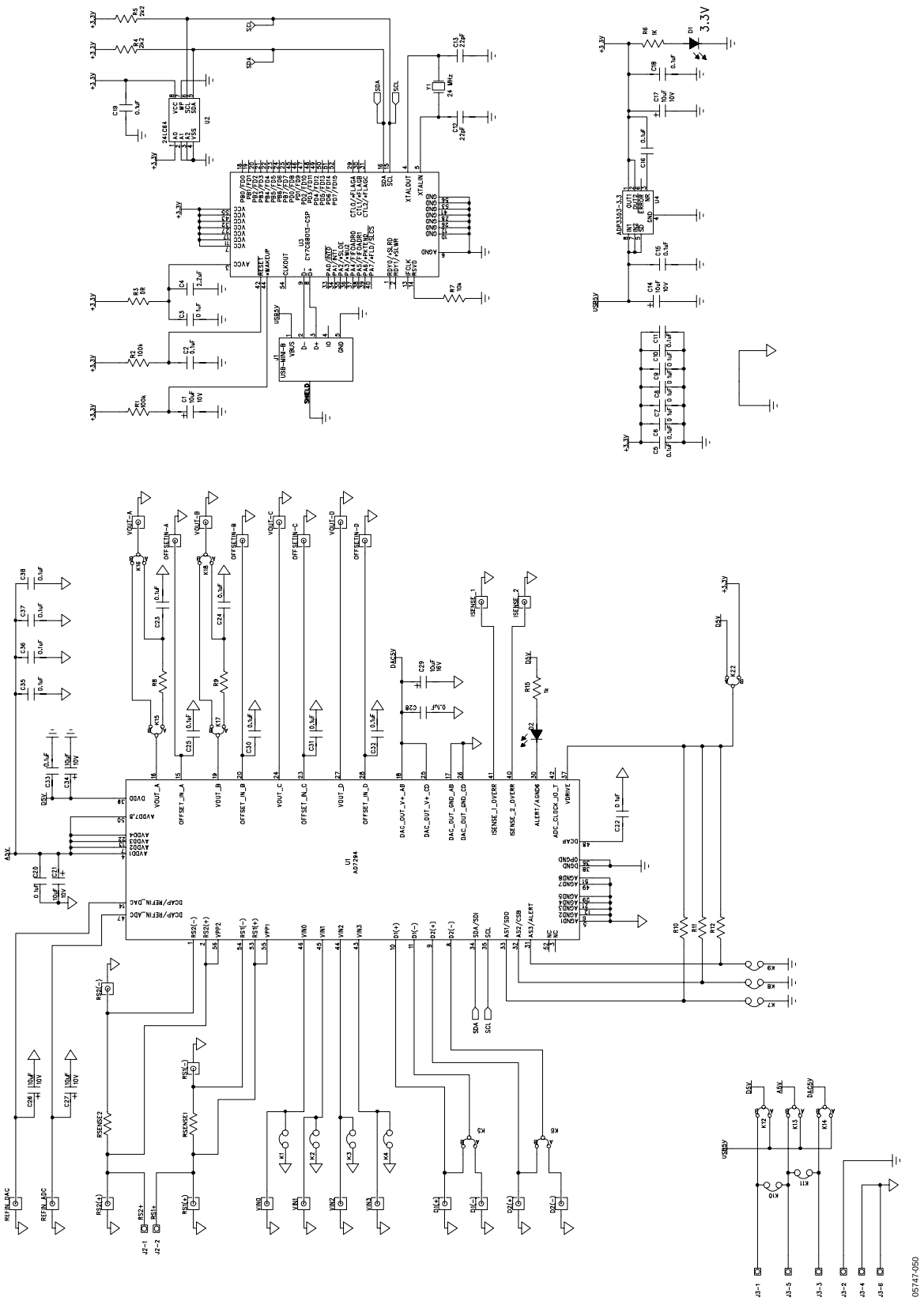


Figure 38. Evaluation Board Schematic

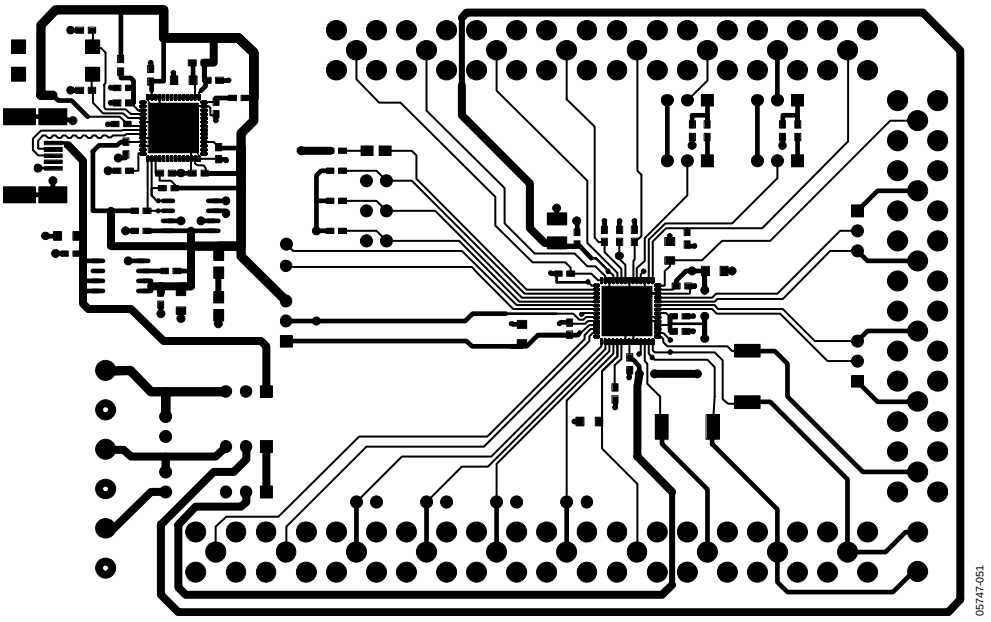


Figure 39. Component Side Artwork

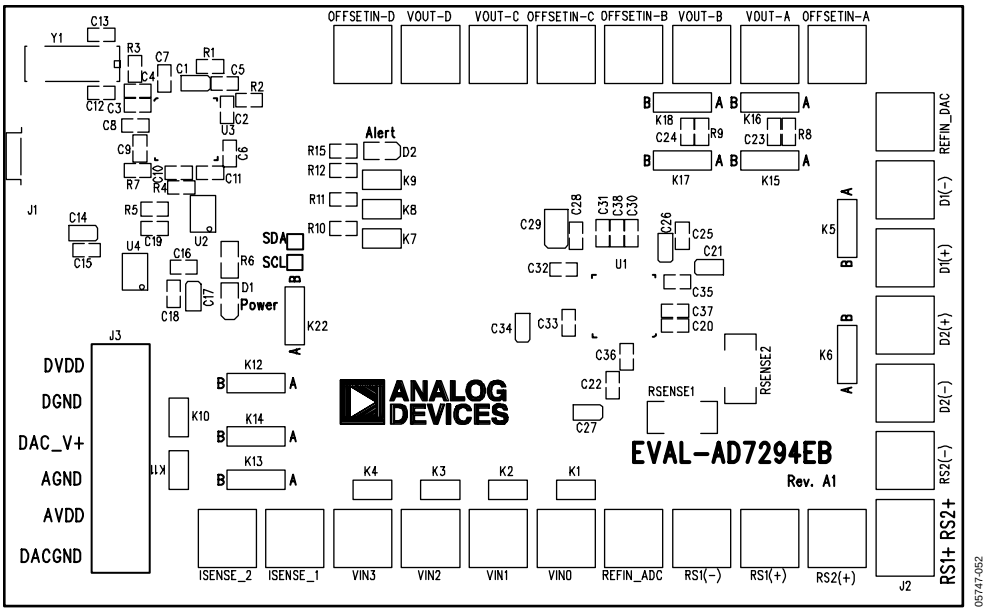


Figure 40. Component Side SilkScreen

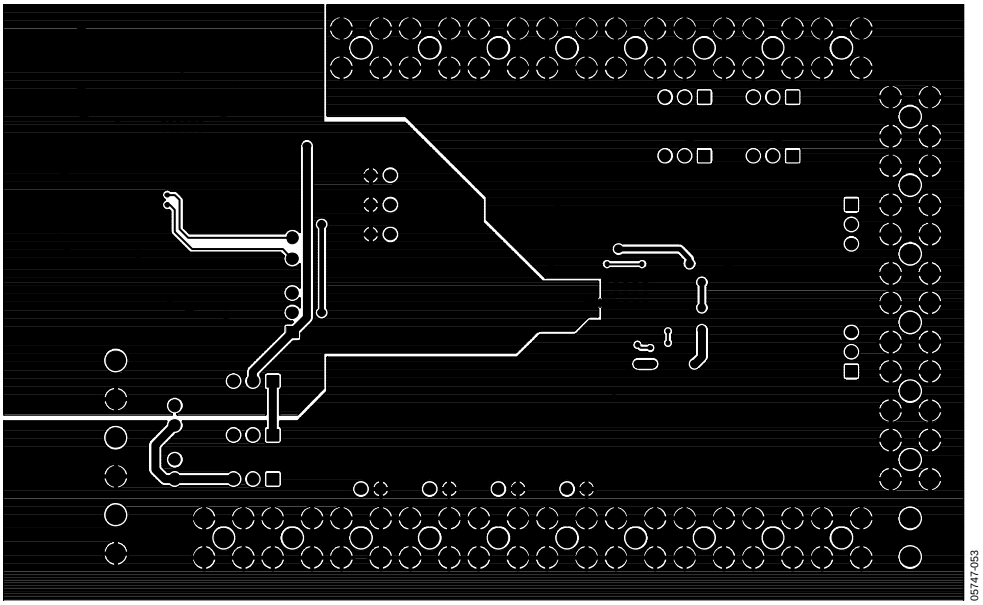
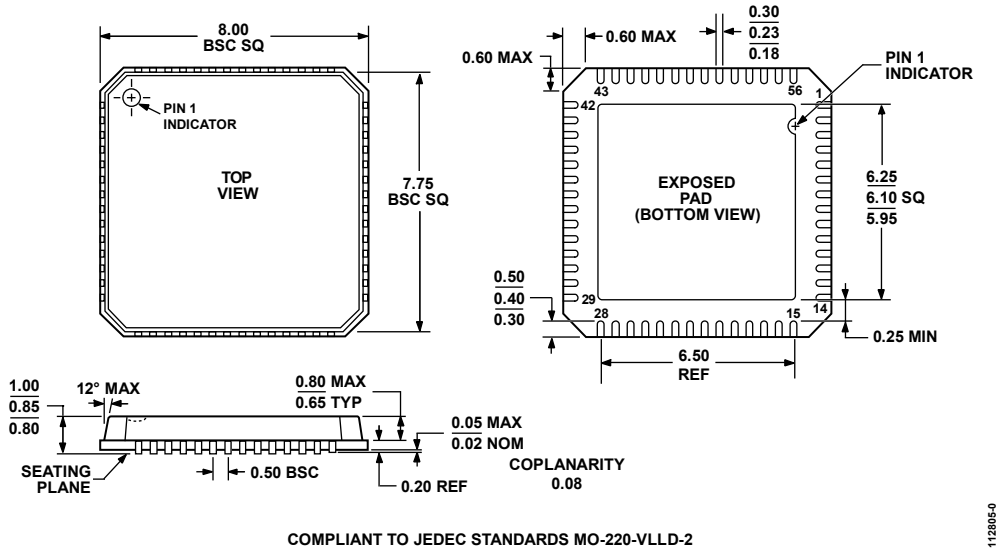


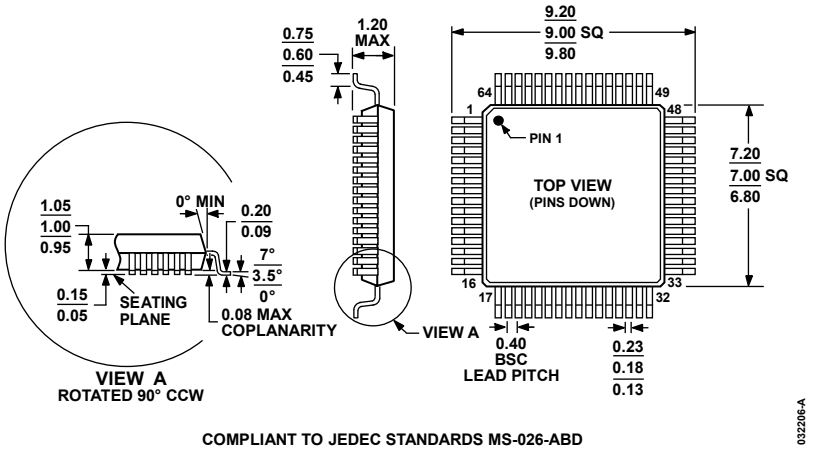
Figure 41. Solder Side Artwork

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 42. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8mm × 8 mm Body, Very Thin Quad
(CP-56-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-ABD

Figure 43. 64-Lead Thin Plastic Quad Flat Package [TQFP]
(SU-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7294BCPZ[1]	−40°C to +105°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-1
AD7294BSUZ[1]	−40°C to +105°C	64-Lead Thin Plastic Quad Flat Package [TQFP]	SU-64-1
EVAL-AD7294EBZ[1]		Evaluation Board.	

[1] Z = RoHS Compliant Part.

PR05747-0-10/07(PrD)