Monolithic Octal 12-Bit DACPORT

AD75089

FEATURES
Eight Complete Voltage Output DACs
On-Chip Voltage Reference
On-Chip Data Latches with Readback Feature
Output Voltage Range: ±5 V
Compact 44-Pin PLCC Package

APPLICATIONS
Automatic Test Equipment
Instrumentation
Avionics
Robotics
Process Control

PRODUCT DESCRIPTION

The AD75089 DACPORT® contains eight complete 12-bit, voltage output digital-to-analog converters in one monolithic IC. It thus offers the highest density 12-bit D/A function available.

Each DAC offers flexibility, accuracy and good dynamic performance. The R-2R structure is fabricated from thin-film resistors that are laser-trimmed to achieve guaranteed monotonicity over the full operating temperature range. DAC-to-DAC matching performance is specified.

The output amplifier combines the best features of bipolar and MOS devices to achieve good dynamic performance and low offset. Settling time is under 10 μs, and each output can drive a 2 mA, 500 pF load. Short circuit protection allows indefinite shorts to V_{CC}, V_{DD}, V_{SS}, and GND.

Digital circuitry is implemented in CMOS logic. The fast, low power, digital interface allows this DACPORT to interface with most microprocessors through a single 12-bit wide bus. A readback feature allows the internal DAC registers to be read back through the digital port as 12-bit words. When disabled, the readback drivers are placed in a high impedance mode.

A RESET control pin is provided to allow simultaneous asynchronous reset of all DAC data latches, causing the DAC outputs to go to the negative extreme of their range.

The analog portion of the DACPORT consists of eight DAC cells, eight output amplifiers, a voltage reference, a control amplifier and switches. Each DAC cell is an inverting R-2R type. The output current from each DAC is switched to the

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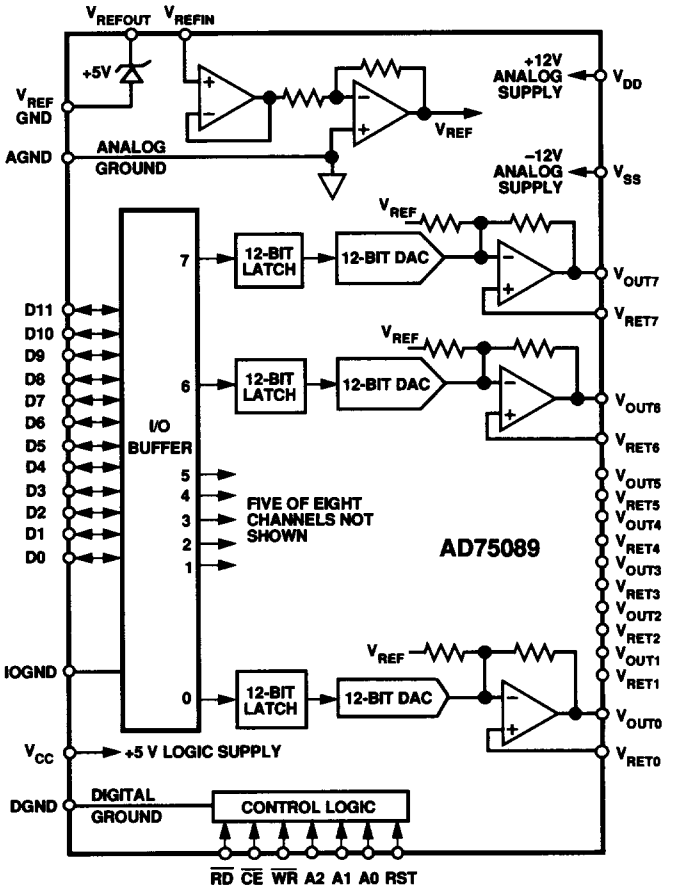
FUNCTIONAL BLOCK DIAGRAM



on-chip application resistors and output amplifier. The chip may be operated from the internal reference or an external reference.

The high performance and functional completeness of this DACPORT result from their fabrication in Analog Devices' BiMOS II process. This epitaxial BiCMOS process features bipolar transistors for precise analog circuitry, CMOS transistors for dense logic and analog switches, laser-trimmed thin-film resistors and double-level metal interconnects.

REV. 0

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AD75089—SPECIFICATIONS (V_{CC} = +5 V, V_{DD} = +12 V, V_{SS} = −12 V, V_{REFIN} = +5.000 V, all V_{RET} pins connected to Analog Ground, T_A = +25°C unless otherwise noted.)

Parameter	Min	Typ	Max	Units
RESOLUTION		12		Bits
ANALOG OUTPUT				
Voltage Range, V_{OUT} max to V_{OUT} min		±5		Volts
Output Current (Each Channel, Source or Sink)	2			mA
Load Capacitance (Each Channel)		500		pF
Short Circuit Current (Each Channel)		25	50	mA
ACCURACY				
Gain Error, Including Internal Reference	−15	±8	15	LSB
Integral Linearity Error	−1	±1/2	1	LSB
Integral Linearity Error, T_{MIN} to T_{MAX}		±1		LSB
Differential Linearity Error	−3/4	±1/4	3/4	LSB
Differential Linearity Error, T_{MIN} to T_{MAX}		±1/2		LSB
Gain Error Drift		±10		ppm of FSR/°C
Offset Drift		±7		ppm of FSR/°C
Noise, 0.1 to 2 MHz Bandwidth		200		μV rms
REFERENCE INPUT				
Input Resistance		10		MΩ
Voltage Range		+5.5/−3.0		Volts
REFERENCE OUTPUT				
Output Voltage	4.95		5.05	Volts
Temperature Coefficient		±15		ppm/°C
POWER REQUIREMENTS				
V_{CC}	4.5	5.0	5.5	Volts
I_{CC}		0.1	5	mA
V_{DD}, V_{SS}	±11.4	±12.0	±12.6	Volts
I_{DD}		16	28	mA
I_{SS}	−28	−15		mA
Total Power		350		mW
ANALOG GROUND CURRENT[1] PER EACH OF 8 CHANNELS		±600		μA
MATCHING PERFORMANCE				
Gain[2]	−5	±2.5	5	LSB
Offset[3]	−4	±2	4	LSB
CROSSTALK				
Analog (DC)[4]		−90		dB
Digital (Transient)[4]		−60		dB
DYNAMIC PERFORMANCE (R_L = 5 kΩ, C_L = 500 pF)				
Slew Rate		3.0		V/μs
Settling Time to ±1/2 LSB				
V_{OUT} max to V_{OUT} min or V_{OUT} min to V_{OUT} max		8		μs
POWER SUPPLY GAIN SENSITIVITY				
11.4 V ≤ V_{DD} ≤ 12.6 V		±8	±25	ppm/% of V_{DD}
−12.6 V ≤ V_{SS} ≤ −11.4 V		±8	±25	ppm/% of V_{SS}

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.4			Volts
V_{IL}	0		0.8	Volts
I_{IH} @ V_{IN} = V_{CC}	−10	±1	10	μA
I_{IL} @ V_{IN} = DGND	−10	±1	10	μA
DIGITAL OUTPUTS				
V_{OL} @ I_{SINK} = 1.6 mA			0.4	Volts
V_{OH} @ I_{SOURCE} = 0.5 mA	2.4			Volts
DIGITAL TIMING[5]				
Data Write Mode (Figure 1)				
Data Setup Time, t_{DSU}		0		ns
Address Setup Time, t_{ASU}		0		ns
Chip Enable-Write Time, t_{CEW}		0		ns
Write Pulse Width, t_W		40		ns
Write-Chip Enable Time, t_{WCE}		0		ns
Address Hold Time, t_{AH}		0		ns
Data Hold Time, t_{DH}		1		ns
Data Readback Mode (Figure 2)				
Address Setup Time, t_{ASU}		0		ns
Chip Enable-Read Time, t_{CER}		0		ns
Read Pulse Width, t_R		35		ns
Access Time from Read, t_{RD}		150		ns
Data Bus Release Time, t_{REL}		40		ns
Read-Chip Enable Time, t_{RCE}		0		ns
Address Hold Time, t_{AH}		0		ns
Asynchronous Reset				
Reset Pulse Width, t_{RST}		80		ns
TEMPERATURE RANGE (T_{MIN}, T_{MAX})	0		+70	°C

NOTES
[1]Analog ground current is the code dependent current flowing in each of the V_{RET} pins.
[2]Gain matching error is the largest difference in gain error between any two DACs in one package.
[3]Offset matching error is the largest difference in offset values between any two DACs in one package.
[4]See Definitions of Specifications section.
[5]Reference level for timing measurements = 1.5 V.

See definitions of specifications later on in this data sheet.
Specifications subject to change without notice.

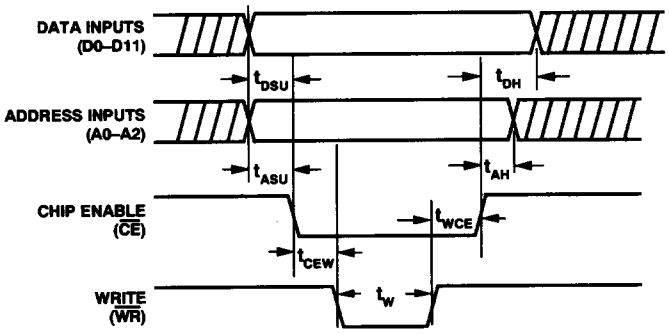


Figure 1. Write Timing Diagram

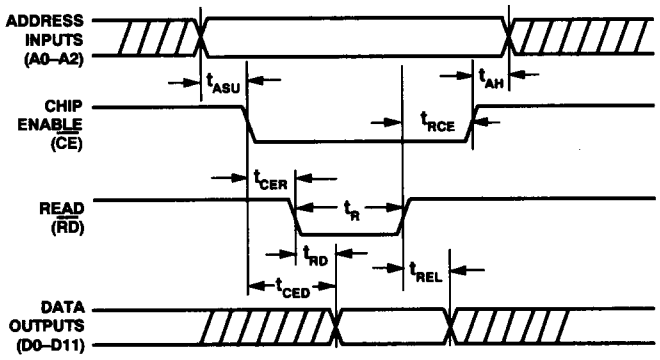


Figure 2. Readback Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

(Specifications apply to all grades except where noted)

V_{CC} to DGND or IOGND	0 V to +7 V
V_{DD} to AGND	0 V to +18 V
V_{SS} to AGND	−18 V to 0 V
V_{DD} to V_{SS}	0 V to +26.4 V
AGND to DGND	−1 V to +1 V
AGND to VREFGND	±13.2 V
AGND to VRET0–7	±13.2 V
V_{REFIN} Input	V_{DD} to V_{SS}
Digital Inputs	−0.3 V to +7 V
Analog Outputs	
	Indefinite Shorts to V_{CC}, V_{DD}, V_{SS}, and AGND
Soldering Temperature	+300°C, 10 sec
Power Dissipation	1000 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Output Voltage Range	Temperature Range	Package Option*
AD75089JP	±5 V	0°C to +70°C	P-44A

*P = Plastic Leaded Chip Carrier (PLCC) package.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD75089 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

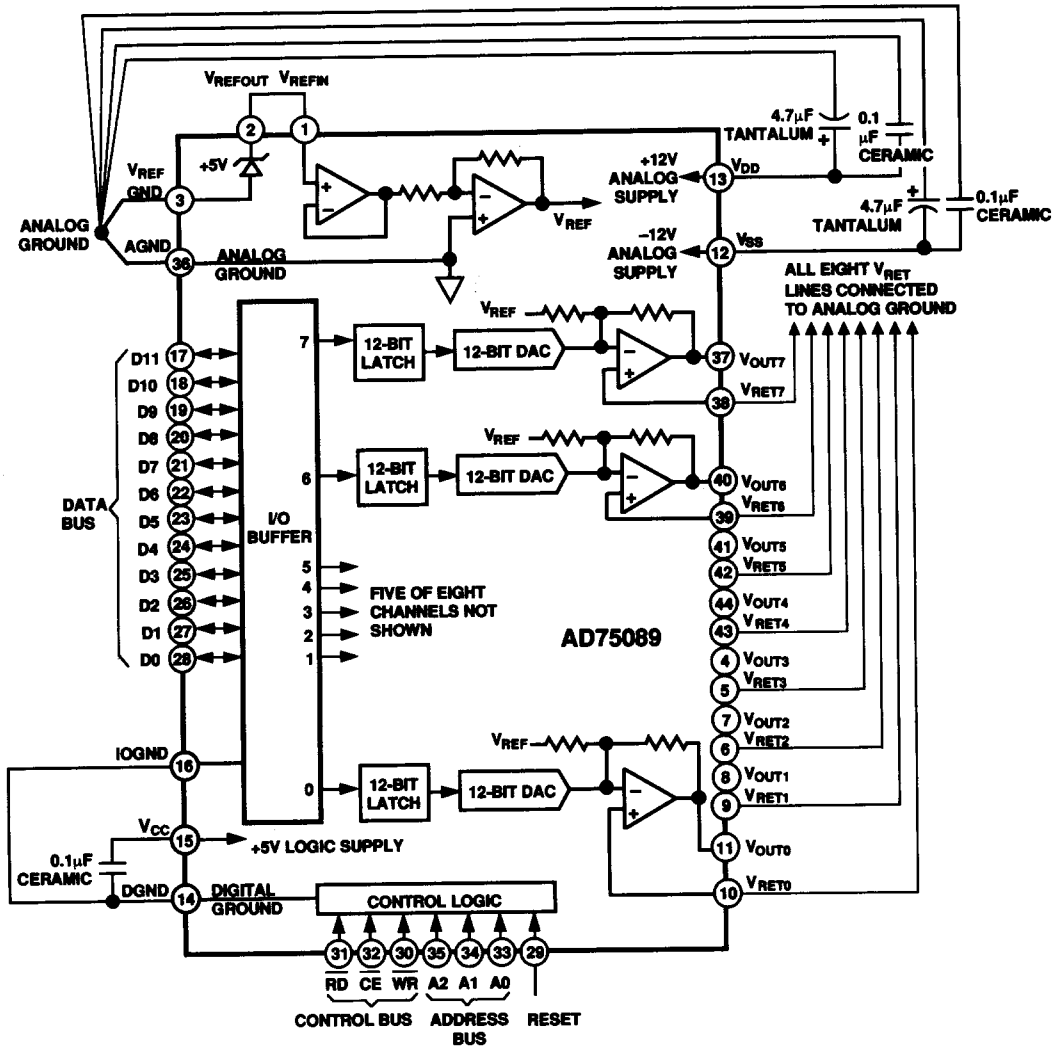
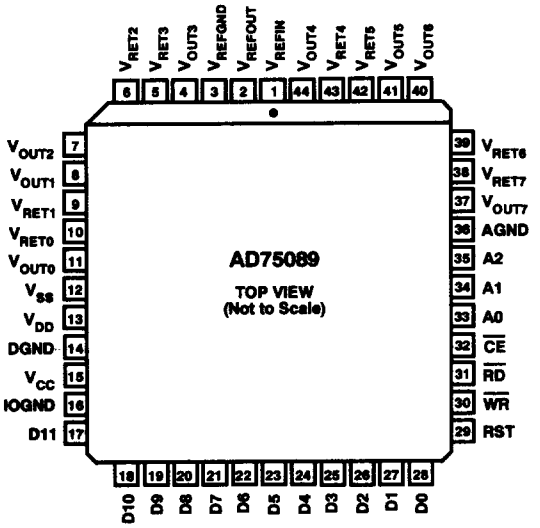


Figure 3. Recommended Circuit Schematic

PIN CONFIGURATION

44-Pin PLCC Package



DEFINITIONS OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR: Integral linearity error is the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from −full scale to +full scale) for any digital input code.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. The AD75089 is monotonic over its full operating temperature range.

DIFFERENTIAL LINEARITY ERROR: Monotonic behavior requires that the differential linearity error be less than 1 LSB over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code. For example, for a 10 V output span, a change of 1 LSB in digital input code should result in a 2.44 mV change in the analog output (1 LSB = 10 V/4096 = 2.44 mV). If in actual use, however, a 1 LSB change in the input code results in a change of only 0.61 mV (1/4 LSB) in analog output, the differential nonlinearity error would be −1.83 mV, or −3/4 LSB.

GAIN ERROR: DAC gain error is a measure of the difference between the output span of an ideal DAC and an actual device.

SETTLING TIME: Settling time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition.

PIN DESCRIPTIONS

Pin	Name	Description
1	V_{REFIN}	Reference Input
2	V_{REFOUT}	5 V Reference Output
3	V_{REFGND}	Reference Ground
4	V_{OUT3}	Analog Output 3
5	V_{RET3}	Analog Return 3
6	V_{RET2}	Analog Return 2
7	V_{OUT2}	Analog Output 2
8	V_{OUT1}	Analog Output 1
9	V_{RET1}	Analog Return 1
10	V_{RET0}	Analog Return 0
11	V_{OUT0}	Analog Output 0
12	V_{SS}	−12 V Analog Power Supply
13	V_{DD}	+12 V Analog Power Supply
14	DGND	Digital Ground
15	V_{CC}	+5 V Logic Power Supply
16	IOGND	Bus Interface Ground
17	D11	Data Bus Bit 11 (MSB)
18	D10	Data Bus Bit 10
19	D9	Data Bus Bit 9
20	D8	Data Bus Bit 8
21	D7	Data Bus Bit 7
22	D6	Data Bus Bit 6
23	D5	Data Bus Bit 5
24	D4	Data Bus Bit 4
25	D3	Data Bus Bit 3
26	D2	Data Bus Bit 2
27	D1	Data Bus Bit 1
28	D0	Data Bus Bit 0 (LSB)
29	RST	Reset Input; Active High
30	$\overline{WR}$	Write Input; Active Low
31	$\overline{RD}$	Read Input; Active Low
32	$\overline{CE}$	Chip Enable Input; Active Low
33	A0	Address Input Bit 0 (LSB)
34	A1	Address Input Bit 1
35	A2	Address Input Bit 2 (MSB)
36	AGND	Analog Ground
37	V_{OUT7}	Analog Output 7
38	V_{RET7}	Analog Return 7
39	V_{RET6}	Analog Return 6
40	V_{OUT6}	Analog Output 6
41	V_{OUT5}	Analog Output 5
42	V_{RET5}	Analog Return 5
43	V_{RET4}	Analog Return 4
44	V_{OUT4}	Analog Output 4

CROSSTALK: Crosstalk is the change in an output caused by a change in one or more of the other inputs or outputs. Analog or DC crosstalk is primarily caused by internal heating or ohmic drops arising from changes in load current. Digital or transient crosstalk is produced by capacitive coupling from the data inputs or from other changing DAC outputs.

FULL-SCALE RANGE: FSR is 10 V for the ±5 V range.

TRANSISTOR COUNT

The AD75089 contains 5,225 transistors.

BINARY CODE TABLE

Offset Binary Value in DAC Latch	Nominal Analog Output Voltage, V_{REF} = +5.000 V
MSB LSB	
1111 1111 1111	+4.9976 V
1000 0000 0000	0.0000 V
0000 0000 0000	−5.0000 V

ANALOG CIRCUIT CONSIDERATIONS

Grounding Recommendations

The AD75089 has twelve pins for analog and digital grounds, designated AGND, V_{RET0}–V_{RET7}, V_{REFGND}, IOGND, and DGND. The AGND pin is the ground reference point for the device. V_{REFGND} is the ground reference point for the on-chip voltage reference. V_{RET0} through V_{RET7} are the 8 ground return pins for the 8 DACs and their output amplifiers. The 10 analog ground pins should be connected radially to the analog ground point in the system. The external reference and any external loads should also be returned to the analog ground point. To minimize crosstalk, all paths to the single analog ground point must be short and direct.

The IOGND and DGND pins should be connected to the digital ground point in the circuit. These pins return current from the bus interface and logic portions, respectively, of the AD75089 circuitry to ground.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection may be broken or otherwise disconnected, then two diodes should be connected in inverse parallel between the analog and digital ground pins of the AD75089 to limit the maximum ground voltage difference.

Power Supplies, Sequencing and Decoupling

The AD75089 requires three power supplies for proper operation. V_{CC} powers the logic portions of the device and requires +5 volts. V_{DD} and V_{SS} power the remaining portions of the circuitry and require +12 V and −12 V, respectively.

All junction-isolated parts powered from multiple supplies require proper attention to supply sequencing. Because BiMOS II uses junction isolation, parasitic diodes exist between V_{DD} and V_{CC} and between V_{SS} and DGND. These parasitic diodes must be reverse-biased to prevent potentially destructive latch-up. This means that V_{DD} must always be greater than (V_{CC} − 0.5 V) and V_{SS} must always be less than (DGND + 0.5 V). External Schottky (e.g., 1N5818) or silicon (e.g., 1N4001) diodes may be used for protection when system supply sequencing cannot be guaranteed. One diode should be connected between V_{DD} and V_{CC}, with the anode connected to V_{CC}. A second diode should connect DGND and V_{SS}, with the anode tied to V_{SS}.

Decoupling capacitors should be used on all power supply pins. Good engineering practice dictates that the bypass capacitors be located as near as possible to the package pins. Recommended values are 4.7 μF tantalum and 0.1 μF ceramic from V_{DD} and V_{SS} to analog ground, and 0.1 μF from V_{CC} to digital ground.

Voltage Reference

The AD75089 is designed to operate from a reference voltage of +5 V. The internal reference can serve the entire chip. If superior tolerance, PSRR, or temperature performance are needed, external devices, such as the AD586, may be used.

Output Considerations

Each DAC output can source or sink ±2 mA of current to an external load. Short-circuit protection limits load current to a maximum of 40 mA per channel. Load capacitance of up to 500 pF can be accommodated with no effect on stability.

AD75089 output voltage settling time is 10 μs maximum. Figure 4 shows the output voltage settling time of the AD75089 with a fixed 5 V reference and all bits switched from 1 to 0 and from 0 to 1.

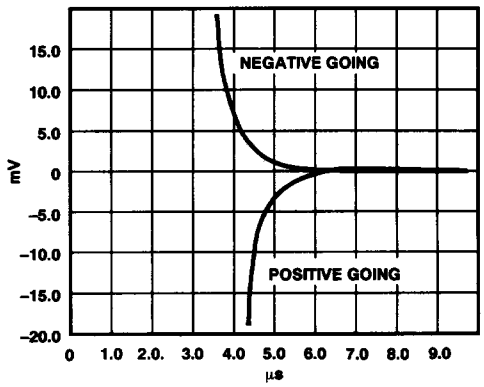


Figure 4. Settling Time; Full-Scale Output Change

Crosstalk

Crosstalk is a spurious signal on one DAC output caused by a change in one or more of the other DACs. Crosstalk can be induced by capacitive, thermal, or load-current induced feedthrough. Figure 5 shows typical crosstalk. The upper trace of the left photo shows DAC 6 switching from −5.0 V to +5.0 V and back to −5.0 V. The lower trace shows brief spikes in the output of DAC 7 caused by capacitive feedthrough from the input data. The longer disturbances are caused by analog feedthrough from DAC 6's output. The loads of both DACs are 5 kΩ in parallel with 500 pF. The right photo shows the detail of the falling edge of DAC 6 (large trace) and the effect on DAC 7 (middle trace) under the same conditions.

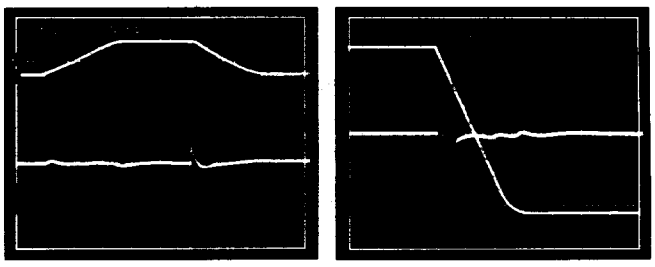


Figure 5. Output Crosstalk

DIGITAL INTERFACING

To write to the chip, apply the desired address, and then take Chip Enable ($\overline{CE}$) and Write ($\overline{WR}$) low. Typically, $\overline{CE}$ is tied to the system address decoder, and $\overline{WR}$ connects to the system write strobe.

If the data is changed while $\overline{CE}$ and $\overline{WR}$ are low, the DAC register is transparent, and it will follow the input data.

Readback

To read data back from the chip, apply the desired address, and then take Chip Enable ($\overline{CE}$) and Read ($\overline{RD}$) low. Typically, $\overline{CE}$ is tied to the system address decoder, and $\overline{RD}$ connects to the system read strobe.

If the address is changed while $\overline{CE}$ and $\overline{RD}$ are low, the data output will follow the selected address after a delay of t_{AD}.

Data Reset

To reset all data latches asynchronously, take Reset (RST) high. This clears all data latches and causes the DAC outputs to go to the negative end of their output range, i.e., −5 V.

APPLICATIONS

RESET TO ZERO VOLTS

Asserting RESET clears all AD75089's DAC registers and forces the DAC outputs to −5 V. In some cases a reset to 0 V is preferable. The circuit in Figure 6a will force all DAC outputs to 0 V following a reset.

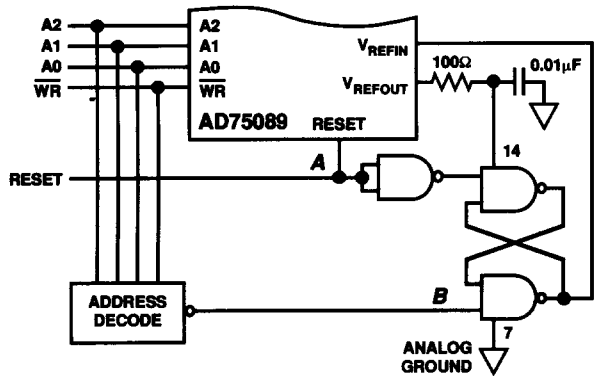


Figure 6a. Circuitry to Reset All AD75089 DAC Outputs to 0 V

This circuit takes advantage of the high input impedance of V_{REFIN} and the fact that a CMOS gate's output looks like a resistance connected to either of the gate's power supply pins. The gate's V_{DD} is supplied by the AD75089's Reference Output, and its V_{SS} terminal should be connected to Analog Ground. Resetting the AD75089 will also reset the S-R flip-flop formed by the two cross-coupled gates, forcing V_{REFIN} and all eight DAC outputs to ground. The flip-flop is set by a low-going pulse applied to node B, driving the high impedance V_{REFIN} pin to the gate's supply voltage of V_{REFOUT}. Address decoding will ensure that the flip-flop's output remains low until all eight DACs have been updated.

This circuit can latch up if the logic-1 voltages applied to nodes A or B exceed V_{REFOUT} by more than 300 mV. Simple resistor dividers can be used as shown in Figure 6b to protect against this possibility.

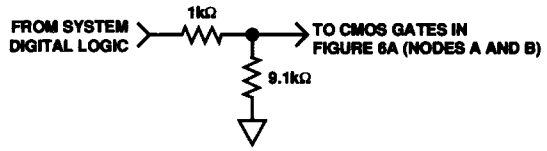


Figure 6b. Protecting Against V_{DD} (Digital Logic) > V_{REFOUT}

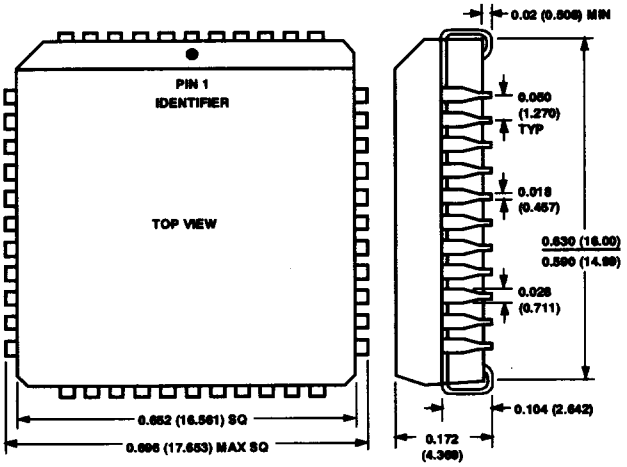
Offsetting Output Ranges

The functional block diagram in Figure 3 implies that the AD75089's output ranges can be offset by driving the various V_{RET} pins. Unfortunately, the actual internal circuitry differs from the simplified arrangement in the figure, and the gain seen from a V_{RET} "input" to the associated DAC output is actually code-dependent. A nonzero voltage applied to a V_{RET} terminal will offset the companion V_{OUT} by an amount that changes with the applied DAC code. Offsetting the AD75089's output ranges by driving the V_{RET} pins is NOT recommended. External amplifiers with the appropriate gain and level shifting circuitry should be used if output spans other than −5 V to +5 V are required.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

44-Lead Plastic Leaded Chip Carrier (P-44A)



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