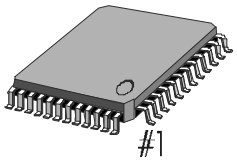
INTRODUCTION

S1T8528 is a 1 CHIP RF IC which can be used in high performance CTO CLP systems at max. 60MHz. S1T8528 is designed to include a receiver, PLL and COMPANDER to minimize PCB space requirements. Improved RX characteristics such as inter-modulation, spurious response and adjacent channel interface have been included to satisfy the universal standards.

The 1 CHIP RF IC has considerably reduced the cost by including a build-in 1'st mixer, low battery detector, fMCU, RSSI, RF regulator and speaker amp. Also, it fulfills carrier detector threshold control, speaker volume control, operating mode selection and MUTE function using S/W, thus making external application easier.

48–QFP–1010E



FEATURES

- Operating voltage range: 2.0V ~ 5.5V
- Typical supply current: 8.9mA at 3.6V
- Built-in low battery detection function (selectable 3.45V, 3.3V, 3.0V, 2.2V, 2.1V)
- Built-in speaker volume control and speaker amplifier
- Built-in splatter filter
- Support mode selection (Active, Rx, Standby and Inactive mode)
- FM Receiver
  - — Excellent Receiver characteristics

< 10.7MHz crystal filter used >

Input sensitivity	Adjacent channel rejection	Spurious rejection (image of the second IF)	Intermodulation rejection
0.7μVrms at 12dB SINAD	> 55dB	> 60dB	> 50dB

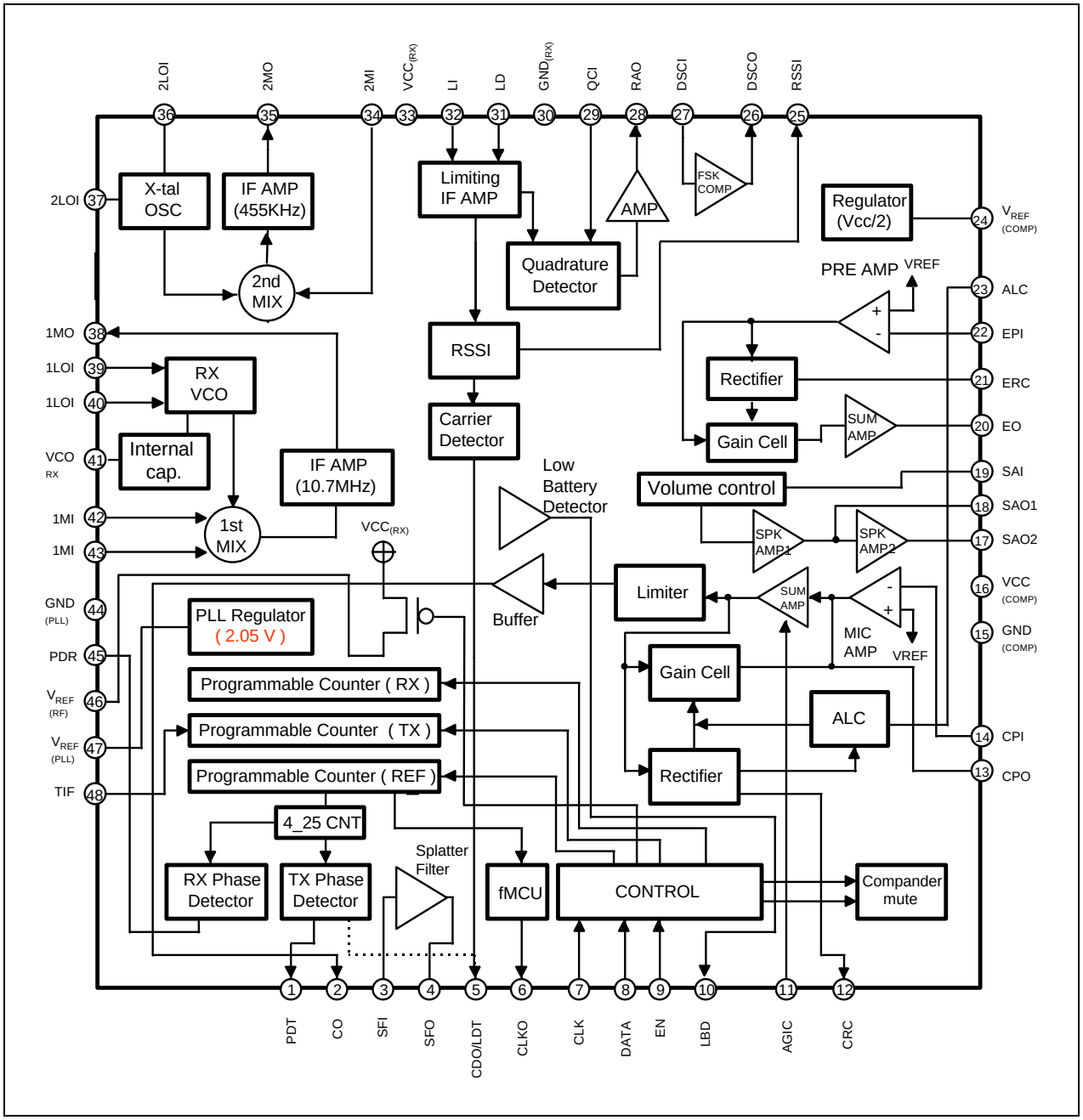
  - — RSSI (Linear) and Carrier detector output (Digital) function
- Compander
  - — Easy gain control and application using external component
  - — -Included ALC (Automatic Level Control) circuit
- Universal PLL
  - — RX (TX) divided counter range : 1/16 ~ 1/16383
  - — Reference frequency divided counter range : 1/16 ~ 1/4095
  - — Lock detector signal output
  - — Serial interface with MICOM for controlling each block
  - — Clock Output for MICOM oscillator substitution. (X-tal divided clock by 2, 3, 4 and 5)

ORDERING INFORMATION

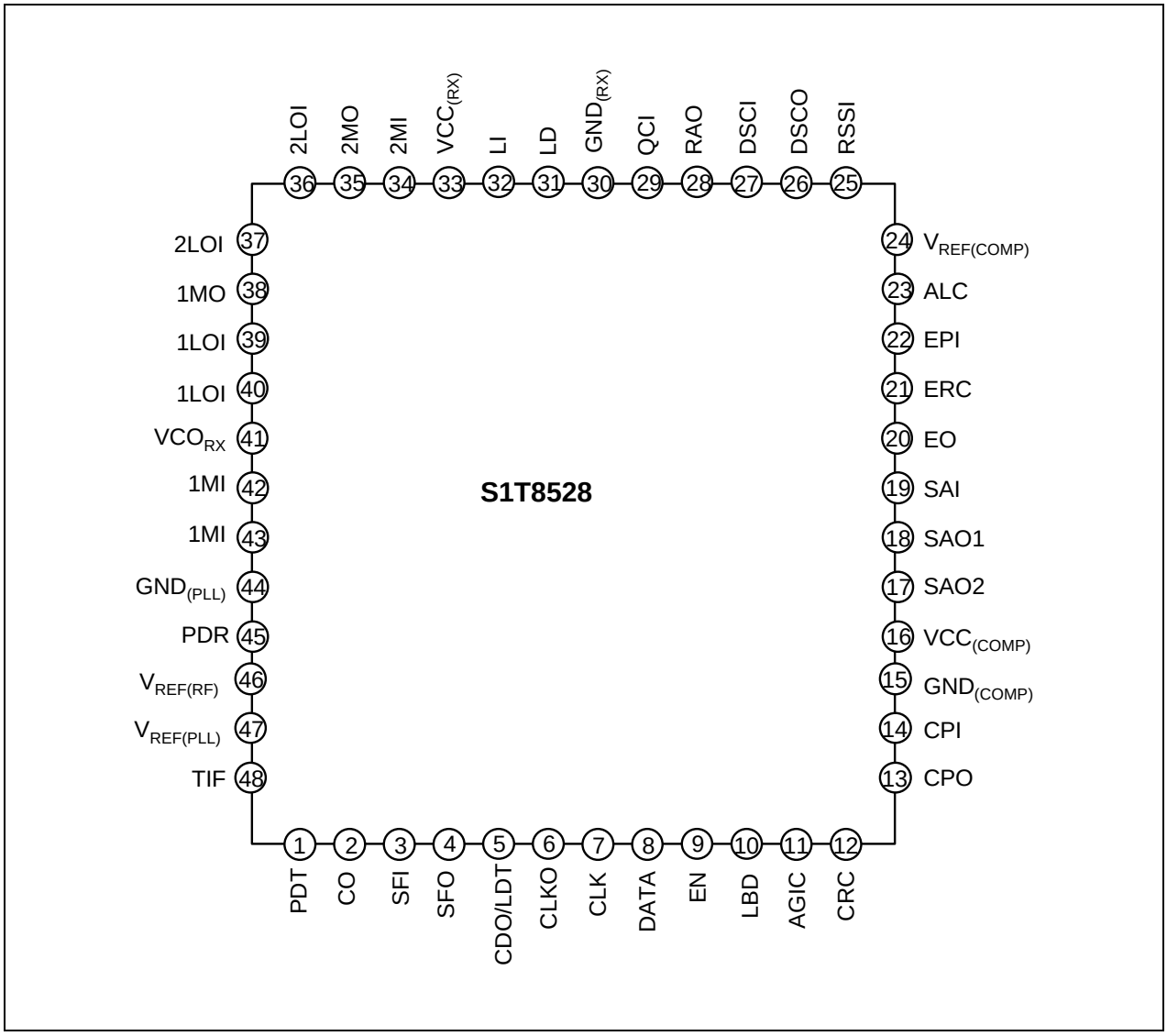
Device	Package	Operating Temperature
+ S1T8528X01-Q0R0	48–QFP–1010E	–20C to + 70C

+ : New product

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	Description
1	PDT	Phase detector output terminal of the transmitter at PLL. If $f_{TX} > f_{REF}$ or f_{TX} is leading $\rightarrow$ the output is negative pulse If $f_{TX} < f_{REF}$ or f_{TX} is lagging $\rightarrow$ the output is positive pulse If $f_{TX} = f_{REF}$ and the same phase $\rightarrow$ the output is High Impedance
2	CO	Compressor output terminal of compander: connected to the splatter filter amp input terminal.
3	SFI	Input terminal of Splatter filter amp.
4	SFO	Output terminal of Splatter filter amp.
5	LDT/CDO	LDT: Output terminal of transmitter lock detector in PLL block. Output is low if PLL is in lock state and is high if PLL is in unlock state. CDO: As an output terminal of the carrier detector buffer, connected to (RSSI) terminal of MICOM. This pin outputs the contents of Meter Driver buffer which is turned on/off, according to the signal level detected by Meter Driver.
6	f_{MCU}	Clock output terminal for MCU crystal. This pin provides the clock source for MCU or other system as an output of X-tal osc. ÷ 2/ ÷3/ ÷4/ ÷5. Which can be controlled by the bit of the control register. Clock ON/OFF control is possible by MCU
7 8 9	CLK DATA EN	These pins are serial interface terminals for programming reference counter, auxiliary reference counter, TX channel counter, RX channel counter and control block that controls internal each block with 4 mode selection.
10	LBD	Low Battery Detecting output. (Selectable 3.45V, 3.3V, 3.0V, 2.2V, 2.0V). During the normal operation, output level is low, but it is high at low battery detection. As this pin is an open collector type, it requires a pull-up resister.
11	AGIC	This pin bypasses AC elements at the feedback loop which come from the SUM amp block of COMPRESSOR. A capacitor should be connected between this terminal and GND. (C = 2.2uF)
12	CRC	Converts waveform from the full wave rectifier to DC element at the rectifier block of Compressor. (RC = 33 msec at C = 3.3uF)
13	CPO-	Pre-amp output terminal of Compressor. Used as an input terminal for voice signals.
14	CPI	Inverting type Pre-amp input terminal of Compressor.
15	$GND_{(COMP)}$	Ground. Ground of Compander.
16	$Vcc_{(COMP)}$	Supply voltage. Power supply terminal of Compander.
17	SAO 2	Output terminal of speaker amp 2. This signal is the same as SAO1 output, but phase difference is 180° for SAO1 DC voltage level is Vcc / 2.

PIN DESCRIPTION (Continued)

Pin No	Symbol	Description
18	SAO 1	Output terminal of Speaker amp 1. DC voltage level is Vcc/ 2.
19	SAI	Speaker Amp 1 input terminal. Between this terminal and Expander output terminal, apply DC coupled capacitor.
20	EO	Output terminal of Expander
21	ERC	Converts waveform from the full wave rectifier to DC element at the rectifier block of Expander. (RC = 33 msec at C = 3.3uF)
22	EPI	Pre-amp inverting input terminal of Expander. Adjusts the negative feedback loop gain. (in application, gain is 5)
23	ALC	Reference current input terminal of Automatic Level Control (ALC); Adjusts THD of compressor output voltage to less than 3% or limits the frequency deviation of TX if the input is higher than a certain level. The ALC circuit may be turned off depending on the ALC reference current or the magnitude of output voltage may be limited if it is higher than a certain level.
24	$V_{REF(COMP)}$	Reference voltage (VREF= 1/2 VCC). Supplies a regulator voltage to the Compressor and Expander of COMPANDER.
25	RSSI	Received Signal Strength Indicator terminal (Analog type)
26	DSCO	Output terminal of Data Slicing comparator. Separates Frequency Shift Keying (FSK) serial data and executes data shaping and limiting.
27	DSCI	Input terminal of Data slicing comparator. Non-inverting type with the negative input terminal biased to 1/2 Vcc.
28	RAO	Recovered Audio Output terminal. Voice signals detected by the Quadrature Detector are amplified and then output through this terminal.
29	QCI	Quadrature coil input terminal. The 455kHz oscillator circuit is an Lp = 680uH, Cp = 180pF valued LC tank circuit. Voice signals are detected by mixture of 455kHz (by phase difference) which is converted from mixer 2.
30	GND_{RX}	Ground . Ground for Receiver.
31 32	LD LI	Limiter input and decoupling terminal. Limiter block removes amplitude modulation elements caused by fading or FM signal noise. Limiting IF stage makes the second intermediate frequency amplify and limit. The input impedance of the limiting IF amplifier is set to 1.5kΩ. While FM waves are transmitted with constant magnitude, their magnitudes are slightly modulated due to reflection from obstacles, fading phenomenon, noise wave and mixing with AM wave elements before entering the receiver's antenna. The limiter makes amplitude uniform by removing these AM wave elements.
33	$V_{CC(RX)}$	Supply voltage. Supplies power to the Receiver.

PIN DESCRIPTION (Continued)

Pin No	Symbol	Description
34	2MI	Input terminal of mixer 2. Output from mixer 1 is entered to mixer 2 input terminal via 10.7MHz ceramic filter. Second mixer converts frequency to second intermediate frequency (455kHz: AM IF).
35	2MO	Output terminal of Mixer 2. Second intermediate frequency (455kHz), generated by mixing first intermediate frequency (10.7MHz) and Second Local Oscillator is output.
36 37	2LOI 2LOI	Input terminal of second local oscillator. These pins generate 2'nd local oscillation frequency and are designed as colpitt type oscillator. 10.24MHz or 10.245MHz can be applied as for 2'nd local oscillator.
38	1MO	Output terminal of mixer 1. The signal from mixer 1 and the frequency of the first local oscillator are mixed to produce the first intermediate frequency, which is the output through this terminal. The output terminal is an emitter follower with an output impedance of 330Ω to match the 330Ω input / output impedance of the 10.7MHz ceramic filter.
39 40	1LOI 1LOI	Input terminal of the first local oscillator. The local oscillator is a voltage controlled oscillator. Local oscillation frequency and received frequency are mixed at mixer 1 and then converted to the first intermediate frequency of 10.7MHz or 10.695MHz.
41	VCO_{RX}	The terminal which variable capacitor is included in the chip. Used as an input terminal where 1st local oscillation frequency is changed by varying the capacitor connected between 1st local oscillator terminals. The internal variable capacitor has the value of 18.73 ~ 15.86 pF depending on the applied voltage. (1.0 ~ 2.0V)
42 43	1MI 1MI	Input terminal of Mixer1. This mixer is made of doubly balanced multiplier. The received signal amplified at RF AMP is input to this terminal.
44	$GND_{(PLL)}$	Ground. Ground for analog at PLL.
45	PDR	Phase detector output terminal of the receiver at PLL. If $f_{RX} > f_{REF}$ or f_{RX} is Leading $\rightarrow$ The output is negative pulse If $f_{RX} < f_{REF}$ or f_{RX} is Lagging $\rightarrow$ The output is positive pulse If $f_{RX} = f_{REF}$ and the same phase $\rightarrow$ The output is high impedance
46	$V_{REF(RF)}$	An internal PMOS pass transistor provides power supplier for the RF pre amplifier. PMOS pass transistor is on in Active/Rx mode and off in Standby/Inactive mode.
47	$V_{REF(PLL)}$	PLL voltage reference output pin. An internal voltage regulator provides a stable power supply voltage for the RX and TX PLLs. (2.05V)
48	TIF	Input terminal of TX channel counter. AC coupling with TX VCO. Minimum input level is 300 mVp-p (at 60MHz).

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage	Vcc	5.5	V
Power Dissipation	P_D	600	mW
Operating Temperature	T_{OPR}	–20 — + 70	°C
Storage Temperature	T_{SCG}	–55 — + 150	°C

CURRENT CONSUMPTION AT EACH MODE (VCC = 3.6V)

Modes	Min.	Typ.	Max.
Active mode (Communication mode)	–	8.9mA	–
RX mode	–	4.8mA	–
Stand-by mode	–	700uA	–
Inactive mode (Battery Saving Mode)	–	50uA	70uA

CURRENT CONSUMPTION IN EACH BLOCK (VCC = 3.6V)

Modes		Min.	Typ.	Max.
Receiver part		–	3.5mA	4.6mA
Expander part		–	0.8mA	1.1mA
Speaker part		–	1.0mA	1.4mA
compressor part		–	1.7mA	2.1mA
PLL	RX part	–	1.2mA	1.6mA
	TX part	–	0.7mA	1.1mA
Total		–	8.9mA	11.9mA

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	Vcc	–	2.0	–	5.5	V
RECEIVER (V_{CC} = 3.6V, f_C = 49.7MHz, f_{DEV} = ± 3kHz, f_{MOD} = 1kHz,Ta = 25°C, unless otherwise specified)						
Sensitivity (input for 12dB SINAD)	V_{SEN}	MIX1 Matched Impedance Input	–	0.7	2.0	µVrms
Input for -3dB Limiting	V_{LIM}	MIX1 Matched Impedance Input	–	0.7	2.0	µVrms
S/N Ratio	S/N	RFin = 1mVrms	48	55	–	dB
Recovered Audio Output	$V_{O(RA)}$	RFin = 1mVrms, After 2nd stage LPF	147	177	207	mVrms
Recovered Audio Output Voltage Drop	$V_{O(RAD)}$)	Vcc = 5.5V → 2.0V RFin = 1mVrms	–3.0	–1.5	–	dB
Detector Output Resistance	$R_{O(DET)}$	RFin = 1mVrms	–	1.2	–	KΩ
Detect Output Voltage	$V_{O(DET)}$	RFin = 1mVrms	1.0	1.5	2.0	V
Detector Output Distortion	THD_{DET}	RFin = 1mVrms (with CCITT Filter)	–	1.0	2.5	%
Comparator Threshold Voltage Difference	ΔV_{TH}	V_{COMP} = 360mVp-p R_{HYS} = 180KΩ	70	110	150	mV
Comparator Output Voltage 1	V_{OH}	V_{COMP} =360mVp-p R_{HYS} = 180kΩ	Vcc-0.4	–	–	V
Comparator Output Voltage 2	V_{OL}	V_{COMP} = 360mVp-p R_{HYS} = 180kΩ	–	0.1	0.4	V
First Mixer Conversion Voltage Gain	$\Delta G_{V(1M)}$	$V_{MIX1\ 1/2}$ = 1mVrms R_L = 330kΩ	12	15	18	dB
Second Mixer Conversion Voltage Gain	$\Delta G_{V(2M)}$	V_{MIX2} = 1mVrms R_L = 1.5kΩ	18	22	26	dB
Demodulator Bandwidth	DBW	RFin = 1mVrms	–	10	–	kHz
Limiter Input Sensitivity	$V_{I(LIM)}$	Fc = 455kHz , –3dB Limiting	–	20	40	uVrms
AM Rejection Ratio	AMRR	RFin = 1mVrms AM MOD = 30% @1kHz	–	40	–	dB
First Mixer 3rd Order Intercept Point	IMD3	MIX1 Input 50Ω Termination	–	– 15	–	dBm
First Mixer Input Impedance	$R_{I(1M)}$ / $C_{I(1M)}$	Fc = 50MHz	–	690 7.2	–	Ω pF
First Mixer output Impedance	$Ro_{(1M)}$	Fc = 10.7MHz	–	330	–	Ω

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Second Mixer input Impedance	$R_{I(2M)}$	Fc = 10.7MHz	–	4	–	kΩ
Second Mixer output Impedance	$Ro_{(2M)}$	Fc = 455kHz	–	1.5	–	kΩ
Carrier Detector Threshold	CD_{TH}	MIX1 Single-Ended Matching, Default Threshold=1010	–	–95	–	dBm
Low Battery Detector	LBD	LBD0 ~ LBD3 = 0 (Default) Only LBD2 = 0 Only LBD1 = 0 Only LBD3 = 0	– 0.15	3.45 3.3 3.0	0.1	V
		LBD0 ~ LBD3 = 1	–0.1	2.2 2.1	0.075	
RSSI Slope	V_{RSSI}	MIX1 Single-Ended Matching	–	30	–	mV/dB
RSSI Output Voltage Dynamic Range	RSSI	MIX1 Single-Ended Matching	–	60	–	dB
Carrier Detect Output High Voltage	V_{OH}	RFin = 1μVrms Default Threshold = 1010	Vcc-0.4	–	–	V
Carrier Detect Output Low Voltage	V_{OL}	RFin = 10μVrms Default Threshold = 1010	–	–	0.4	V
COMPRESSOR (Vcc = 3.6V, fc = 1kHz, Ta = 25°C, unless otherwise specified)						
Standard Output Voltage	Vo(com)	Vinc = 63.2mVrms → 0dB ALC disabled (pin 13)	269	316	363	mVrms
Compressor Gain Difference	$\Delta G_{V1(COM)}$	Vinc = –20dB	–10	0	1.0	dB
	$\Delta G_{V2(COM)}$	Vinc = –40dB	–1.5	0	1.5	dB
Compressor Output Distortion	THD_{COM}	Vinc = 63.2mVrms → 0dB	–	0.5	1.0	%
Mute Attenuation Ratio	ATT_{MUTE}	Vinc = 0dB	60	80	–	dB
Compressor Limiting Voltage	$V_{LIM(COM)}$	Vinc = Variable	1.05	1.35	1.65	Vp-p
ALC	VALC	R_{ALC} = 150kΩ, Vinc = 10dB	310	390	450	mVrms
Splatter filter	Vo(SF)	V_{INC} = 63.2mVrms → 0 dB	269	316	363	mVrms
Maximum Output Voltage	$V_{OMIC(MAX)}$	RL = 10KΩ	–	2.8	–	Vp-p
EXPANDER (Vcc = 3.6V, fc = 1kHz, Ta = 25°C, unless otherwise specified)						
Standard Output Voltage	$V_{O(EXP)}$	Vin_E = 63.2mVrms → 0dB	***309***	***356***	***403***	mVrms

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Expander Gain Difference	$\Delta G_{V1(EXP)}$	Vin_E = –10dB	–1.0	0	1.0	dB
	$\Delta G_{V2(EXP)}$	Vin_E = – 20dB	–1.5	0	1.5	dB
	$\Delta G_{V3(EXP)}$	Vin_E =– 30dB	–2.0	0	2.0	dB
Expander Output Distortion	THD_{EXP}	Vin_E = 63.2mVrms → 0dB	–	0.5	1.0	%
Mute Attenuation Ratio	ATT_{MUTE}	Vin_E = 63.2mVrms → 0dB	60	80	–	dB
Expander Maximum Output Voltage	$V_{OEXP(MAX)}$	Vin_E = Variable THD = 10%	800	–	–	mVrms
Maximum Output Voltage	$V_{OSPK(MAX)}$	R_L = 150Ω	–	2.2	–	Vp-p
		RL = 600Ω	–	3.0	-	Vp-p
Input Current	I_{IH}	Vin = Vcc	–	–	5	µA
	I_{IL}	Vin = 0V	–5	–	–	µA
Input Voltage	V_{IH}	–	Vcc-0.3	–	–	V
	V_{IL}	–	–	–	0.3	V
Output Current	I_{OH}	Vout = Vcc	0.3	–	–	mA
	I_{OL}	Vout = 0V	0.3	–	–	mA
Output Voltage	V_{OH1}	PDT,PDR: Io = -0.3mA (Sourcing)	Vcc-0.4	–	–	V
	V_{OL1}	PDT,PDR: Io = 0.3mA (Sinking)	–	–	0.4	V
	V_{OH2}	LD,f_{MCU}: Io = – 0.1mA (Sourcing)	Vcc-0.5	–	–	V
	V_{OL2}	LD,f_{MCU}: Io = 0.1mA (Sinking)	–	–	0.5	V
PLL regulator voltage	V_{PLLREG}	–	1.90	2.05	2.20	V
Regulator Load Current	I_{REG}	Vout = V_{REG}(OPEN)-0.05V	–	3.0	–	mA

PLL PROGRAM SUMMARY

- MCU (MICOM) Serial Interface (MSB : 1st INPUT)
  Use CLK (Pin 7), DATA (Pin 8) , and EN (Pin 9) terminals for program.
  DATA and CLK terminals are used for loading data to internal Shift - Register. When EN terminal is 'Low', It is possible to program TX-Channel Counter, RX - Channel Counter and various control functions of PLL. When EN terminal is 'High', Program 1st Local Oscillator Capacitor Selection in receiver for U.S.A - 25 CH function.

— TX - Register, RX-Register, Control Register

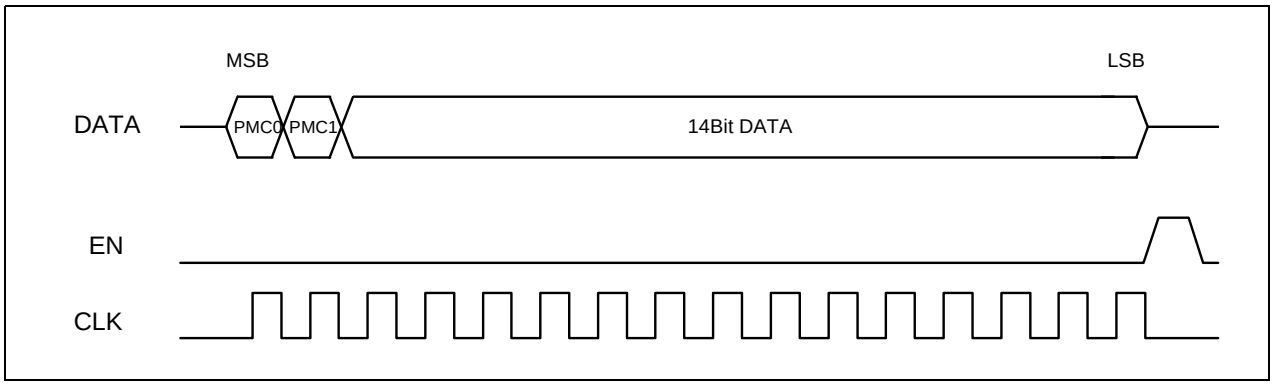


Figure 1.

— Reference - Register

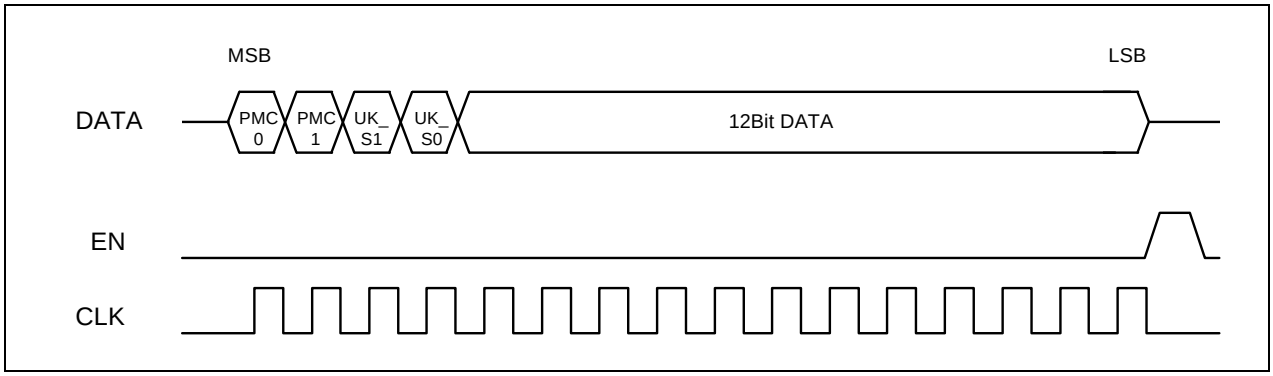


Figure 2.

— Auxiliary - Register(16bits)

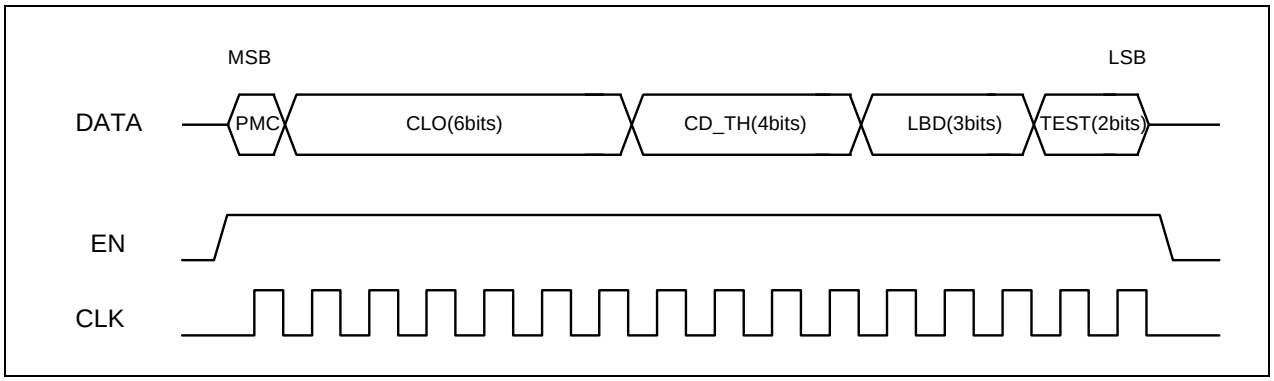


Figure 3.

- **Programmable Counter**

— RX - counter: Setting frequency for RX.VCO (14 Bits --> 1/16 ~ 1/16383)
[Default_CH. = USA_#21 (REMOTE) : 36.075MHz (Div._NO = 7215)]

< RX. Register (16bits) >

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC1	D13	D12	D11	D10	D9	D8
Default value 7215	*		0	1	1	1	0	0

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default value 7215	0	0	1	0	1	1	1	1

— TX - counter: Setting frequency for TX.VCO (14 Bits --> 1/16 ~ 1/16383)
[Default_CH. = USA_#21 (REMOTE) : 49.830MHz (Div._NO = 9966)]

< TX. Register (16 bits) >

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC1	D13	D12	D11	D10	D9	D8
Default value 9966	*		1	0	0	1	1	0

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Default value 9966	1	1	1	0	1	1	1	0

* Program Latch Assignl

PMC0 (Bit15)	PMC1 (Bit14)	Register Assign
0	0	Control
0	1	UPLL_Rx
1	0	UPLL_Ref
1	1	UPLL_Tx

— Ref - counter: Setting reference frequency for phase detector (12 Bits --> 1/16 ~ 1/4095)
[Default_Divider = 2048, X-tal_OSC = 10.240 MHz -->Fref = 5KHz]< Ref. Register (16bits) >

< Ref. Register (16bits) >

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC1	UK_S1	UK_S0	D11	D10	D9	D8
Default value 2048	*		Ref.freq. selection for United Kingdom		1	0	0	0

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	D7	D6	D5	D4	D3	fMCU_M	FMCU1	FMCU0
Default value 2048	0	0	0	0	0	MPU CLK Mute	MPU CLK CNTl_1	MPU CLK CNTL_0

— UK_Selection

UK_S0	UK_S1	FR1	FR2	FrefTX	FrefRX
0	0	fREF (A)	–	fREF (A)	fREF (A)
1	0	fREF (A)	fREF/4 (B)	fREF/4 (B)	fREF/4 (B)
0	1	fREF/4 (B)	fREF/25 (C)	fREF/4 (B)	fREF/25 (C)
1	1	fREF/4 (B)	fREF/25 (C)	fREF/25 (C)	fREF/4 (B)

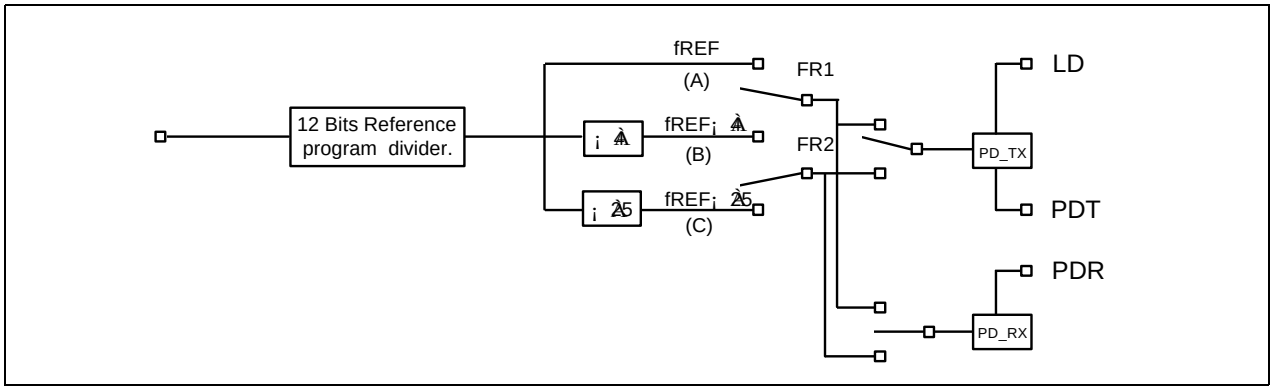


Figure 4. Reference frequency selection

- **Control program**

Control register (16 Bits)

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC0	PMC1	BS1	BS0	LBD_BS	CO_M	EX_M	SPK_M
Description	Program Mode Control_0	Program Mode Control_1	Power Save Control_1	Power Save Control_0	Low Battery Detector Battery Save	Compressor Mute	Expander Mute	Speaker Mute
Function	* Program Latch Assign		** Power Save Mode		0:Normal (LBD-On) 1:LBD-Part Power-Off	0: Normal 1: Mute	0:Normal 1:Mute	0:Nomal 1:Mute

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SPK3	SPK2	SPK1	SPK0	LDT/CDO	fMCU_M	fMCUS1	fMCUS0
Description	SPK Control_3	SPK Control_2	SPK Control_1	SPK Conrol_ 0	LDT/CDO Select	MCU Clock Mute	MCU Clock Control_1	MCU Clock Control_0
Function	Speaker Volume Control				0: CDO 1: LDT	0: Normal 1: Mute	*** MCU Clock Output	

** Power Save Mode Assign

BS1 (Bit13)	BS0 (Bit12)	Power Save Mode	
0	0	Rx	Default
0	1	Active	
1	0	STD_By	
1	1	Inactive	

*** MCU Clock Output Control & Frequency

fMCU_M	fMCUS1	fMCUS0	Clock Output Divider
1	Don't Care	Don't Care	Low
0	0	0	2
0	0	1	3
0	1	0	4
0	1	1	5 (Default)

X-tal / Divider	10.24MHz	11.15MHz	12.0MHz
2	5.120MHz	5.575MHz	6.0MHz
3	3.413MHz	3.717MHz	4.0MHz
4	2.560MHz	2.788MHz	3.0MHz
5	2.048MHz	2.230MHz	2.4MHz

*** Speaker Amplifier Volume Control

DATA				Gain/Attenuation	Output Level [SAO1-SAO2]
SPK3	SPK2	SPK1	SPK0		
0	0	0	0	–18dB	25mVrms
0	0	0	1	–16dB	–
0	0	1	0	–14dB	–
0	0	1	1	–12dB	50mVrms
0	1	0	0	–10dB	–
0	1	0	1	–8dB	–
0	1	1	0	–6dB	100mVrms
0	1	1	1	–4dB	–
1	0	0	0	–2dB	–
1	0	0	1	0dB	200mVrms
1	0	1	0	+2dB	–
1	0	1	1	+4dB	–
1	1	0	0	+6dB	400mVrms
1	1	0	1	+8dB	–
1	1	1	0	+10dB	–
1	1	1	1	+12dB	800mVrms

- **Auxiliary Register (16 Bits)**

Auxiliary Register Function

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	PMC	CLO5	CLO4	CLO3	CLO2	CLO1	CLO0	CD_TH3
Description	Auxiliary register Selection	***Cap=5.9p***	***Cap=4.8p***	***Cap=3.2p***	***Cap=1.6p***	***Cap=1.3p***	***Cap=0.8p***	CD_TH Control_3
Function	***** Program Mode Control	1'st LO Cap Select						CD Control_3

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CD_TH2	CD_TH1	CD_TH0	LBD3	LBD2	LBD1	TEST2	TEST1
Description	CD_TH Control_2	CD_TH Control_1	CD_TH Control_0	LBD Control_3	LBD Control_2	LBD Control_1	TEST Mode2	TEST Mode1
Function	Carrier Detector Threshold Control			Low Battery Detector Voltage Control			**** TEST Mode & LDT-CDO Mode	

**** TEST Mode & LDT-CDO Mode

LDT/CDO	TEST1	TEST2	LDT / CDO	Remark
0	0	0	Rx block CDO	Default
	1	0	Rx block CDO	–
	0	1	4_25cnt block FR2	–
	1	1	4_25cnt block FR2	–
1	0	0	PLL block LDT	–
	1	0	PLL block LDT	–
	0	1	Test PLL_RX	–
	1	0	Test PLL_TX	–

**** Carrier Detector Threshold Control

DATA				Carrier Detector Threshold
CD_TH3	CD_TH2	CD_TH1	CD_TH0	
0	0	0	0	–20dB
0	0	0	1	–18dB
0	0	1	0	–16dB
0	0	1	1	–14dB
0	1	0	0	–12dB
0	1	0	1	–10dB
0	1	1	0	–8dB
0	1	1	1	–6dB
1	0	0	0	–4dB
1	0	0	1	–2dB
1	0	1	0	0dB (Default)
1	0	1	1	+2dB
1	1	0	0	+4dB
1	1	0	1	+6dB
1	1	1	0	+8dB
1	1	1	1	+10dB

- **Operating internal circuit blocks in each mode**

Mode (state)	Operating circuit blocks
Active state (Communication mode)	PLL regulator / MICOM I/F (Data, CLK, EN) / 2nd local oscillator / Receiver/ 1st local oscillator/ RX PLL/ Carrier detector / FSK comparator / Low battery detector / TX PLL / Expander & speaker amp / Compressor /Splatter filter amp, Clock Output
Receiving mode	PLL regulator / MICOM I/F(Data, CLK, EN) / 2nd local oscillator / Receiver/ 1st local oscillator/ RX PLL/ Carrier detector / FSK comparator / Low battery detector, Clock Output
Stand-by mode (Battery Save Mode#2)	PLL regulator, MICOM I/F (Data, CLK, EN), 2nd local oscillator, Clock Output
Inactive state (Battery Saving Mode#1)	Interrupt

- **Auxiliary Register(CLO_LBD Program)**
  [Rx - 1st local oscillation internal cap. for U.S.A - 25CH & low battery detecting voltage]

— CLO register (6 bits) : Receiver 1st local oscillator internal capacitor selection

Bit	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9
Name	PMC	CLO5	CLO4	CLO3	CLO2	CLO1	CLO0
Default Value 0	1 *****	0	0	0	0	0	0
Function	-	0:Normal 1:Internal Cap. for USA 25 Channel =***5.9pF***	0:Normal 1:Internal Cap. for USA 25 Channel = ***4.8pF***	0:Normal 1:Internal Cap. for USA 25 Channel = ***3.2pF***	0:Normal 1:Internal Cap. for USA 25 Channel =***1.6pF***	0:Normal 1:Internal Cap. for USA 25 Channel =***1.3p F***	0:Normal 1:Internal Cap. for USA 25 Channel = ***0.8pF***

***** PMC (Program Mode Control)
PMC = 'HIGH' & EN = 'HIGH' ---> Auxiliary Register Program Mode

— Rx-Low Battery Detect Voltage

Bit	Bit15 (MSB)	Bit 4	Bit 3	Bit 2	Low Battery Detector Voltage	Remark
Name	PMC	LBD3	LBD2	LBD1		
Default Value	1 *****	0	0	0	3.45V	Default
Function	1	1	0	1	3.3V	–
	1	1	1	0	3.0V	–
	0	0	1	1	2.2V	–
	1	1	1	1	2.1V	–

***** PMC (Program Mode Control)
PMC = 'HIGH' & EN = 'HIGH' ---> Auxiliary Register Program Mode

- **Example 1 >**
  Low battery detector voltage : 2.1V
  U.S.A _CH-#1 (REMOTE) ---> 1st local osc. varicap. value =15.86pF, ***Internal cap. = 9.3pF***
  (Ext_L = 0.45uH, EXT_C = 30pF)

— 16 bit data format

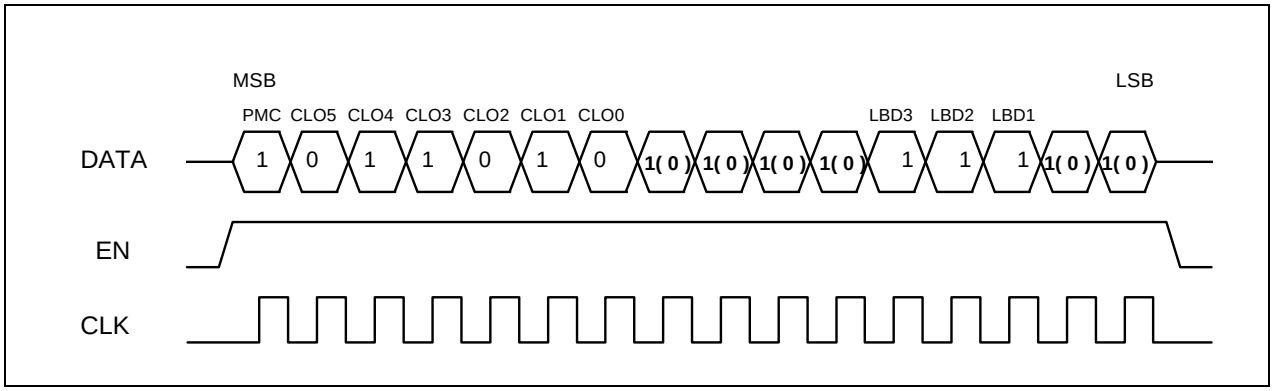


Figure 5.

- **Example data for U.S.A 25_channel selection**

1st Local Osc. Internal Capacitor Select						Base Channels	Hand Channels	Varicap Value	External C	External L	Internal C
Bit5 (CLO5)	Bit4 (CLO4)	Bit3 (CLO3)	Bit2 (CLO2)	Bit1 (CLO1)	Bit0 (CLO0)	1 ~ 25CH.	1 ~ 25CH.	1.0V~2.0V TYP 1.5V	27pF (30pF)	0.45uH	pF
0	0	0	0	0	0	16~25CH.		18.73 ~15.86pF	27pF	0.44uH	-
0	0	0	0	0	1	-	16~25CH.	18.73 ~15.86pF	***47pF***	0.20uH	***0.8***
0	0	0	0	1	1	01~04CH.		18.73 ~15.86pF	27pF	0.44uH	***2.1***
0	0	0	1	0	0	05~10CH.		18.73 ~15.86pF	27pF	0.44uH	***1.6***
0	0	0	0	0	1	11~15CH.		18.73 ~15.86pF	27pF	0.44uH	***0.8***
0	1	1	0	1	0	-	01~06CH.	18.73 ~15.86pF	***47pF***	0.20uH	***9.3***
0	1	0	1	1	0	-	07~15CH.	18.73 ~15.86pF	***47pF***	0.20uH	**8.8**

Phase detector / Lock Detector Output Waveforms

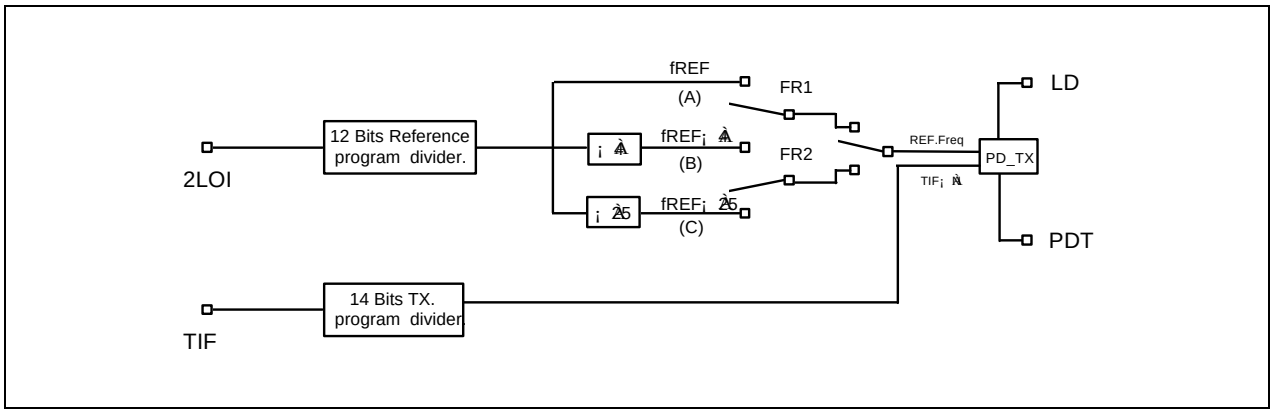


Figure 6.

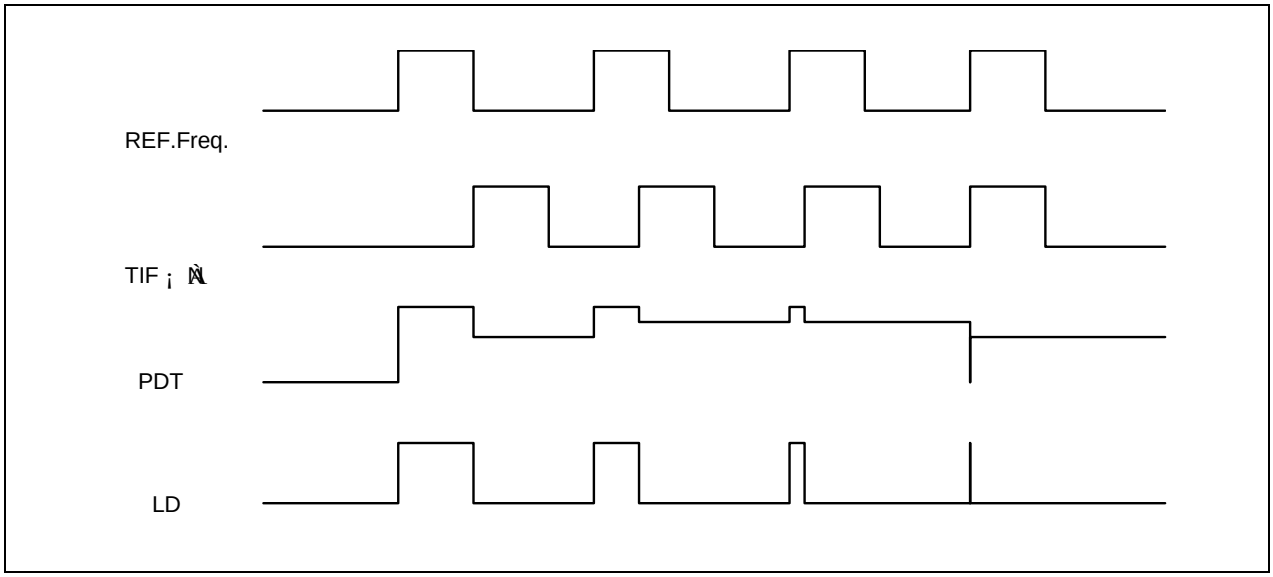
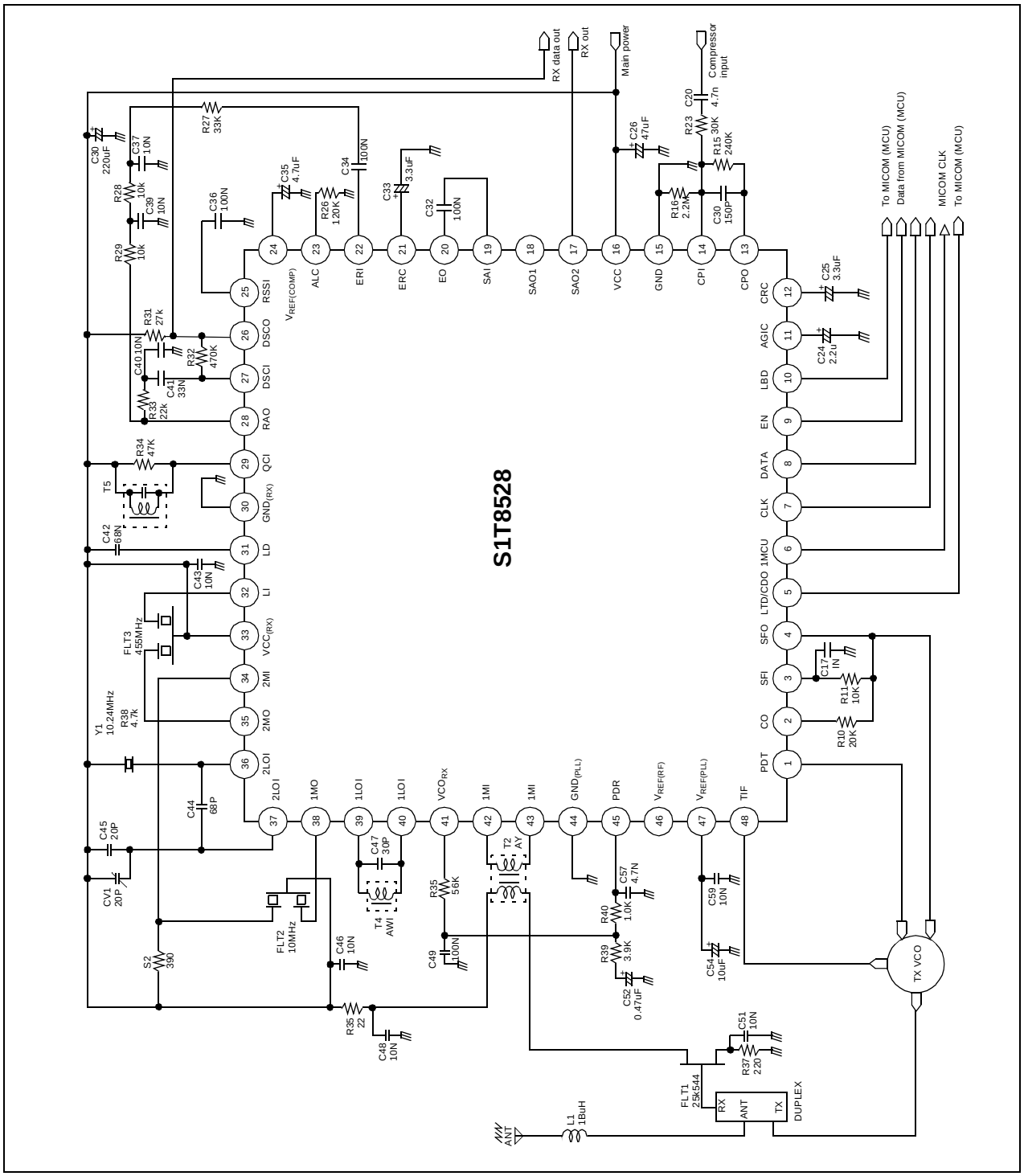
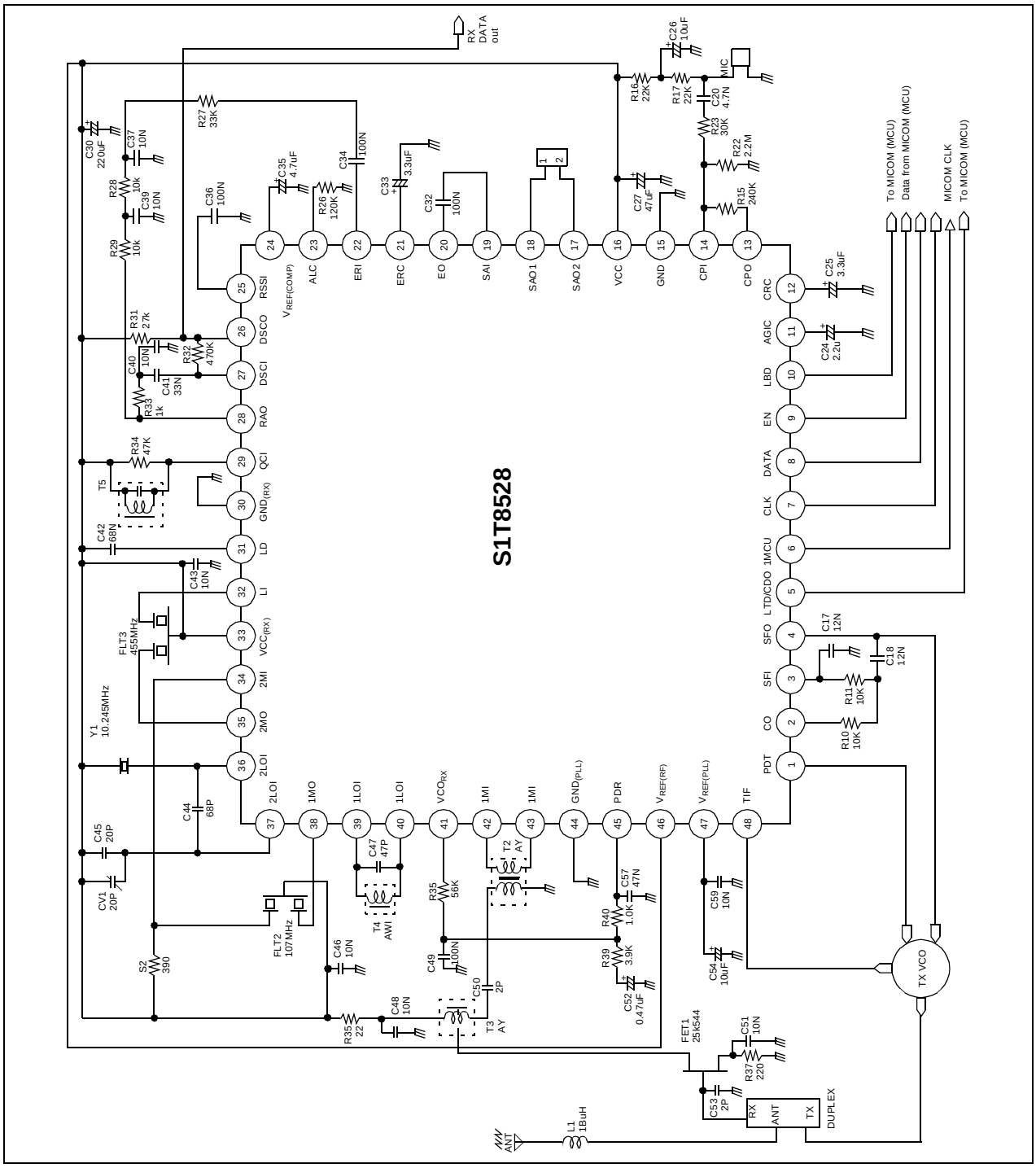


Figure 7. Phase Detector / Lock Detector Output Waveform

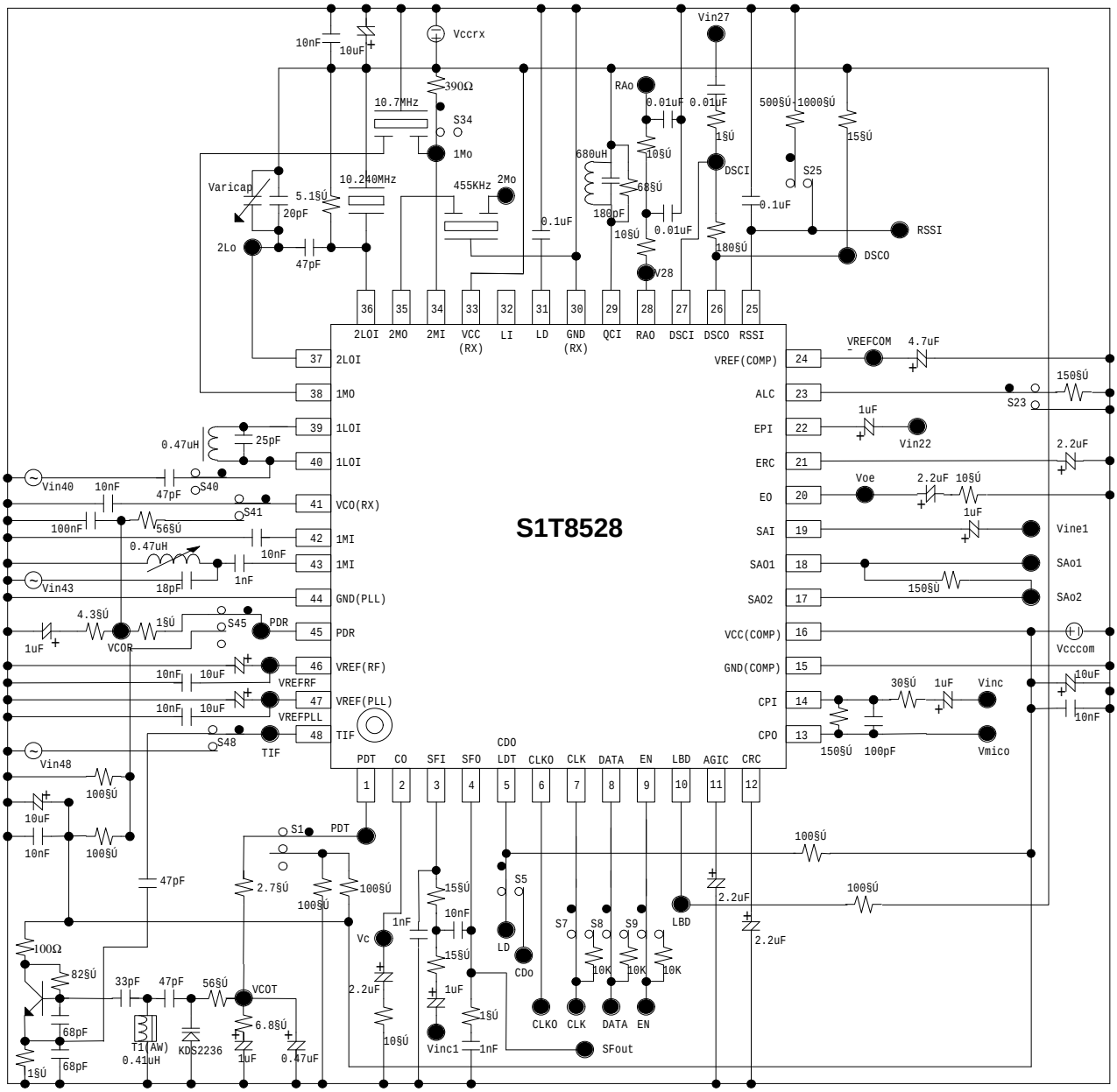
APPLICATION CIRCUIT (BASE SET)

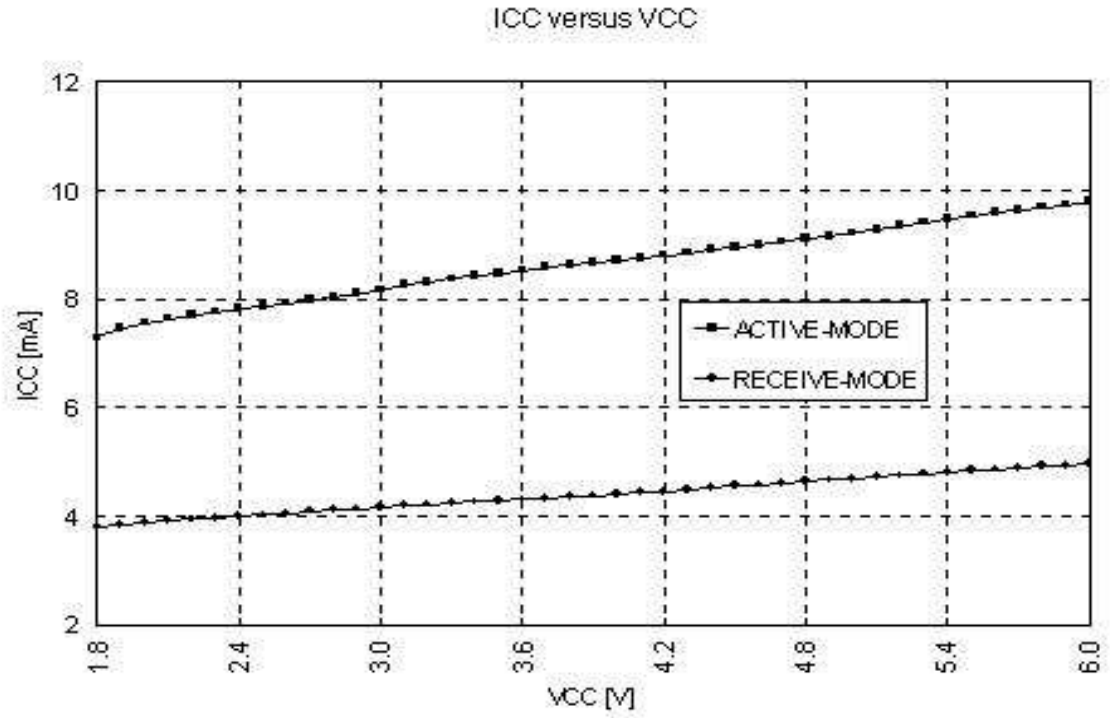


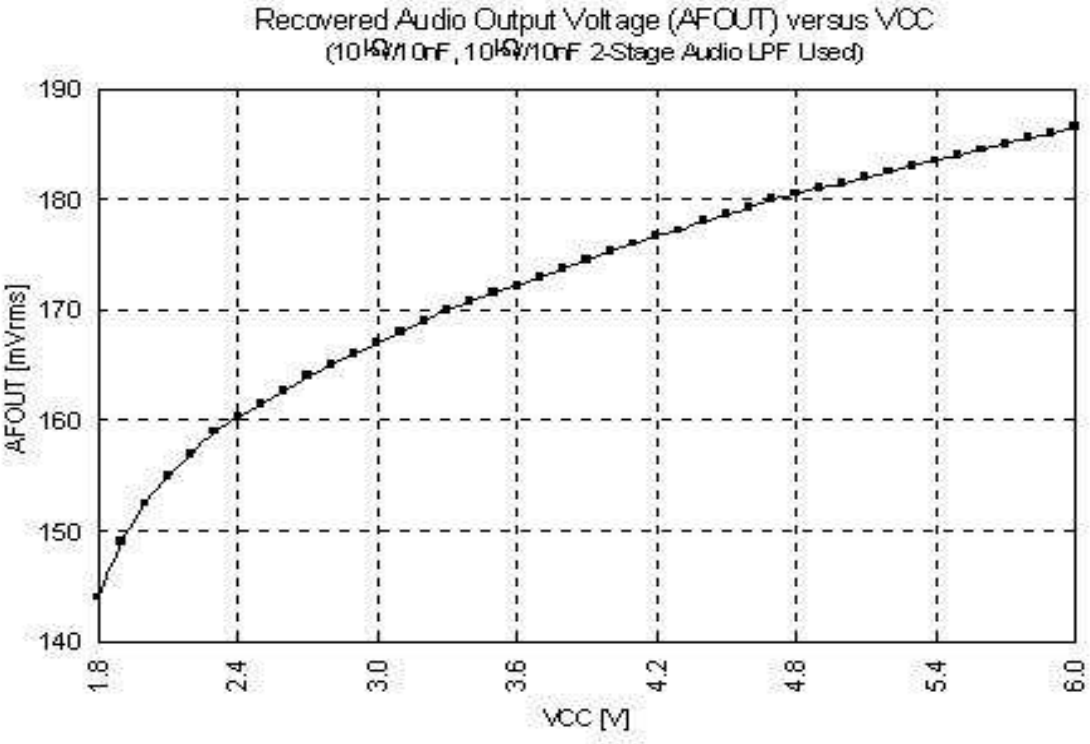
APPLICATION CIRCUIT (HAND SET)

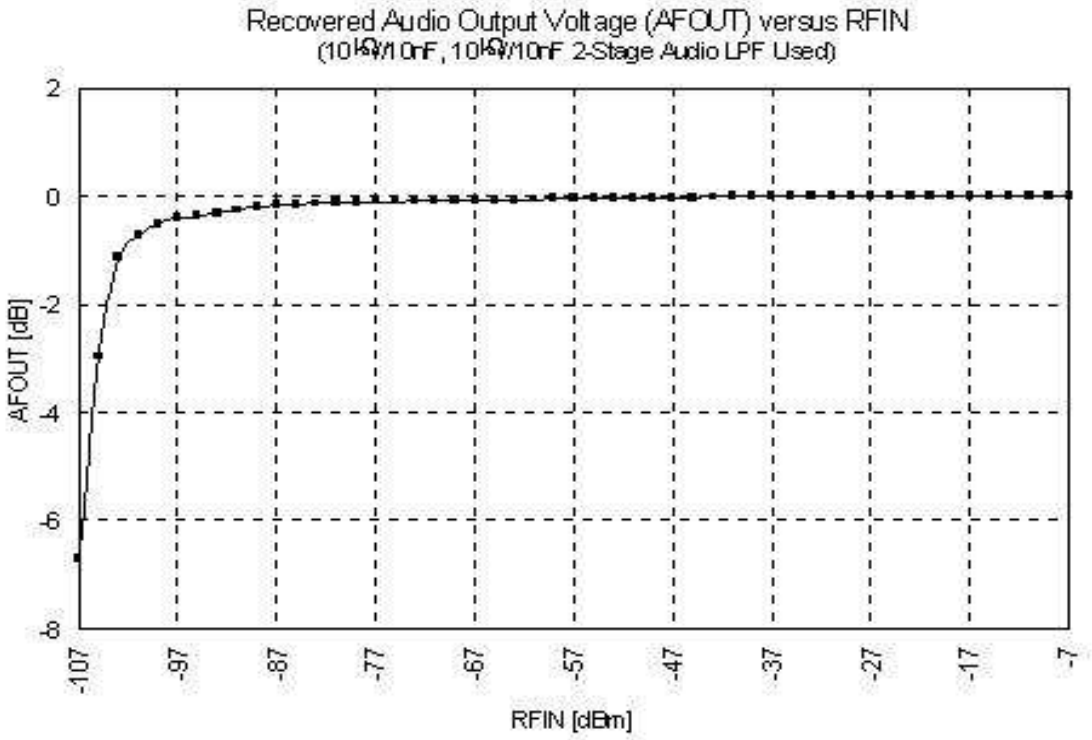


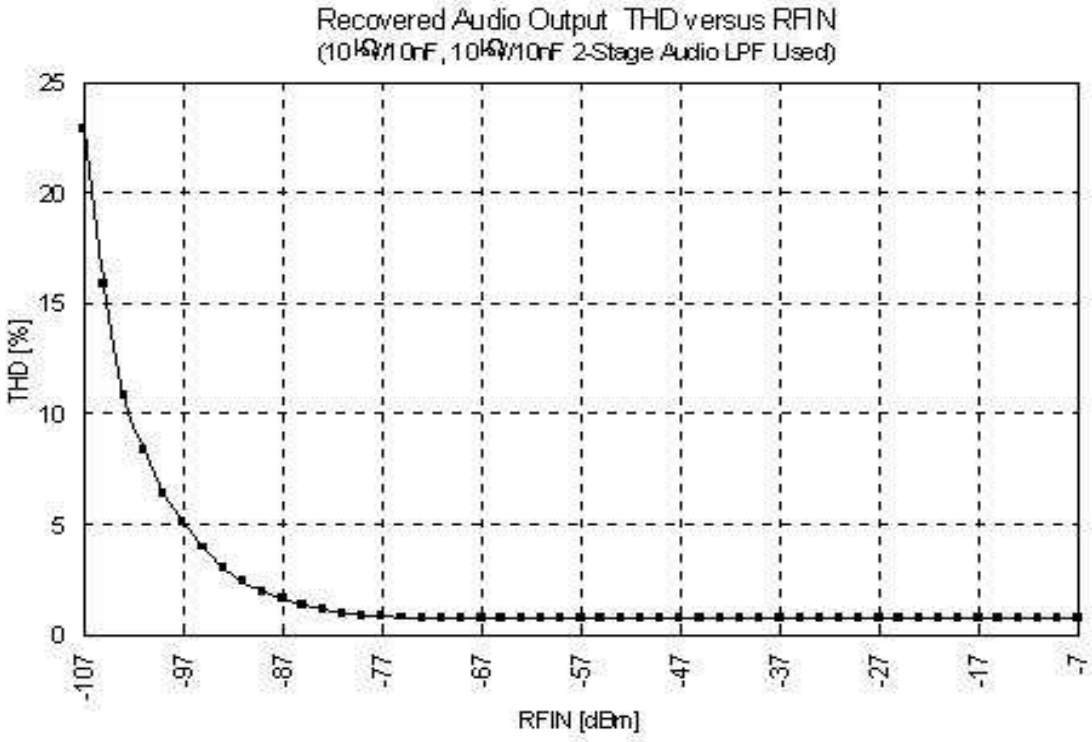
TEST CIRCUIT

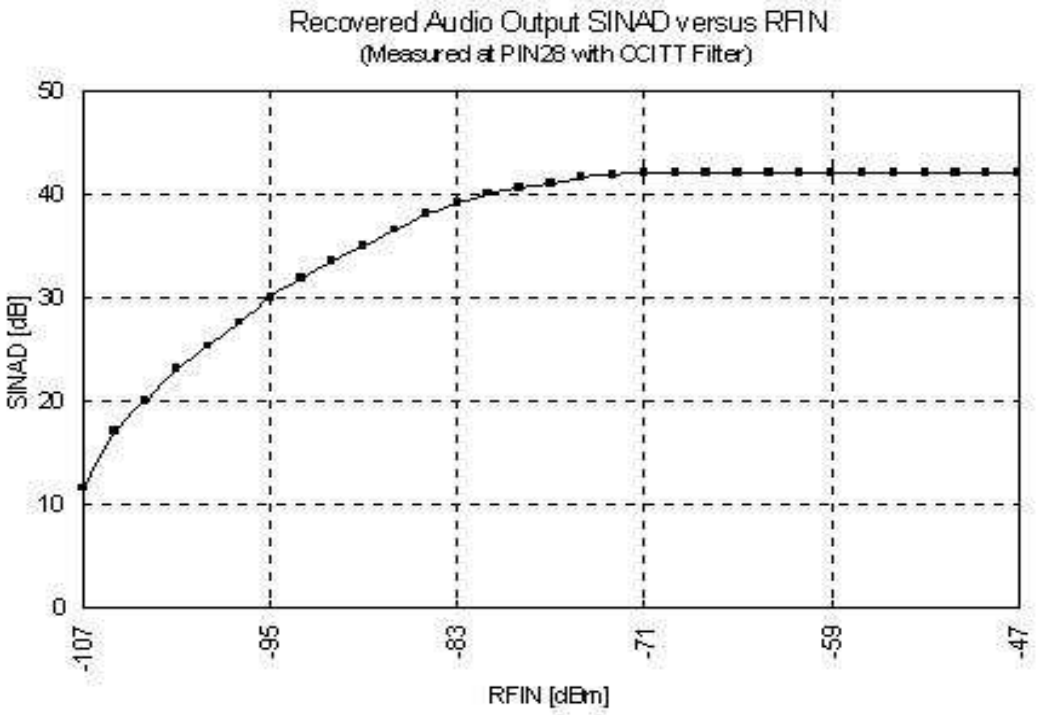


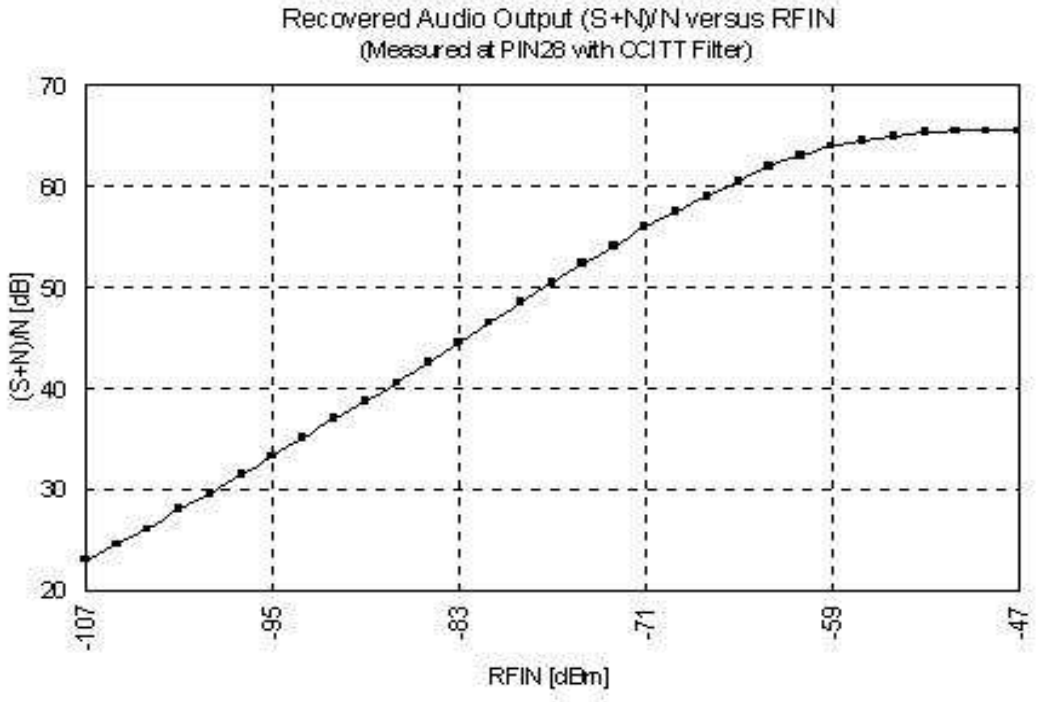


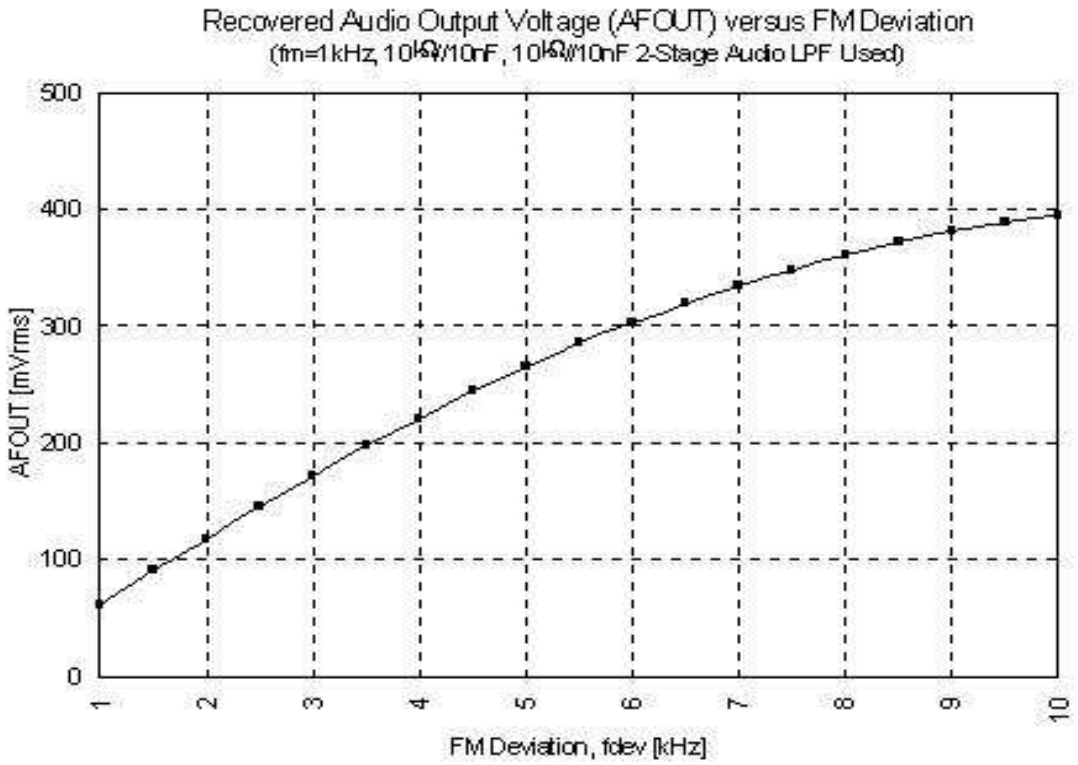


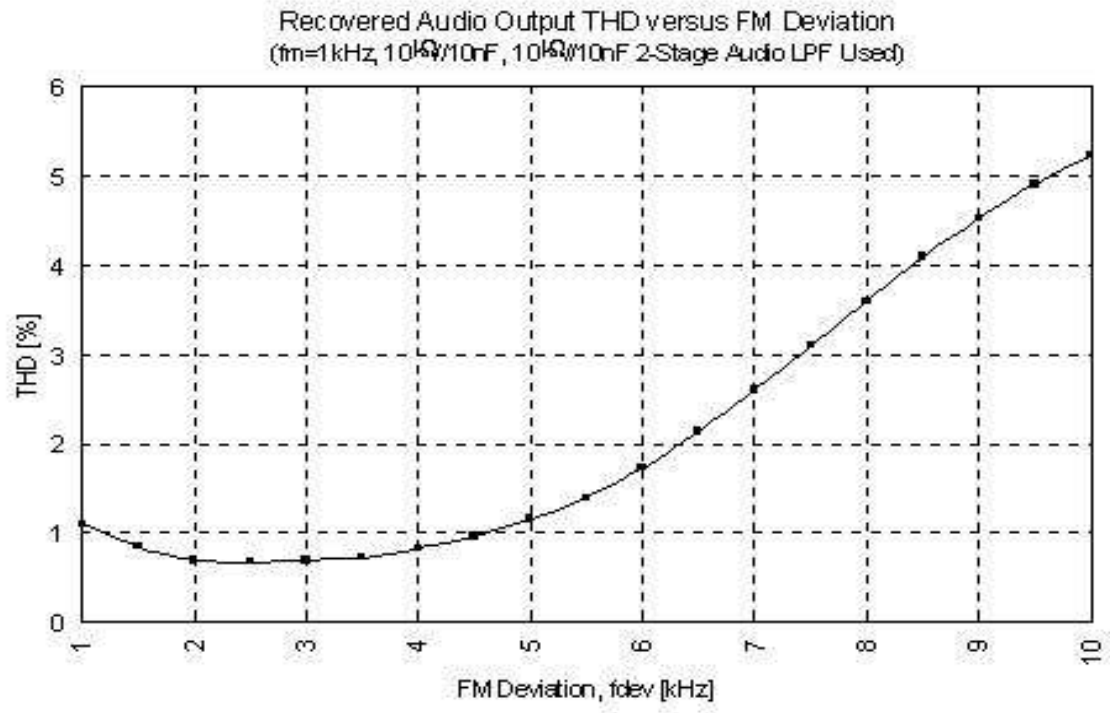


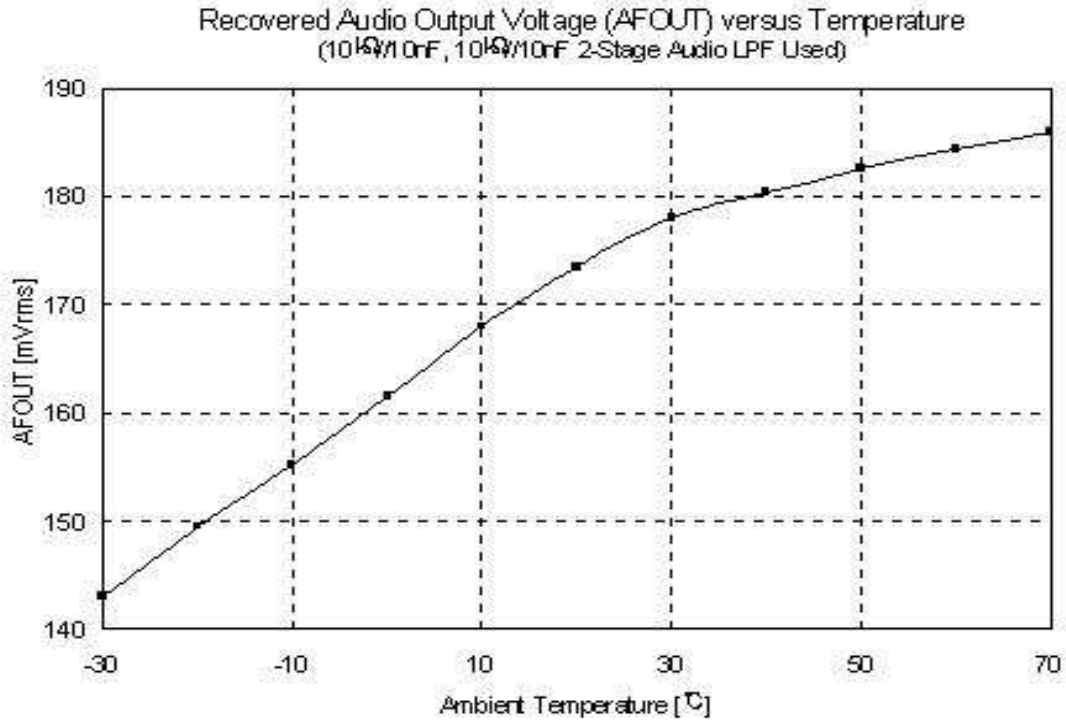


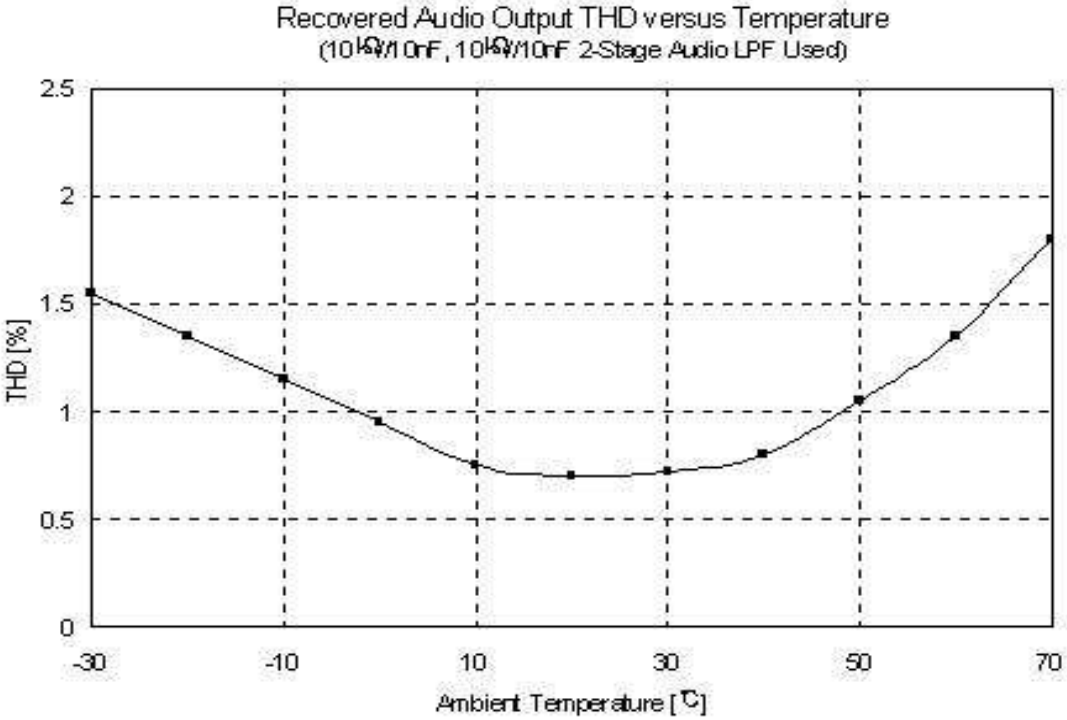




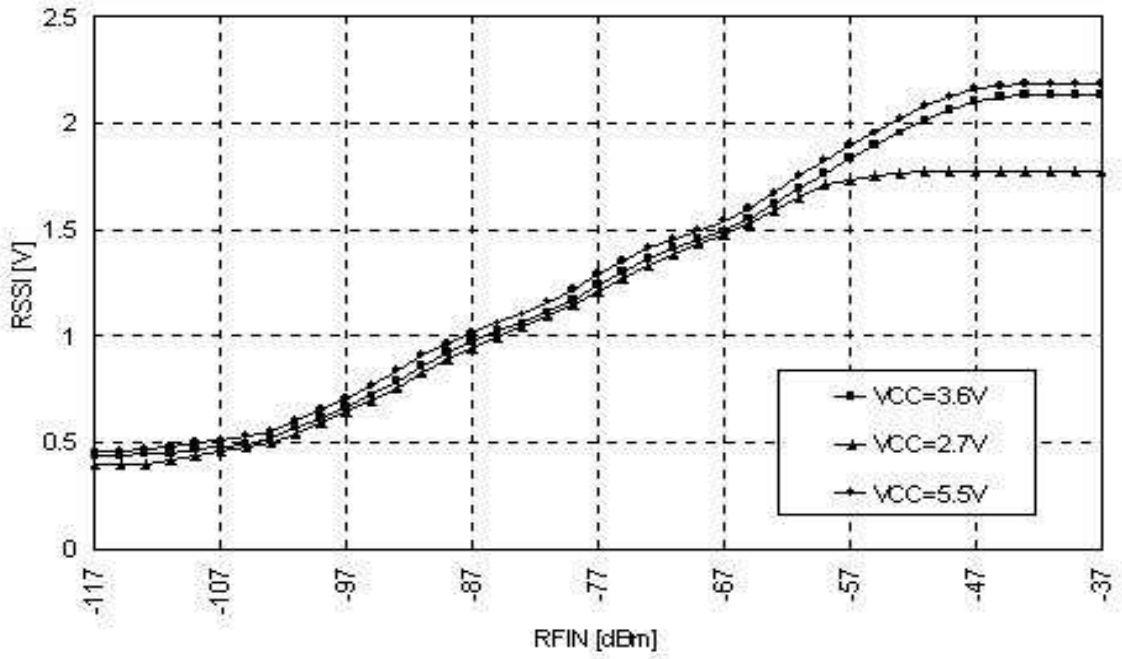




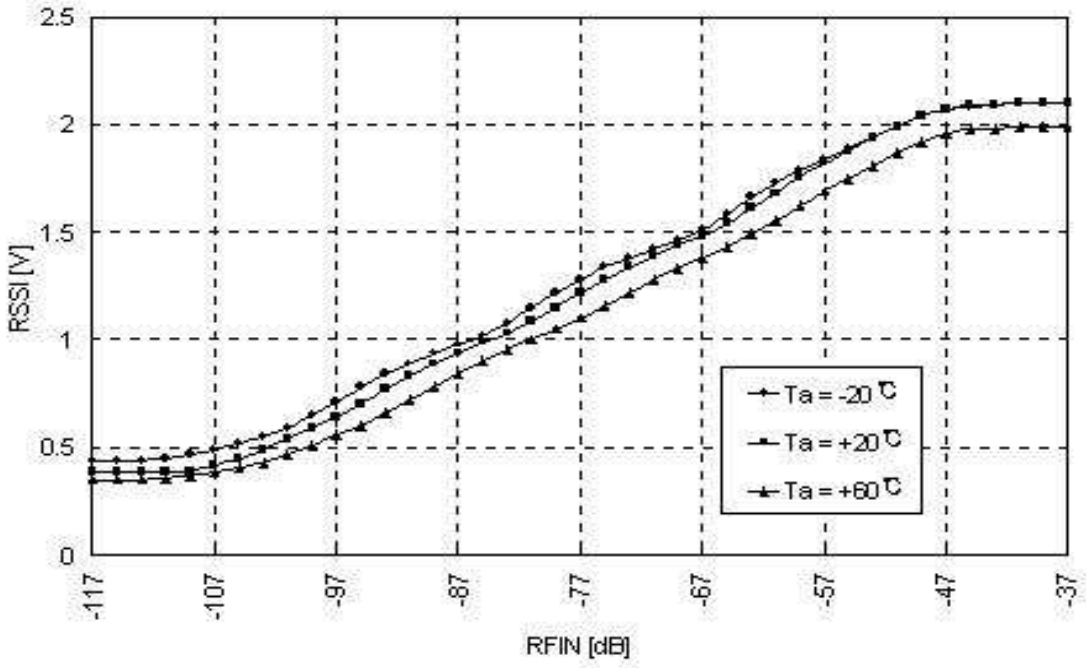


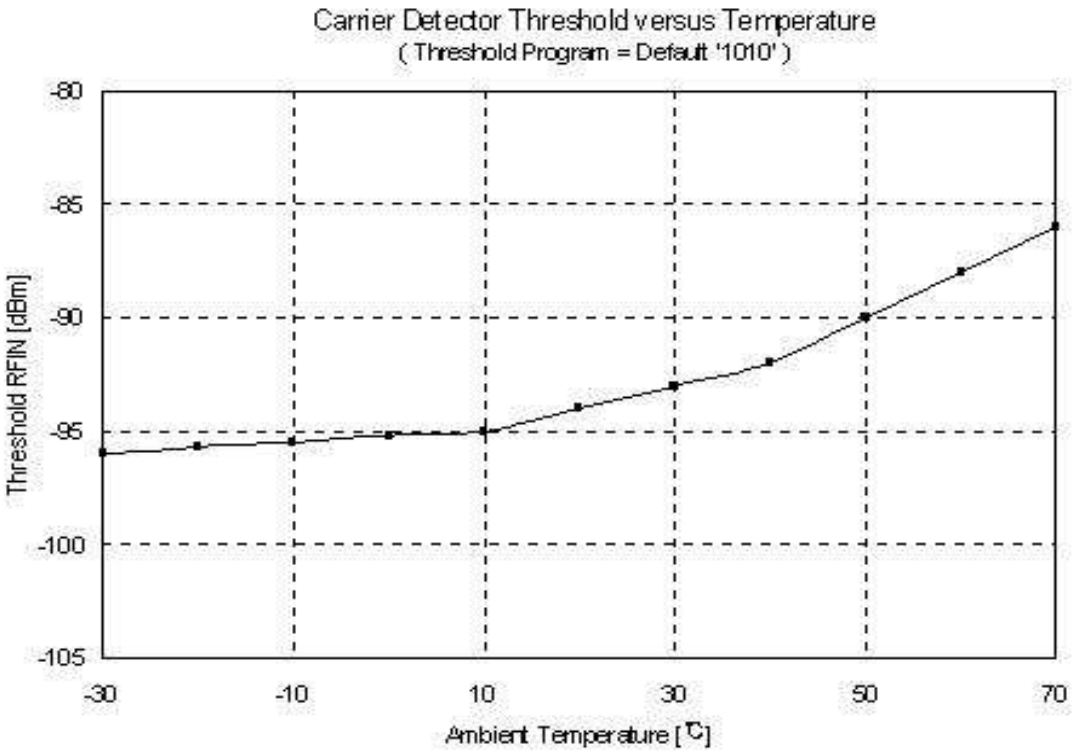


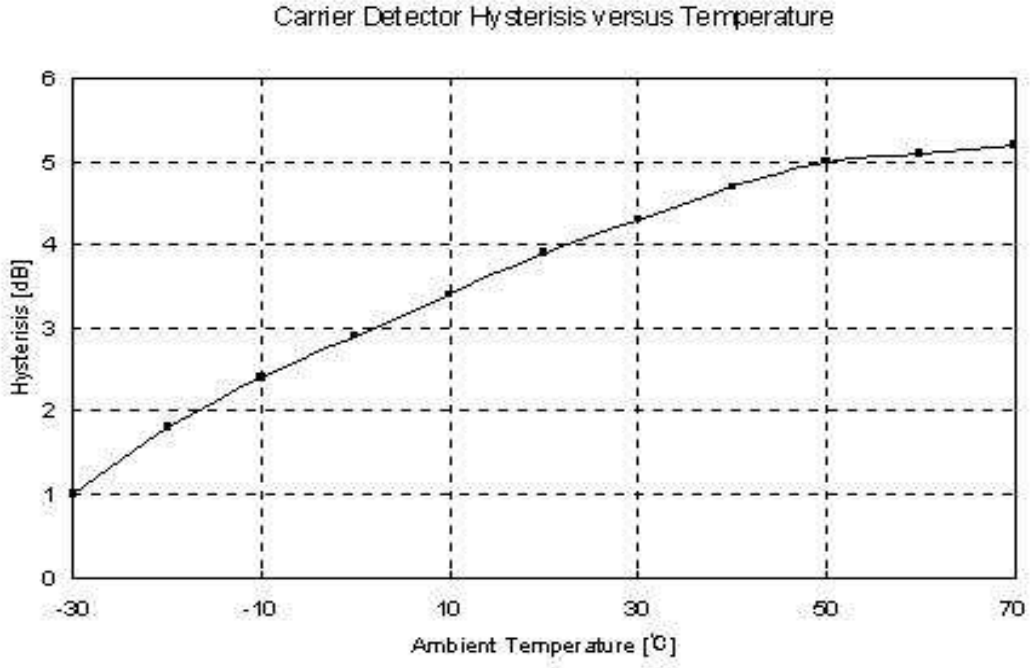
Analog RSSI versus RFIN and VCC

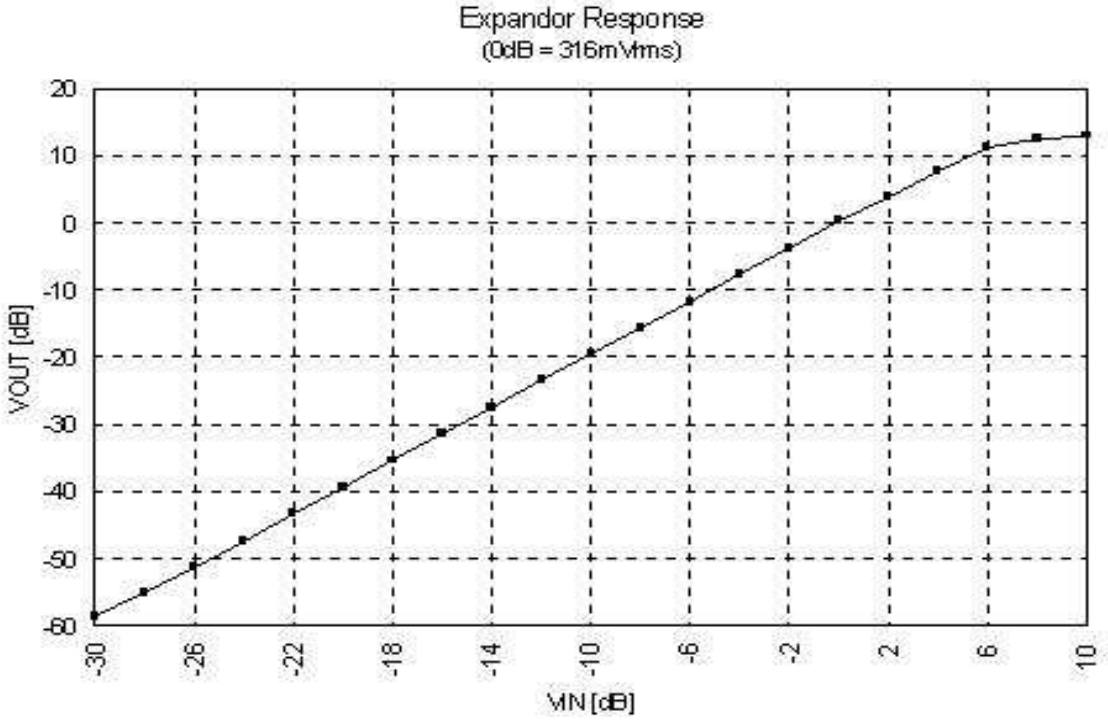


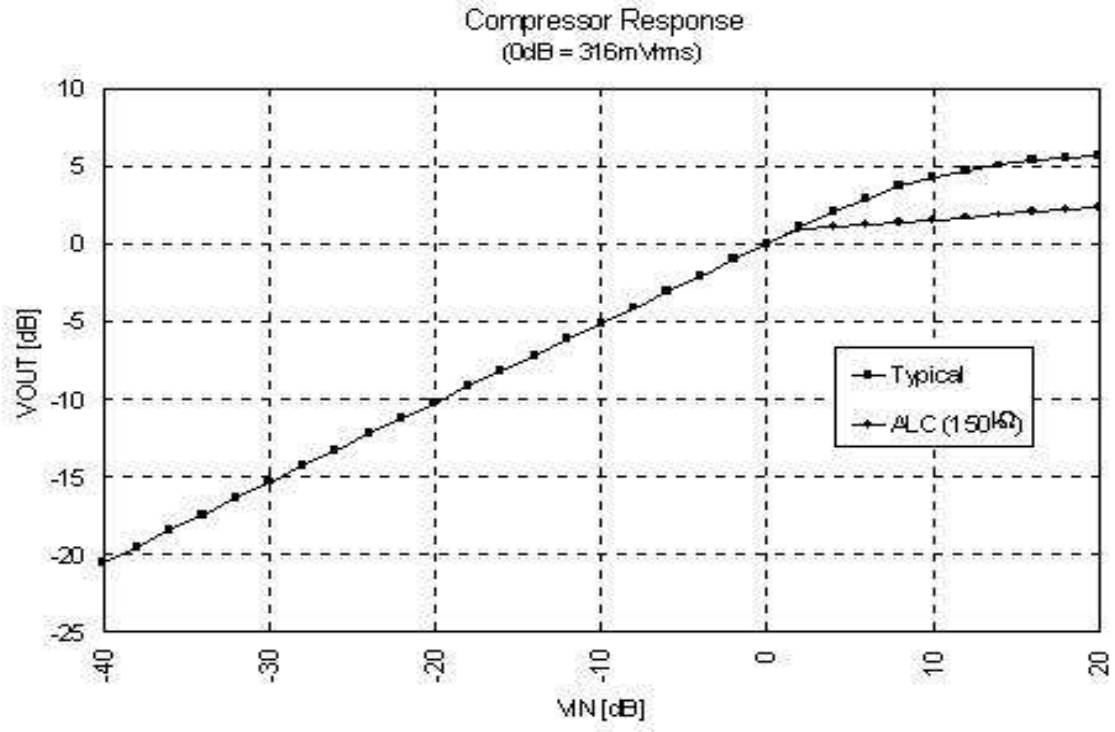
Analog RSSI versus RFIN and Temperature

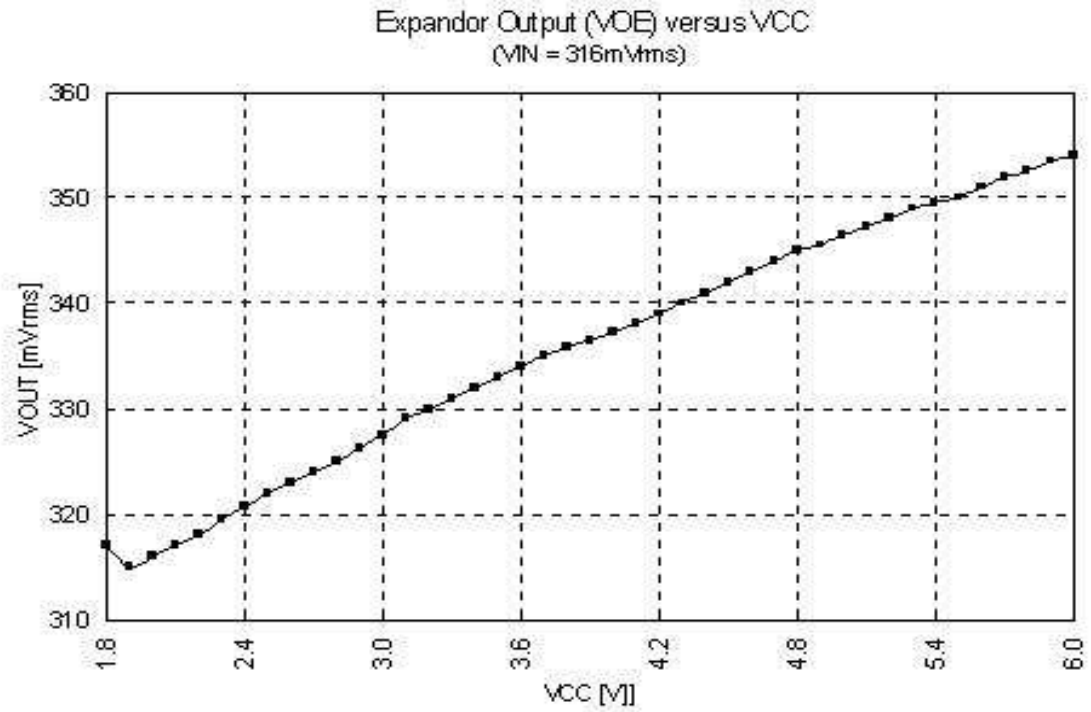


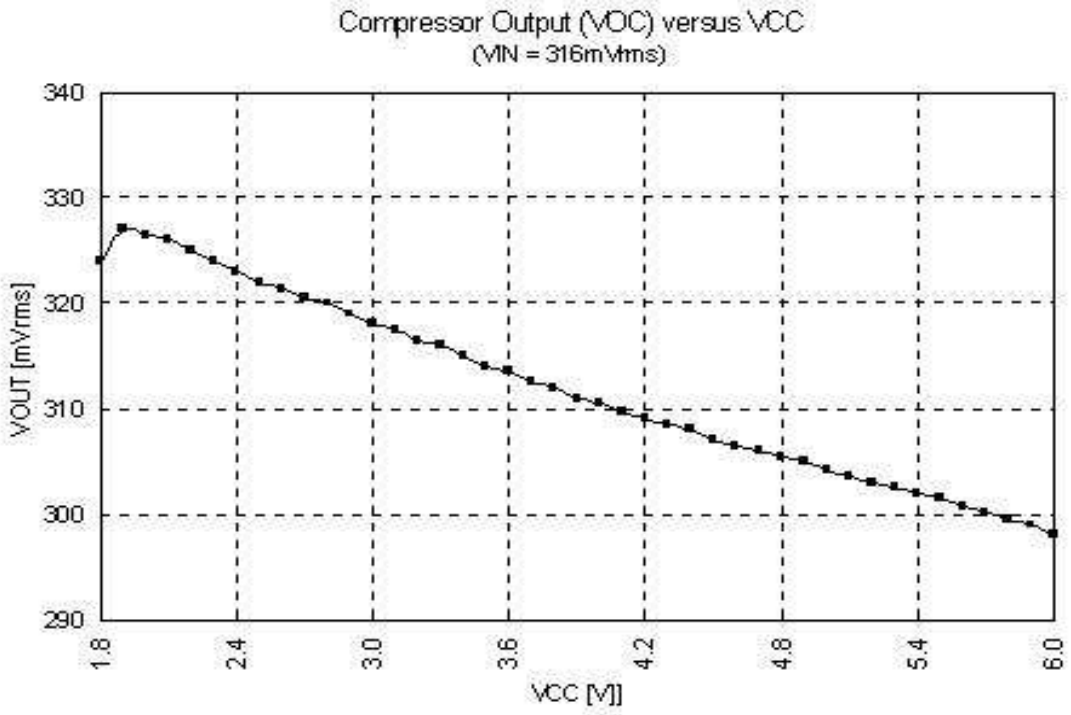


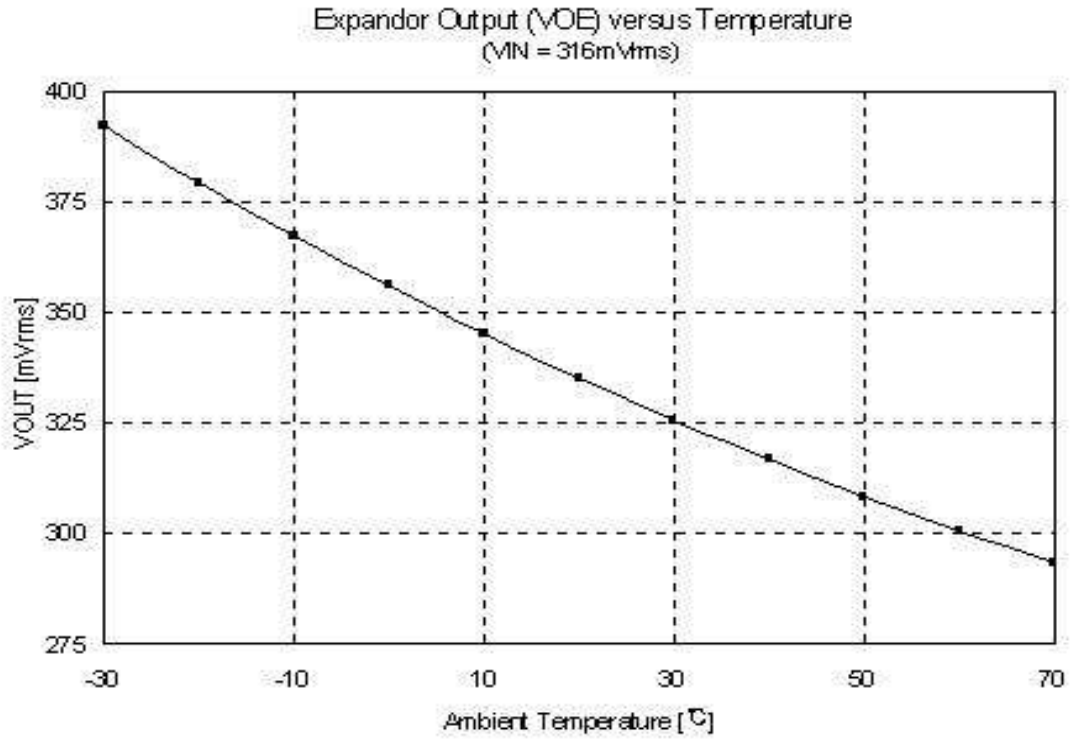


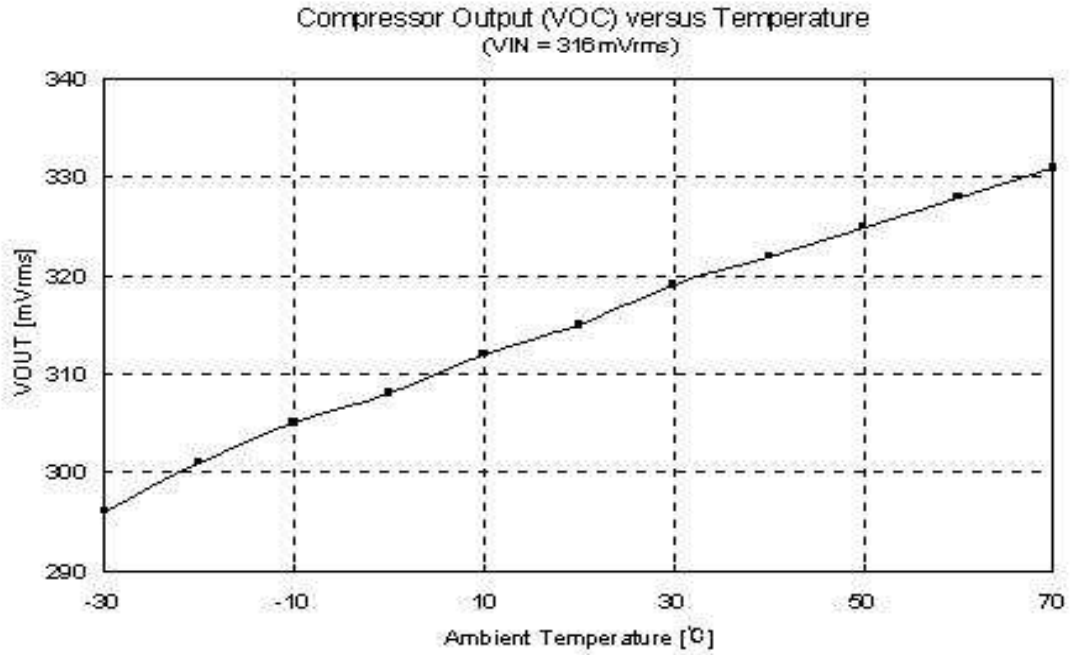












NOTES