



CYPRESS

CY7C1386B

CY7C1387B

# 512K x 36/1M x 18 Pipelined DCD SRAM

## Features

- **Fast clock speed: 200, 167, 150, 133 MHz**
- **Provide high-performance 3-1-1-1 access rate**
- **Fast OE access times: 3.0, 3.4, 3.8, and 4.2 ns**
- **Optimal for depth expansion**
- **3.3V (-5% / +10%) power supply**
- **Common data inputs and data outputs**
- **Byte Write Enable and Global Write control**
- **Double-cycle deselect**
- **Chip enable for address pipeline**
- **Address, data, and control registers**
- **Internally self-timed Write cycle**
- **Burst control pins (interleaved or linear burst sequence)**
- **Automatic power-down available using ZZ mode or CE deselect**
- **High-density, high-speed packages**
- **JTAG boundary scan for BGA packaging version**
- **Automatic power down available using ZZ mode or CE deselect**

## Functional Description

The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced single-layer polysilicon, triple-layer metal technology. Each memory cell consists of six transistors.

The CY7C1386B and CY7C1387B SRAMs integrate 524,288 x 36 and 1,048,576 x 18 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by

registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, data inputs, address-pipelining Chip Enables (CEs), burst control inputs (ADSC, ADSP, and ADV), Write Enables (BWa, BWb, BWc, BWd and BWE), and Global Write (GW).

Asynchronous inputs include the Output Enable ( $\overline{OE}$ ) and burst mode control (MODE).  $DQ_{a,b,c,d}$  and  $DP_{a,b,c,d}$  apply to CY7C1386B and  $DQ_{a,b}$  and  $DP_{a,b}$  apply to CY7C1387B. a, b, c, and d each are 8 bits wide in the case of DQ and 1 bit wide in the case of DP.

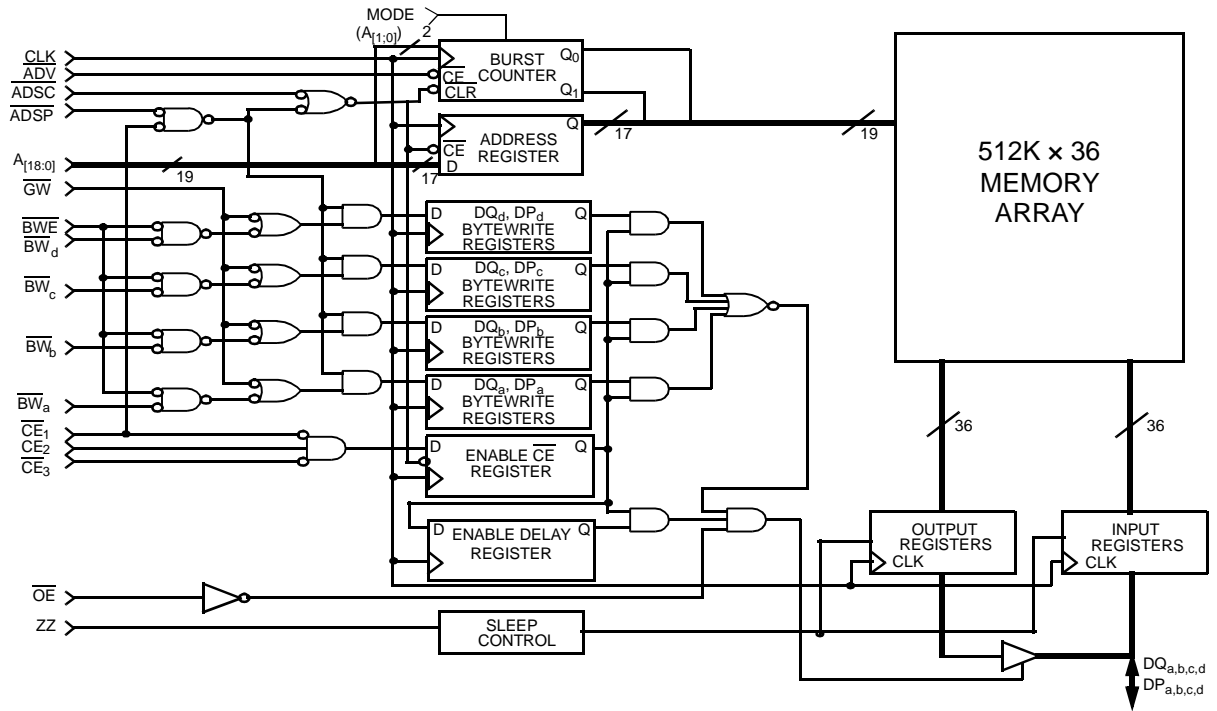
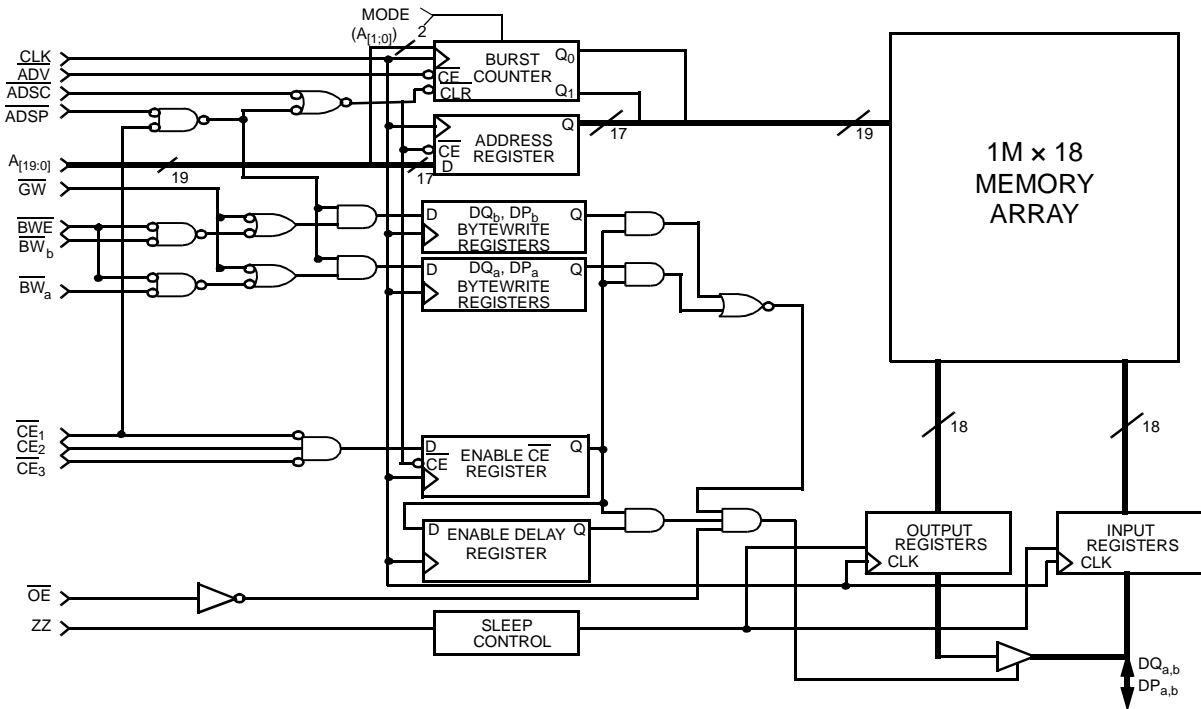
Addresses and chip enables are registered with either Address Status Processor (ADSP) or Address Status Controller (ADSC) input pins. Subsequent burst addresses can be internally generated as controlled by the Burst Advance Pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate self-timed Write cycles. Write cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BWa controls DQa and DQPa. BWb controls DQb and DQPb. BWc controls DQc and DQPc. BWd controls DQd-DQd and DQPd. BWa, BWb, BWc, and BWd can be active only with BWE LOW. GW LOW causes all bytes to be written. Write pass-through capability allows written data available at the output for the immediately next Read cycle. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

The CY7C1386B and CY7C1387B are both double-cycle deselect parts. All inputs and outputs of the CY7C1386B and the CY7C1387B are JEDEC-standard JESD8-5-compatible.

## Selection Guide

	200 MHz	167 MHz	150 MHz	133 MHz	Unit
Maximum Access Time	3	3.4	3.8	4.2	ns
Maximum Operating Current	315	285	265	245	mA
Maximum CMOS Standby Current	20	20	20	20	mA

**Logic Block Diagram CY7C1386B — 512K x 36**

**Logic Block Diagram CY7C1387B — 1M x 18**




**Pin Configurations** (continued)

**119-Ball BGA — Top View**  
**CY7C1386B (512K × 36)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
<b>C</b>	NC	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQc	DQPc	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQPb	DQb
<b>E</b>	DQc	DQc	V <sub>SS</sub>	CE1	V <sub>SS</sub>	DQb	DQb
<b>F</b>	V <sub>DDQ</sub>	DQc	V <sub>SS</sub>	OE	V <sub>SS</sub>	DQb	V <sub>DDQ</sub>
<b>G</b>	DQc	DQc	$\overline{\text{BWC}}$	$\overline{\text{ADV}}$	$\overline{\text{BWb}}$	DQb	DQb
<b>H</b>	DQc	DQc	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQb	DQb
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	DQd	DQd	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQa	DQa
<b>L</b>	DQd	DQd	$\overline{\text{BWD}}$	NC	$\overline{\text{BWA}}$	DQa	DQa
<b>M</b>	V <sub>DDQ</sub>	DQd	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	DQa	V <sub>DDQ</sub>
<b>N</b>	DQd	DQd	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQa	DQa
<b>P</b>	DQd	DQPd	V <sub>SS</sub>	A0	V <sub>SS</sub>	DQPd	DQa
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	V <sub>DD</sub>	A	NC
<b>T</b>	NC	64M	A	A	A	32M	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**CY7C1387B (1M × 18)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	$\overline{\text{ADSP}}$	A	A	V <sub>DDQ</sub>
<b>B</b>	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
<b>C</b>	NC	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQb	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQPd	NC
<b>E</b>	NC	DQb	V <sub>SS</sub>	CE1	V <sub>SS</sub>	NC	DQa
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	OE	V <sub>SS</sub>	DQa	V <sub>DDQ</sub>
<b>G</b>	NC	DQb	$\overline{\text{BWb}}$	$\overline{\text{ADV}}$	V <sub>SS</sub>	NC	DQa
<b>H</b>	DQb	NC	V <sub>SS</sub>	$\overline{\text{GW}}$	V <sub>SS</sub>	DQa	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQb	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQa
<b>L</b>	DQb	NC	V <sub>SS</sub>	NC	$\overline{\text{BWA}}$	DQa	NC
<b>M</b>	V <sub>DDQ</sub>	DQb	V <sub>SS</sub>	$\overline{\text{BWE}}$	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQb	NC	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQa	NC
<b>P</b>	NC	DQPd	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC	DQa
<b>R</b>	NC	A	MODE	V <sub>DD</sub>	V <sub>DD</sub>	A	NC
<b>T</b>	64M	A	A	32M	A	A	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**Pin Configurations** (continued)

**165-Ball Bump FBGA**
**CY7C1386B (512K × 36) — 11 × 15 FBGA**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC	A	$\overline{CE}_1$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	NC
<b>B</b>	NC	A	$CE_2$	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	128M
<b>C</b>	DPc	NC	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	DPb
<b>D</b>	DQc	DQc	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQb	DQb
<b>E</b>	DQc	DQc	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQb	DQb
<b>F</b>	DQc	DQc	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQb	DQb
<b>G</b>	DQc	DQc	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQb	DQb
<b>H</b>	NC	$V_{SS}$	NC	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	NC	NC	ZZ
<b>J</b>	DQd	DQd	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	DQa
<b>K</b>	DQd	DQd	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	DQa
<b>L</b>	DQd	DQd	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	DQa
<b>M</b>	DQd	DQd	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	DQa
<b>N</b>	DPd	NC	$V_{DDQ}$	$V_{SS}$	NC	A	NC	$V_{SS}$	$V_{DDQ}$	NC	DPa
<b>P</b>	NC	64M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	32M	A	A	TMS	A0	TCK	A	A	A	A

**CY7C1387B (1M × 18) — 11 × 15 FBGA**

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	NC	A	$\overline{CE}_1$	$\overline{BWb}$	NC	$\overline{CE}_3$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A	A
<b>B</b>	NC	A	$CE_2$	NC	$\overline{BWa}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A	128M
<b>C</b>	NC	NC	$V_{DDQ}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DDQ}$	NC	DPa
<b>D</b>	NC	DQb	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	DQa
<b>E</b>	NC	DQb	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	DQa
<b>F</b>	NC	DQb	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	DQa
<b>G</b>	NC	DQb	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	NC	DQa
<b>H</b>	NC	$V_{SS}$	NC	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	NC	NC	ZZ
<b>J</b>	DQb	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	NC
<b>K</b>	DQb	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	NC
<b>L</b>	DQb	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	NC
<b>M</b>	DQb	NC	$V_{DDQ}$	$V_{DD}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{DD}$	$V_{DDQ}$	DQa	NC
<b>N</b>	DPb	NC	$V_{DDQ}$	$V_{SS}$	NC	A	NC	$V_{SS}$	$V_{DDQ}$	NC	NC
<b>P</b>	NC	64M	A	A	TDI	A1	TDO	A	A	A	A
<b>R</b>	MODE	32M	A	A	TMS	A0	TCK	A	A	A	A

**Pin Definitions**

Name	I/O	Description
A0 A1 A	Input- Synchronous	<b>Address Inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> are sampled active. A <sub>[1:0]</sub> feeds the 2-bit counter.
BW <sub>a</sub> BW <sub>b</sub> BW <sub>c</sub> BW <sub>d</sub>	Input- Synchronous	<b>Byte Write Select Inputs, active LOW.</b> Qualified with BWE to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
GW	Input- Synchronous	<b>Global Write Enable input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global Write is conducted (ALL bytes are written, regardless of the values on BW <sub>a,b,c,d</sub> and BWE).
BWE	Input- Synchronous	<b>Byte Write Enable input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	<b>Clock Input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW during a burst operation.
CE <sub>1</sub>	Input- Synchronous	<b>Chip Enable 1 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and CE <sub>3</sub> to select/deselect the device. ADSP is ignored if CE <sub>1</sub> is HIGH.
CE <sub>2</sub>	Input- Synchronous	<b>Chip Enable 2 input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>3</sub> to select/deselect the device (TQFP only).
CE <sub>3</sub>	Input- Synchronous	<b>Chip Enable 3 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>1</sub> and CE <sub>2</sub> to select/deselect the device (TQFP only).
OE	Input- Asynchronous	<b>Output Enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input- Synchronous	<b>Advance Input signal, sampled on the rising edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input- Synchronous	<b>Address Strobe from Processor, sampled on the rising edge of CLK.</b> When asserted LOW, A is captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when CE <sub>1</sub> is deasserted HIGH.
ADSC	Input- Synchronous	<b>Address Strobe from Controller, sampled on the rising edge of CLK.</b> When asserted LOW, A <sub>[x:0]</sub> is captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
MODE	Input-Pin	<b>Selects Burst Order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DDQ</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.
ZZ	Input- Asynchronous	<b>ZZ "sleep" input.</b> This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved.
DQ <sub>a</sub> , DP <sub>a</sub> DQ <sub>b</sub> , DP <sub>b</sub> DQ <sub>c</sub> , DP <sub>c</sub> DQ <sub>d</sub> , DP <sub>d</sub>	I/O- Synchronous	<b>Bidirectional data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A <sub>x</sub> during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>x</sub> and DP <sub>x</sub> are placed in a three-state condition. DQ <sub>a,b,c</sub> and d are 8 bits wide. DP <sub>a,b,c</sub> and d are 1 bit wide.

**Pin Definitions**

<b>Name</b>	<b>I/O</b>	<b>Description</b>
TDO	JTAG serial output synchronous	<b>Serial data-out to the JTAG circuit.</b> Delivers data on the negative edge of TCK (BGA only).
TDI	JTAG serial input synchronous	<b>Serial data-in to the JTAG circuit.</b> Sampled on the rising edge of TCK (BGA only).
TMS	Test Mode Select synchronous	This pin controls the Test Access Port (TAP) state machine. Sampled on the rising edge of TCK (BGA only).
TCK	JTAG serial clock	Serial clock to the JTAG circuit (BGA only).
V <sub>DD</sub>	Power supply	<b>Power supply inputs to the core of the device.</b> Should be connected to 3.3V –5% +10% power supply.
V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b> Should be connected to ground of the system.
V <sub>DDQ</sub>	I/O Power Supply	<b>Power supply for the I/O circuitry.</b> Should be connected to a 2.5V –5% or a 3.3V –5% +10% power supply (see page 20).
V <sub>SSQ</sub>	I/O Ground	<b>Ground for the I/O circuitry.</b> Should be connected to ground of the system.
NC	–	<b>No connects.</b> Pins are not internally connected.
32M 64M 128M	–	<b>No connects.</b> Reserved for address expansion. Pins are not internally connected.

## Introduction

### Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CO}$ ) is 4.2 ns (133-MHz device).

The CY7C1386B/ supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium® and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe (ADSP) or the Controller Address Strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable (BWE) and Byte Write Select ( $BW_{a,b,c,d}$  for 1386B and  $BW_{a,b}$  for 1387B) inputs. A Global Write Enable ( $\overline{GW}$ ) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Synchronous Chip Selects ( $\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$  for TQFP /  $\overline{CE}_1$  for BGA) and an asynchronous OE provide for easy bank selection and output three-state control. ADSP is ignored if  $\overline{CE}_1$  is HIGH.

#### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) ADSP or ADSC is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals ( $\overline{GW}$ , BWE) are all deasserted HIGH. ADSP is ignored if  $\overline{CE}_1$  is HIGH. The address presented to the address inputs is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 4.2 ns (133-MHz device) if  $\overline{OE}$  is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the OE signal. Consecutive single read cycles are supported.

The CY7C1386B/CY7C1387B are double-cycle deselect parts. Once the SRAM is deselected at clock rise by the chip select and either ADSP or ADSC signals, its output will three-state immediately after the next clock rise.

#### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) ADSP is asserted LOW, and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the RAM core. The

Write signals ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BWx}$ ) and  $\overline{ADV}$  inputs are ignored during this first cycle.

$\overline{ADSP}$  triggered write accesses require two clock cycles to complete. If  $\overline{GW}$  is asserted LOW on the second clock rise, the data presented to the DQx inputs is written into the corresponding address location in the RAM core. If  $\overline{GW}$  is HIGH, then the write operation is controlled by BWE and  $\overline{BWx}$  signals. The CY7C1386B/CY7C1387B provides byte Write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input (BWE) with the selected Byte Write ( $\overline{BW}_{a,b,c,d}$  for CY7C1386B, and  $\overline{BW}_{a,b}$  for CY7C1387B) input will selectively write to only the desired bytes. Bytes not selected during a byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1386B/CY7C1387B is a common I/O device, the  $\overline{OE}$  must be deasserted HIGH before presenting data to the DQ inputs. Doing so will three-state the output drivers. As a safety precaution, DQ are automatically three-stated whenever a Write cycle is detected, regardless of the state of  $\overline{OE}$ .

#### Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$  write accesses are initiated when the following conditions are satisfied: (1) ADSC is asserted LOW, (2) ADSP is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs ( $\overline{GW}$ , BWE, and  $\overline{BWx}$ ) are asserted active to conduct a write to the desired byte(s). ADSC triggered write accesses require a single clock cycle to complete. The address presented to  $A_{[17:0]}$  is loaded into the address register and the address advancement logic while being delivered to the RAM core. The  $\overline{ADV}$  input is ignored during this cycle. If a Global Write is conducted, the data presented to the  $DQ_{[x:0]}$  is written into the corresponding address location in the RAM core. If a byte Write is conducted, only the selected bytes are written. Bytes not selected during a byte Write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify Write operations.

Because the CY7C1386B/CY7C1387B is a common I/O device, the  $\overline{OE}$  must be deasserted HIGH before presenting data to the  $DQ_{[x:0]}$  inputs. Doing so will three-state the output drivers. As a safety precaution,  $DQ_{[x:0]}$  are automatically three-stated whenever a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Burst Sequences

The CY7C1386B/CY7C1387B provides a two-bit wraparound counter, fed by  $A_{[1:0]}$ , that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium® applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting  $\overline{ADV}$  LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.



**Interleaved Burst Sequence**

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**Linear Burst Sequence**

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**Sleep Mode**

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. CEs, ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

**ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min.	Max.	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		20	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

**Cycle Descriptions<sup>[1,2,3,4]</sup>**

Next Cycle	Add. Used	ZZ	CE <sub>3</sub>	CE <sub>2</sub>	CE <sub>1</sub>	ADSP	ADSC	ADV	OE	DQ	Write
Unselected	None	0	X	X	H	X	L	X	X	Hi-Z	X
Unselected	None	0	H	X	L	L	X	X	X	Hi-Z	X
Unselected	None	0	X	L	L	L	X	X	X	Hi-Z	X
Unselected	None	0	H	X	L	H	L	X	X	Hi-Z	X
Unselected	None	0	X	L	L	H	L	X	X	Hi-Z	X
Begin Read	External	0	L	H	L	L	X	X	X	Hi-Z	X
Begin Read	External	0	L	H	L	H	L	X	X	Hi-Z	Read
Continue Read	Next	0	X	X	X	H	H	L	H	Hi-Z	Read
Continue Read	Next	0	X	X	X	H	H	L	L	DQ	Read
Continue Read	Next	0	X	X	H	X	H	L	H	Hi-Z	Read
Continue Read	Next	0	X	X	H	X	H	L	L	DQ	Read
Suspend Read	Current	0	X	X	X	H	H	H	H	Hi-Z	Read
Suspend Read	Current	0	X	X	X	H	H	H	L	DQ	Read
Suspend Read	Current	0	X	X	H	X	H	H	H	Hi-Z	Read
Suspend Read	Current	0	X	X	H	X	H	H	L	DQ	Read
Begin Write	Current	0	X	X	X	H	H	H	X	Hi-Z	Write
Begin Write	Current	0	X	X	H	X	H	H	X	Hi-Z	Write
Begin Write	External	0	L	H	L	H	L	X	X	Hi-Z	Write
Continue Write	Next	0	X	X	X	H	H	L	X	Hi-Z	Write
Continue Write	Next	0	X	X	H	X	H	L	X	Hi-Z	Write
Suspend Write	Current	0	X	X	X	H	H	H	X	Hi-Z	Write
Suspend Write	Current	0	X	X	H	X	H	H	X	Hi-Z	Write
ZZ "sleep"	None	1	X	X	X	X	X	X	X	Hi-Z	X

**Notes:**

1. X = "Don't Care." H = HIGH, L = LOW.
2. Write is defined by BWE, BWx, and GW. See Write Cycle Descriptions table.
3. The DQ pins are controlled by the current cycle and the OE signal. OE is asynchronous and is not sampled with the clock.
4. CE<sub>1</sub>, CE<sub>2</sub>, and CE<sub>3</sub> are available only in the TQFP package. The BGA package has a single chip select CE<sub>1</sub>.

**Write Cycle Descriptions<sup>[5,6,7]</sup>**

Function (1386B)	GW	BWE	BWd	BWc	BWb	BWa
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0 - DQa	1	0	1	1	1	0
Write Byte 1- DQb	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 - DQc	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - DQd5	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Function (1387B)	GW	BWE	BWb	BWa
Read	1	1	X	X
Read	1	0	1	1
Write Byte 0 - DQ <sub>[7:0]</sub> and DP <sub>0</sub>	1	0	1	0
Write Byte 1 - DQ <sub>[15:8]</sub> and DP <sub>1</sub>	1	0	0	1
Write All Bytes	1	0	0	0
Write All Bytes	0	X	X	X

**Notes:**

5. X = "Don't Care", 1 = Logic HIGH, 0 = Logic LOW.
6. The SRAM always initiates a Read cycle when ADSP asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_x$ . Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the Write cycle to allow the outputs to three-state.  $\overline{OE}$  is a "don't care" for the remainder of the Write cycle.
7.  $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during Write cycles. During a Read cycle DQ = High-Z when  $\overline{OE}$  is inactive or when the device is deselected, and DQ = data when  $\overline{OE}$  is active.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

The CY7C1386B/CY7C1387B incorporates a serial boundary scan Test Access Port (TAP) in the FBGA package only. The TQFP package does not offer this functionality. This port operates in accordance with IEEE Standard 1149.1-1900, but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to  $V_{DD}$  through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a Reset state that will not interfere with the operation of the device.

### Test Access Port – Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

### Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The e output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A Reset is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test

circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

#### *Instruction Register*

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in the TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a Reset state as described in the previous section.

When the TAP controller is in the CaptureIR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board level serial test path.

#### *Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### *Boundary Scan Register*

The boundary scan register is connected to all the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 70-bit-long register, and the x18 configuration has a 51-bit-long register.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### *Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the

SRAM and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather it performs a capture of the Inputs and Output ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

#### *EXTEST*

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the TAP controller, and therefore this device is not compliant to the 1149.1 standard.

The TAP controller does not recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

#### *IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

#### *SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

#### *SAMPLE/PRELOAD*

SAMPLE / PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (TCS and TCH). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and  $\overline{CK}$  captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

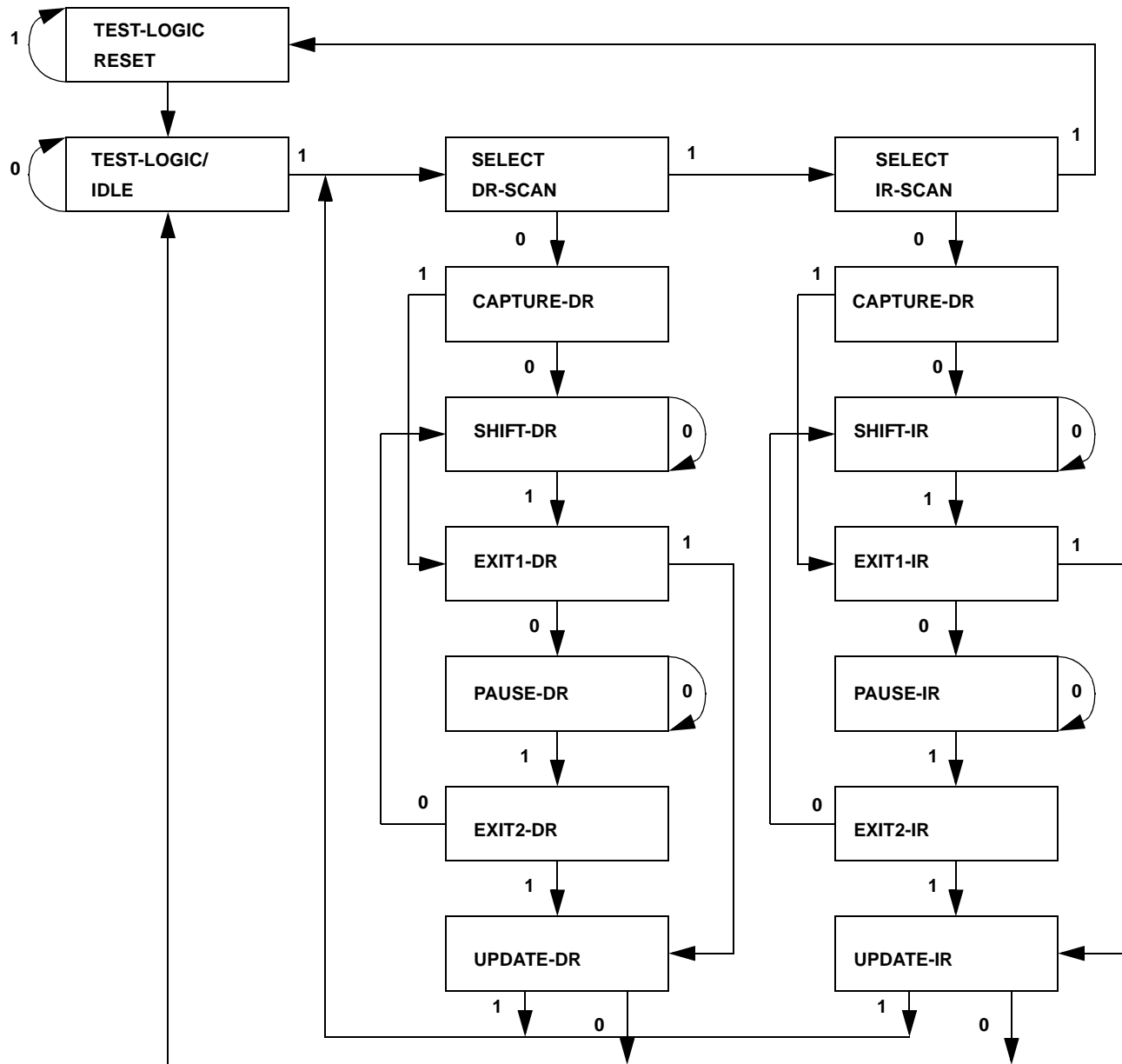
Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

#### *Bypass*

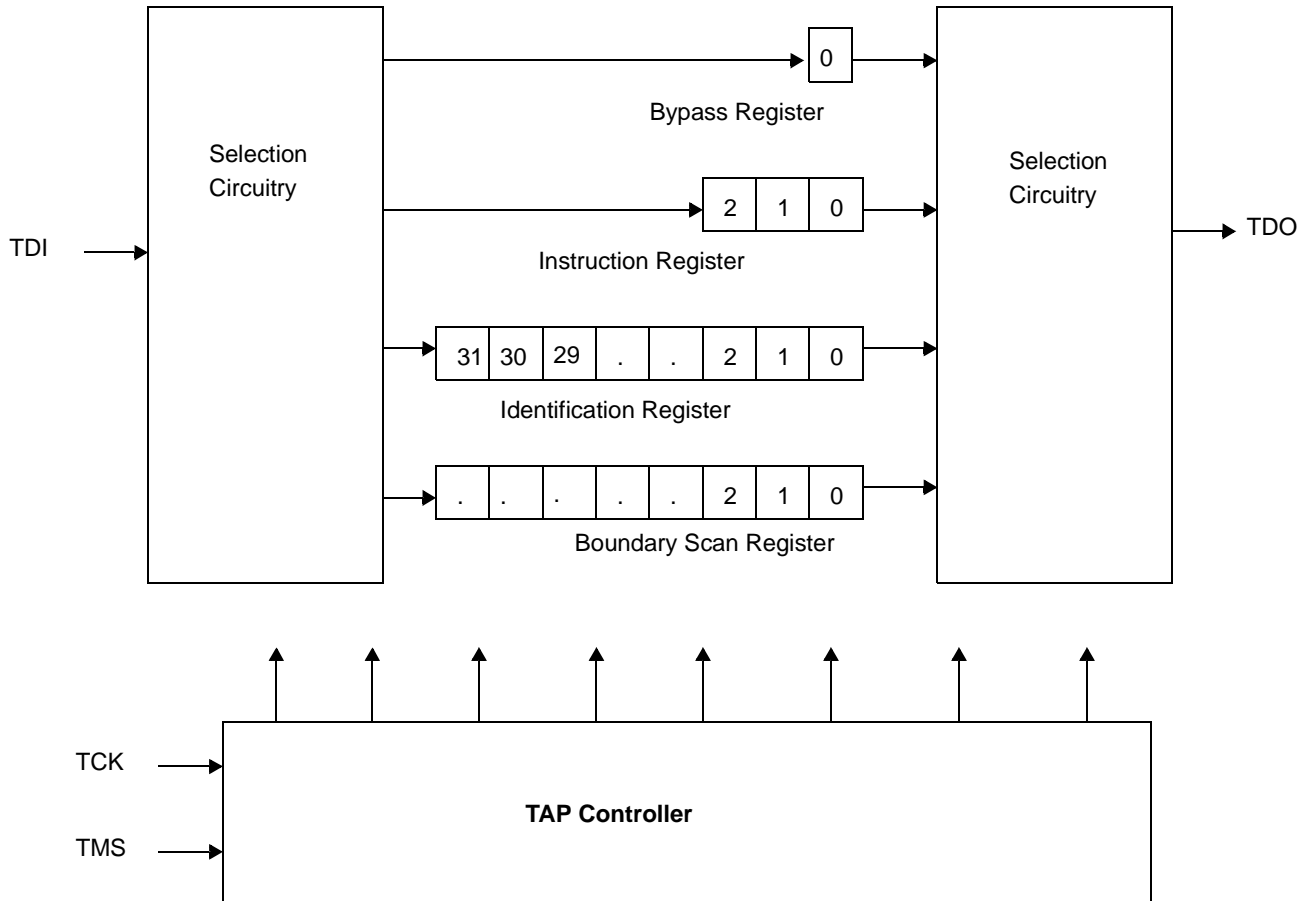
When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

#### *Reserved*

These instructions are not implemented but are reserved for future use. Do not use these instructions.

**TAP Controller State Diagram**

**Note:**

8. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

**TAP Controller Block Diagram**

**TAP Electrical Characteristics** Over the Operating Range<sup>[9, 10]</sup>

Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>OH1</sub>	Output HIGH Voltage	I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OH2</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.2		V
V <sub>OL1</sub>	Output LOW Voltage	I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>OL2</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA		0.2	V
V <sub>IH</sub>	Input HIGH Voltage		1.7	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.7	V
I <sub>X</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA

**Notes:**

9. All Voltage referenced to Ground.

10. Overshoot: V<sub>IH(AC)</sub> ≤ V<sub>DD</sub> + 1.5V for t ≤ t<sub>TCYC</sub>/2, Undershoot: V<sub>IL(AC)</sub> ≤ 0.5V for t ≤ t<sub>TCYC</sub>/2, Power-up: V<sub>IH</sub> < 2.6V and V<sub>DD</sub> < 2.4V and V<sub>DDQ</sub> < 1.4V for t < 200 ms.

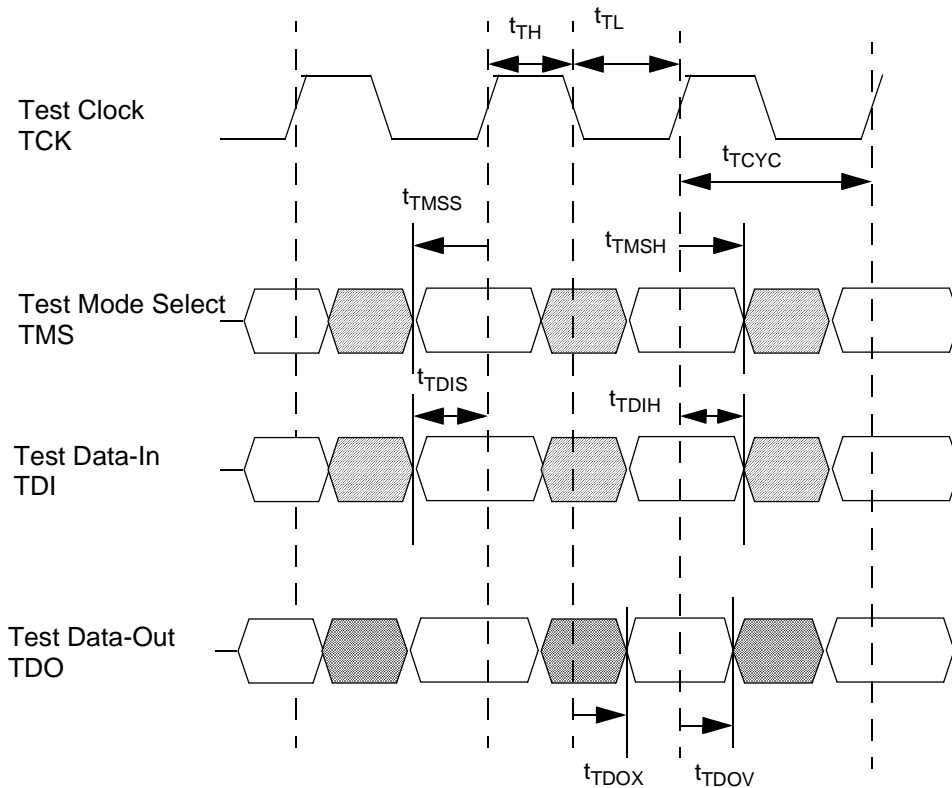
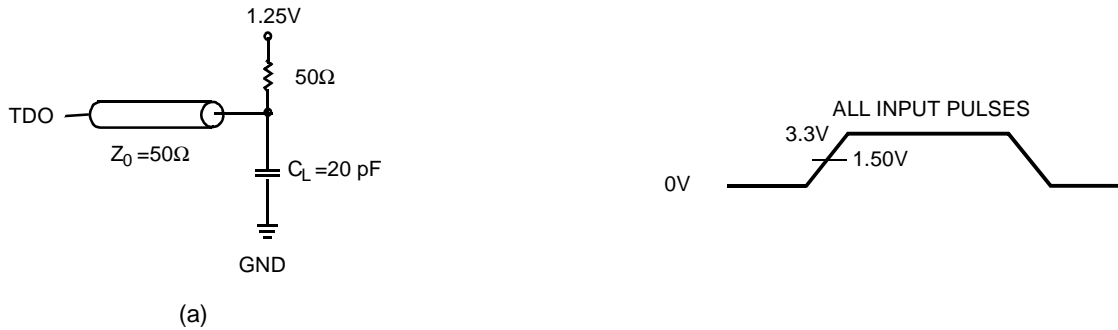
**TAP AC Switching Characteristics** Over the Operating Range<sup>[11,12]</sup>

Parameters	Description	Min.	Max.	Unit
$t_{TCYC}$	TCK Clock Cycle Time	100		ns
$t_{TF}$	TCK Clock Frequency		10	MHz
$t_{TH}$	TCK Clock HIGH	40		ns
$t_{TL}$	TCK Clock LOW	40		ns
<b>Set-up Times</b>				
$t_{TMSS}$	TMS Set-up to TCK Clock Rise	10		ns
$t_{TDIS}$	TDI Set-up to TCK Clock Rise	10		ns
$t_{CS}$	Capture Set-up to TCK Rise	10		ns
<b>Hold Times</b>				
$t_{TMSh}$	TMS Hold after TCK Clock Rise	10		ns
$t_{TDIH}$	TDI Hold after Clock Rise	10		ns
$t_{CH}$	Capture Hold after Clock Rise	10		ns
<b>Output Times</b>				
$t_{TDOV}$	TCK Clock LOW to TDO Valid		20	ns
$t_{TDOX}$	TCK Clock LOW to TDO Invalid	0		ns

**Notes:**

11.  $t_{CS}$  and  $t_{CH}$  refer to the set-up and hold time requirements of latching data from the boundary scan register.  
 12. Test conditions are specified using the load in TAP AC test conditions. TR/TF = 1 ns.



**TAP Timing and Test Conditions**


**Identification Register Definitions**

Instruction Field	512K x 36	1M x 18	Description
Revision Number (31:28)	xxxx	xxxx	Reserved for version number.
Device Depth (27:23)	00111	01000	Defines depth of SRAM. 512K or 1M.
Device Width (22:18)	00100	00011	Defines with of the SRAM. x36 or x18.
Cypress Device ID (17:12)	xxxxx	xxxxx	Reserved for future use.
Cypress JEDEC ID (11:1)	00011100100	00011100100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicate the presence of an ID register.

**Scan Register Sizes**

Register Name	Bit Size (x18)	Bit Size (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

**Identification Codes**

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents. Places the boundary scan register between the TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use. This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

**Boundary Scan Order (512K x 18)**

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	36	A	6B
2	A	3T	37	BWa#	5L
3	A	4T	38	BWb#	5G
4	A	5T	39	BWc#	3G
5	A	6R	40	BWd#	3L
6	A	3B	41	A	2B
7	A	5B	42	CE#	4E
8	DQa	6P	43	A	3A
9	DQa	7N	44	A	2A
10	DQa	6M	45	DQc	2D
11	DQa	7L	46	DQc	1E
12	DQa	6K	47	DQc	2F
13	DQa	7P	48	DQc	1G
14	DQa	6N	49	DQc	1D
15	DQa	6L	50	DQc	1D
16	DQa	7K	51	DQc	2E
17	ZZ	7T	52	DQc	2G
18	DQb	6H	53	DQc	1H
19	DQb	7G	54	NC	5R
20	DQb	6F	55	DQd	2K
21	DQb	7E	56	DQd	1L
22	DQb	6D	57	DQd	2M
23	DQb	7H	58	DQd	1N
24	DQb	6G	59	DQd	2P
25	DQb	6E	60	DQd	1K
26	DQb	7D	61	DQd	2L
27	A	6A	62	DQd	2N
28	A	5A	63	DQd	1P
29	ADV#	4G	64	MODE	3R
30	ADSP#	4A	65	A	2C
31	ADSC#	4B	66	A	3C
32	OE#	4F	67	A	5C
33	BWE#	4M	68	A	6C
34	GW#	4H	69	A1	4N
35	CLK	4K	70	A0	4P

**Boundary Scan Order (1M x 18)**

Bit #	Signal Name	Bump ID	Bit #	Signal Name	Bump ID
1	A	2R	36	DQb	2E
2	A	2T	37	DQb	2G
3	A	3T	38	DQb	1H
4	A	5T	39	NC	5R
5	A	6R	40	DQb	2K
6	A	3B	41	DQb	1L
7	A	5B	42	DQb	2M
8	DQa	7P	43	DQb	1N
9	DQa	6N	44	DQb	2P
10	DQa	6L	45	MODE	3R
11	DQa	7K	46	A	2C
12	ZZ	7T	47	A	3C
13	DQa	6H	48	A	5C
14	DQa	7G	49	A	6C
15	DQa	6F	50	A1	4N
16	DQa	7E	51	A0	4P
17	DQa	6D			
18	A	6T			
19	A	6A			
20	A	5A			
21	ADV#	4G			
22	ADSP#	4A			
23	ADSC#	4B			
24	OE#	4F			
25	BWE#	4M			
26	GW#	4H			
27	CLK	4K			
28	A	6B			
29	BWa#	5L			
30	BWb#	3G			
31	A	2B			
32	CE#	4E			
33	A	3A			
34	A	2A			
35	DQb	1D			



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature ..... -55°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage on V<sub>DD</sub> Relative to GND ..... -0.5V to +4.6V
- DC Voltage Applied to Outputs in High-Z State<sup>[13]</sup> ..... -0.5V to V<sub>DDQ</sub> + 0.5V
- DC Input Voltage<sup>[13]</sup> ..... -0.5V to V<sub>DDQ</sub> + 0.5V
- Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >1500V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temp. <sup>[14.]</sup>	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0°C to +70°C	3.3V -5%/+10%	2.5V -5% 3.3V + 10%
Industrial	-40°C to +85°C		

**Electrical Characteristics** Over the Operating Range

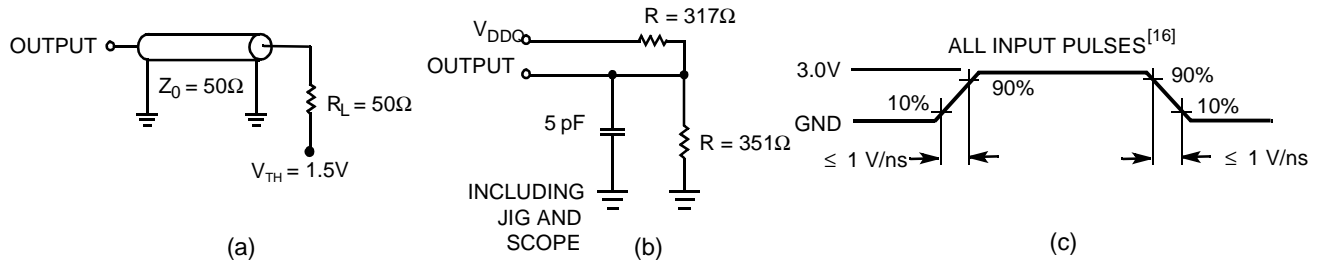
Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>DD</sub>	Power Supply Voltage	3.3V range	3.135	3.63	V
V <sub>DDQ</sub>	I/O Supply Voltage	3.3V range	2.375	3.63	V
		2.5V range	2.375	V <sub>DD</sub>	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>DD</sub> = Min., I <sub>OH</sub> = -4.0 mA	3.3V	2.4	V
		V <sub>DD</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.5V	2.0	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>DD</sub> = Min., I <sub>OL</sub> = 8.0 mA	3.3V	0.4	V
		V <sub>DD</sub> = Min., I <sub>OH</sub> = 1.0 mA	2.5V	0.4	V
V <sub>IH</sub>	Input HIGH Voltage	3.3 V	2.0		V
		2.5V	1.7		V
V <sub>IL</sub>	Input LOW Voltage <sup>[13]</sup>	3.3V	-0.3	0.8	V
		2.5V	-0.3	0.7	V
I <sub>X</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>		5	μA
	Input Current of MODE		-30	30	μA
	Input Current of ZZ	Input = V <sub>SS</sub>	-30	30	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled		5	μA
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	5.0-ns cycle, 200 MHz	315	mA
			6.0-ns cycle, 167 MHz	285	mA
			6.7-ns cycle, 150 MHz	265	mA
			7.5-ns cycle, 133 MHz	245	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	5.0-ns cycle, 200 MHz	140	mA
			6.0-ns cycle, 167 MHz	120	mA
			6.7-ns cycle, 150 MHz	110	mA
			7.5-ns cycle, 133 MHz	105	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = 0	All speed grades	20	mA
I <sub>SB3</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, or V <sub>IN</sub> ≤ 0.3V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3V, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	5.0-ns cycle, 200 MHz	110	mA
			6.0-ns cycle, 167 MHz	100	mA
			6.7-ns cycle, 150 MHz	90	mA
			7.5-ns cycle, 133 MHz	85	mA
I <sub>SB4</sub>	Automatic CS Power-Down Current—TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0	All Speeds	50	mA

**Notes:**

- 13. Minimum voltage equals -2.0V for pulse durations of less than 20 ns
- 14. T<sub>A</sub> is the temperature.

**Capacitance<sup>[15]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ $V_{DD} = 3.3\text{V}$ $V_{DDQ} = 3.3$	3	pF
$C_{CLK}$	Clock Input Capacitance		3	pF
$C_{I/O}$	Input/Output Capacitance		3	pF

**AC Test Loads and Waveforms<sup>[16]</sup>**

**Thermal Resistance<sup>[15]</sup>**

Description	Test Conditions	$Q_{JA}$ (Junction to Ambient)	$Q_{JC}$ (Junction to Case)	Units
119 BGA	Still Air, soldered on a 114.3 × 101.6 × 1.57 mm <sup>3</sup> , 2-layer board	41.54	6.33	$^\circ\text{C/W}$
165 FBGA		44.51	2.38	$^\circ\text{C/W}$
100-pin TQFP	Still Air, soldered on a 4.25 × 1.125 inch, 4-layer printed circuit board	25	9	$^\circ\text{C/W}$

**Notes:**

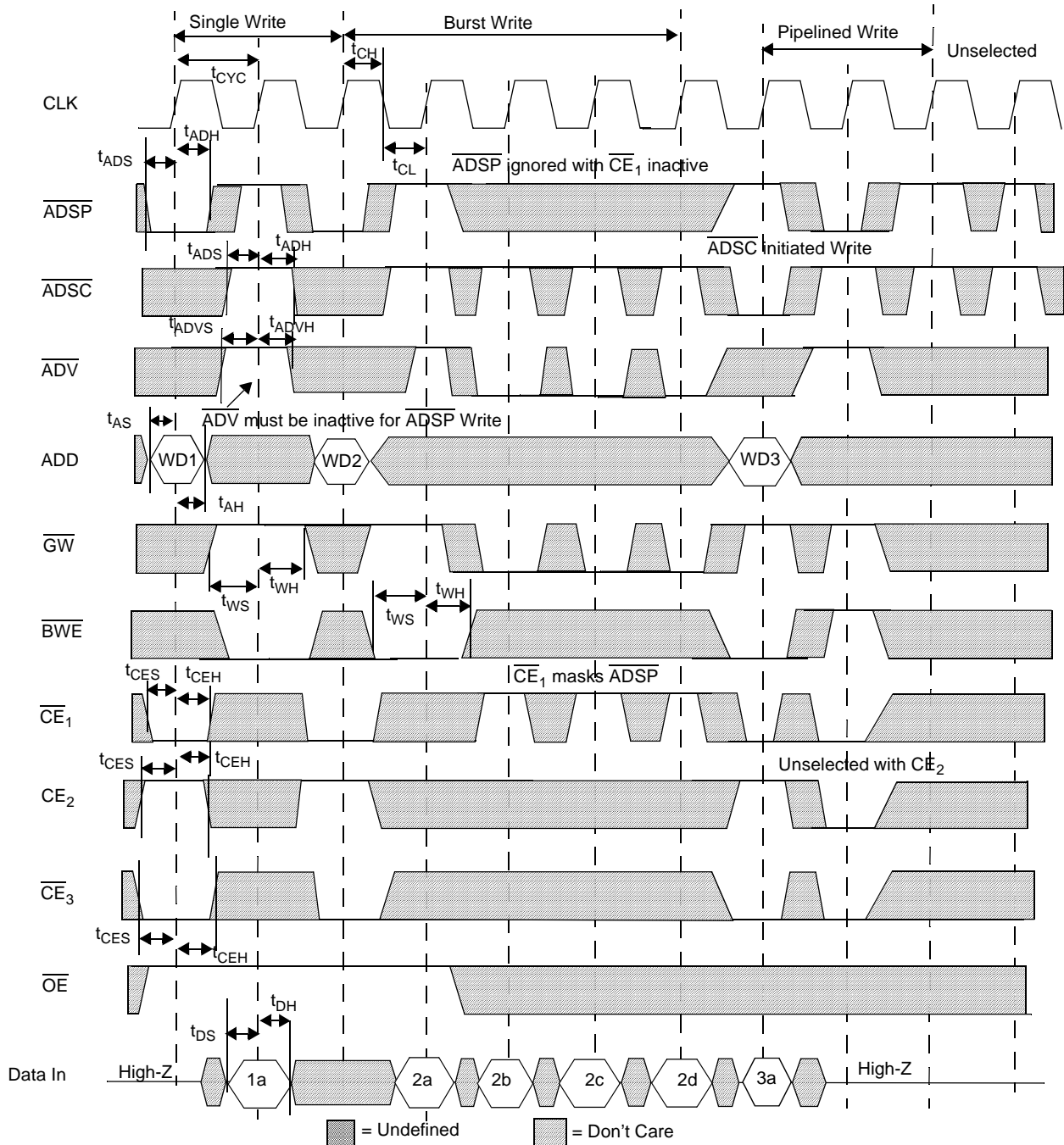
15. Tested initially and after any design or process changes that may affect these parameters.  
 16. Input waveform should have a slew rate of 1 V/ns.

**Switching Characteristics** Over the Operating Range<sup>[17,18,19]</sup>

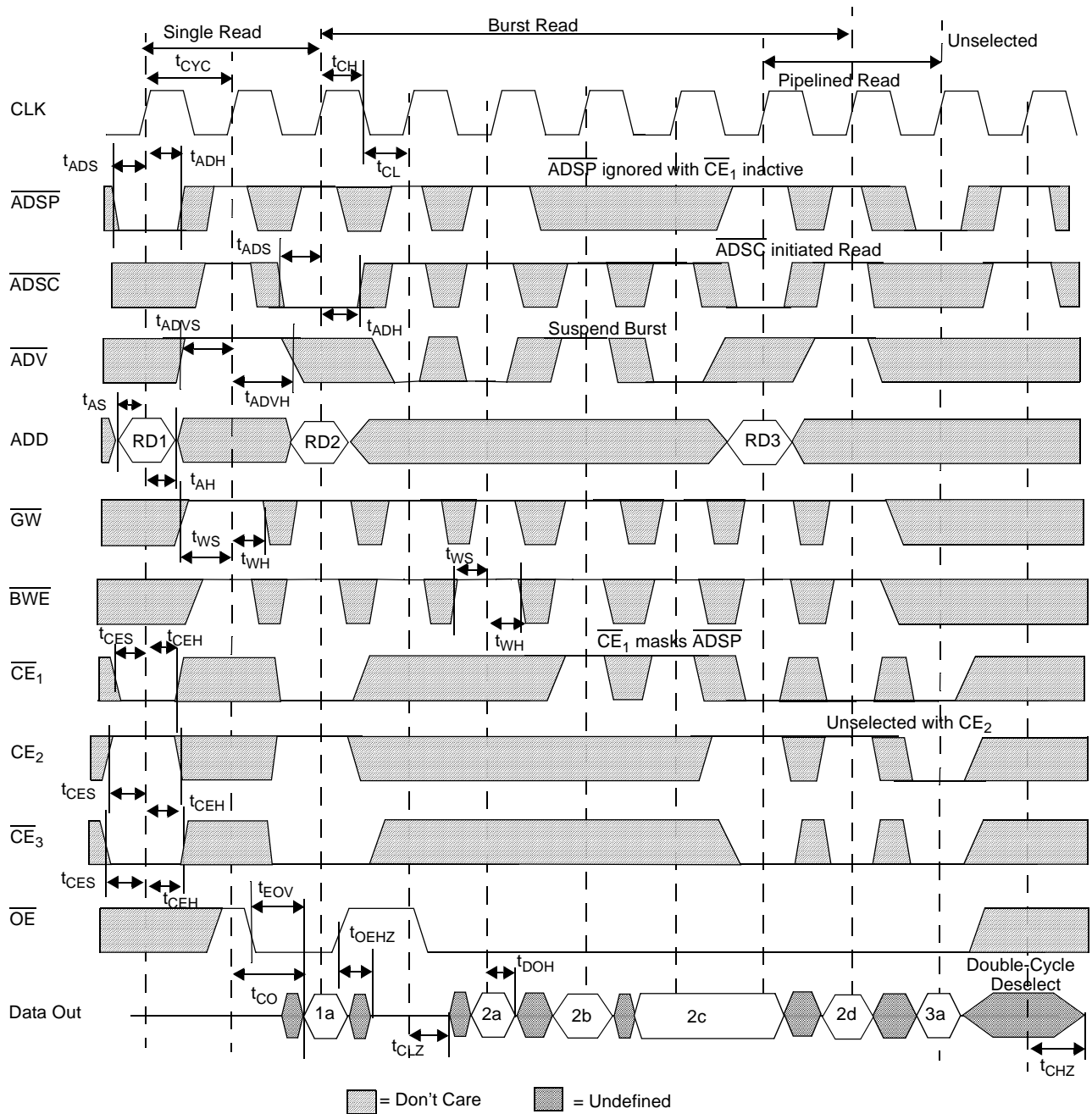
Parameter	Description	-200		-167		-150		-133		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC</sub>	Clock Cycle Time	5.0		6.0		6.7		7.5		ns
t <sub>CH</sub>	Clock HIGH	1.8		2.1		2.3		2.5		ns
t <sub>CL</sub>	Clock LOW	1.8		2.1		2.3		2.5		ns
t <sub>AS</sub>	Address Set-Up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t <sub>AH</sub>	Address Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t <sub>CO</sub>	Data Output Valid After CLK Rise		3.0		3.4		3.8		4.2	ns
t <sub>DOH</sub>	Data Output Hold After CLK Rise	1.5		1.5		1.5		1.5		ns
t <sub>ADS</sub>	ADSP, ADSC Set-Up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t <sub>ADH</sub>	ADSP, ADSC Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t <sub>WES</sub>	BWE, GW, BW <sub>x</sub> Set-Up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t <sub>WEH</sub>	BWE, GW, BW <sub>x</sub> Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t <sub>ADVS</sub>	ADV Set-Up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t <sub>ADVH</sub>	ADV Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t <sub>DS</sub>	Data Input Set-Up Before CLK Rise	1.4		1.5		1.5		1.5		ns
t <sub>DH</sub>	Data Input Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t <sub>CES</sub>	Chip enable Set-Up	1.4		1.5		1.5		1.5		ns
t <sub>CEH</sub>	Chip enable Hold After CLK Rise	0.4		0.5		0.5		0.5		ns
t <sub>CHZ</sub>	Clock to High-Z <sup>[18]</sup>		3.0		3.0		3.0		3.0	ns
t <sub>CLZ</sub>	Clock to Low-Z <sup>[18]</sup>	1.3		1.3		1.3		1.3		ns
t <sub>EOHZ</sub>	OE HIGH to Output High-Z <sup>[18,19]</sup>		4.0		4.0		4.0		4.0	ns
t <sub>EOLZ</sub>	OE LOW to Output Low-Z <sup>[18,19]</sup>	0		0		0		0		ns
t <sub>EOV</sub>	OE LOW to Output Valid <sup>[18]</sup>		3.0		3.4		3.8		4.2	ns

**Notes:**

17. Unless otherwise noted, test conditions assume signal transition time of 2.5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and load capacitance. Shown in (a), (b), and (c) of AC test loads.
18. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OEV</sub>, t<sub>EOLZ</sub>, and t<sub>EOHZ</sub> are specified with a load capacitance of 5 pF as in part (b) of AC test loads. Transition is measured ±200 mV from steady-state voltage.
19. At any given voltage and temperature, t<sub>EOHZ</sub> is less than t<sub>EOLZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub>.

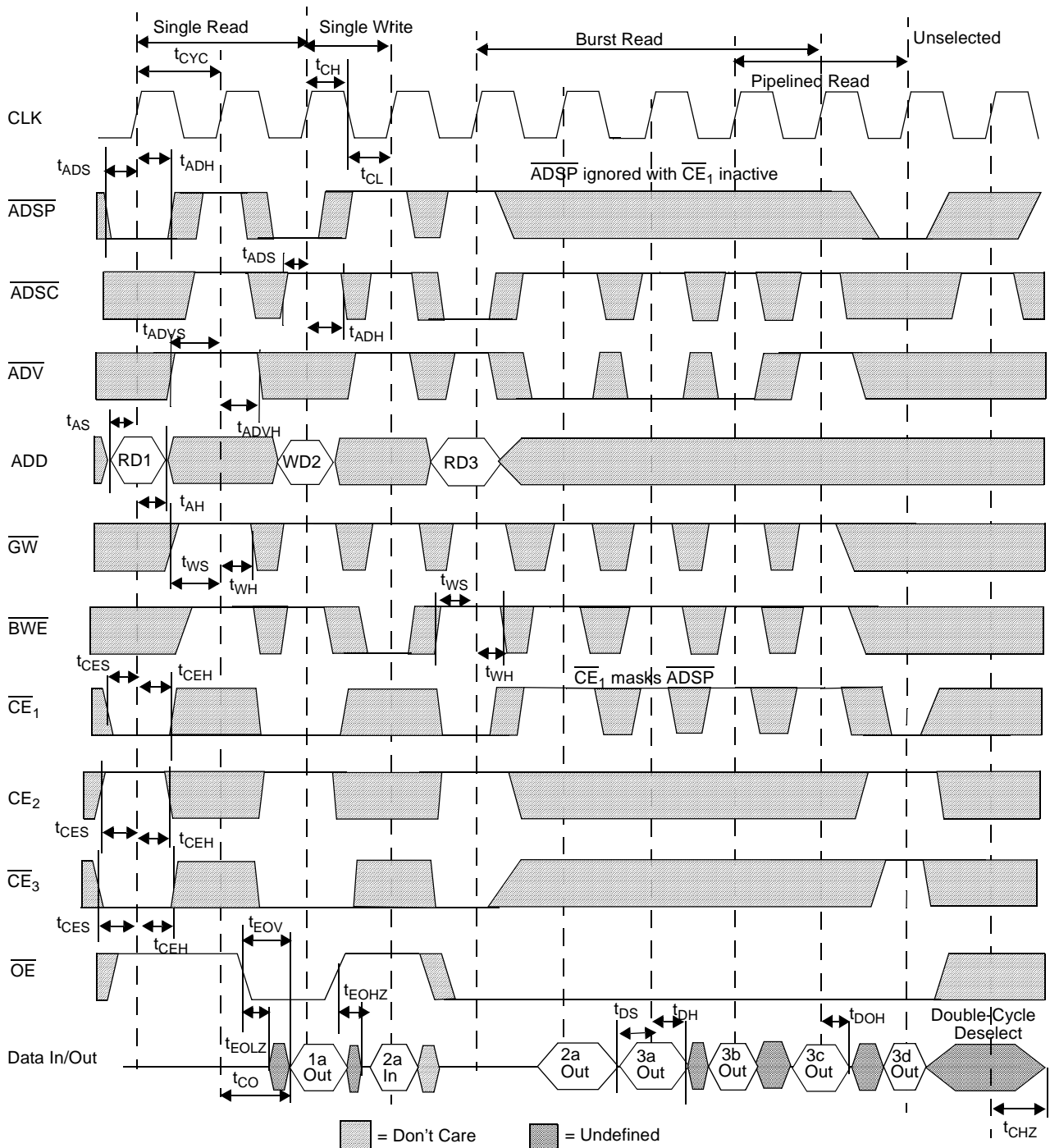
**Switching Waveforms**
**Write Cycle Timing<sup>[4,20,21]</sup>**

**Notes:**

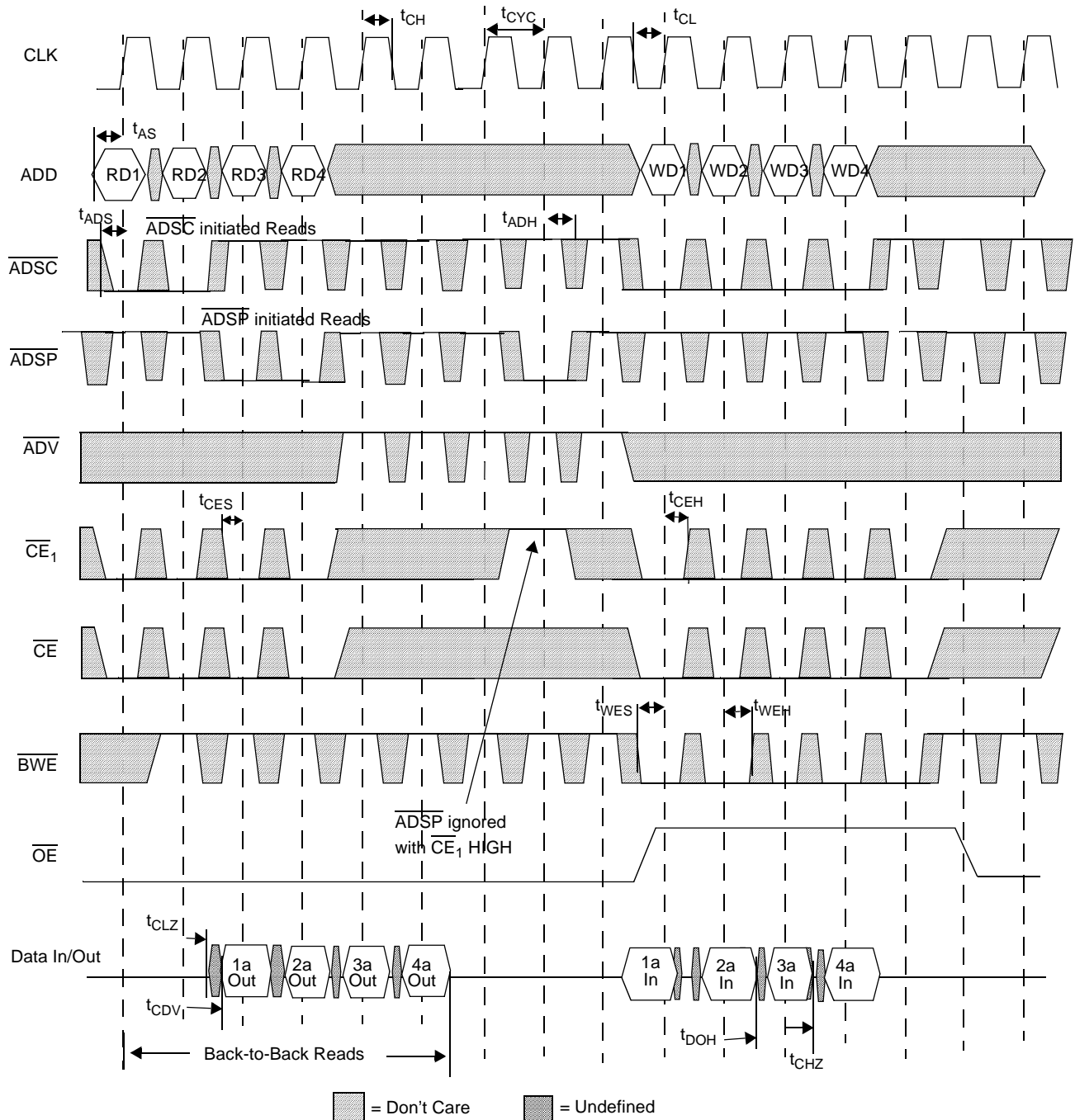
- 20.  $\overline{WE}$  is the combination of  $\overline{BWE}$ ,  $\overline{BWx}$ , and  $\overline{GW}$  to define a Write cycle (see Write cycle descriptions table).
- 21.  $WDx$  stands for Write Data to Address X.

**Switching Waveforms (continued)**
**Read Cycle Timing<sup>[4,20,22]</sup>**

**Note:**

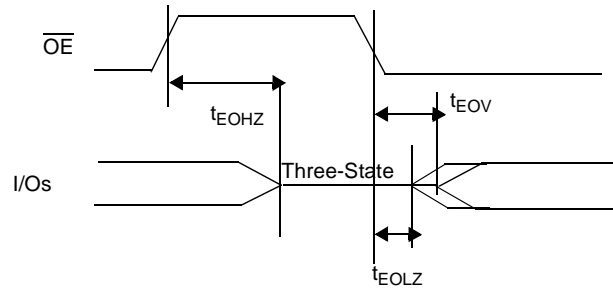
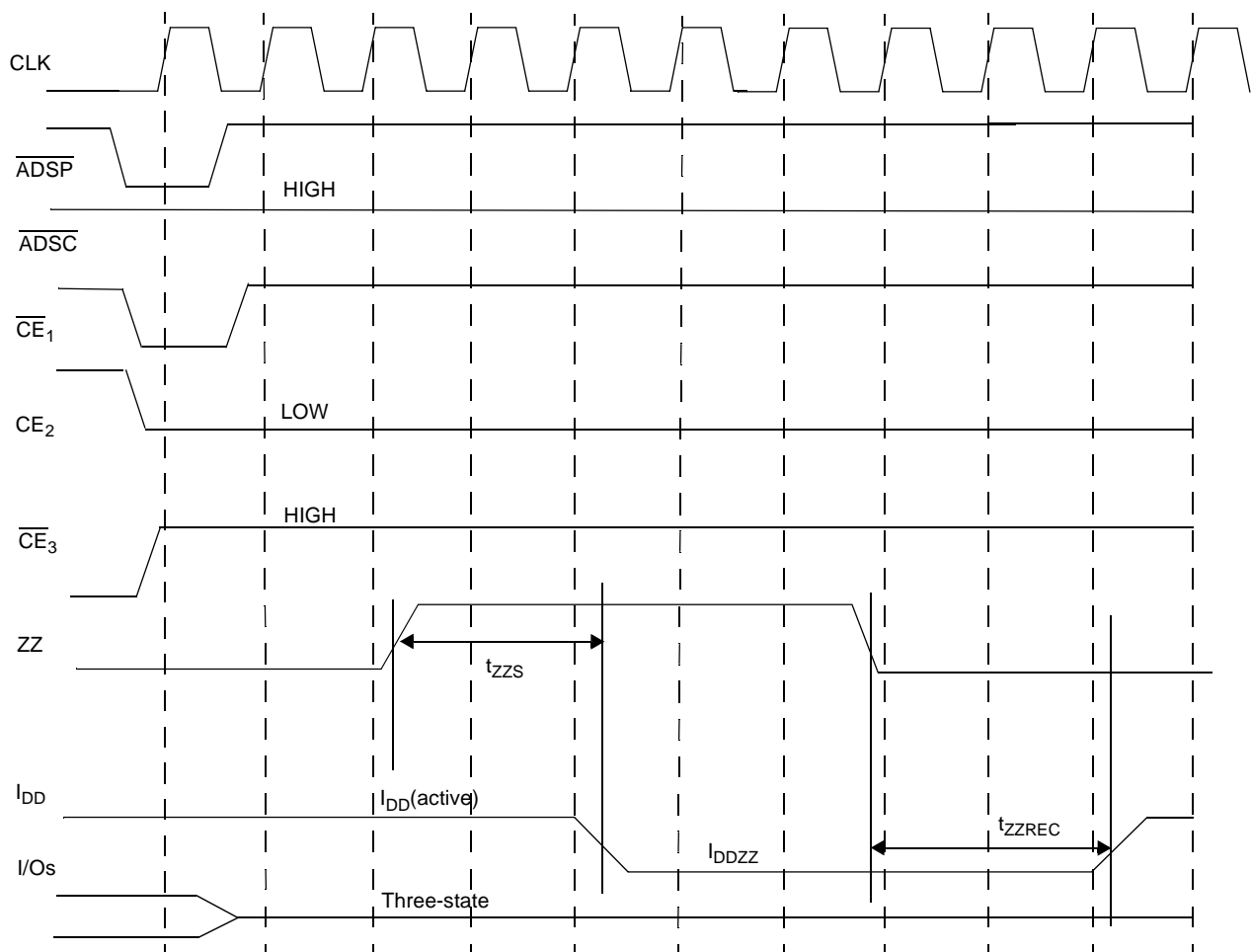
22. RDx stands for Read Data from Address X.



**Switching Waveforms (continued)**
**Read/Write Cycle Timing**<sup>[4,20,21,22]</sup>


**Switching Waveforms (continued)**
**Pipeline Timing<sup>[4,23;24]</sup>**

**Notes:**

23. Device originally deselected.
24.  $\overline{CE}$  is the combination of  $\overline{CE}_2$  and  $\overline{CE}_3$ . All chip selects need to be active in order to select the device.

**Switching Waveforms (continued)**
 **$\overline{OE}$  Switching Waveforms**

**ZZ Mode Timing <sup>[4,25,26]</sup>**

**Note:**

25. Device must be deselected when entering ZZ mode. See Cycle Descriptions Table for all possible signal conditions to deselect the device.
26. I/Os are in three-state when exiting ZZ sleep mode.

**Ordering Information**

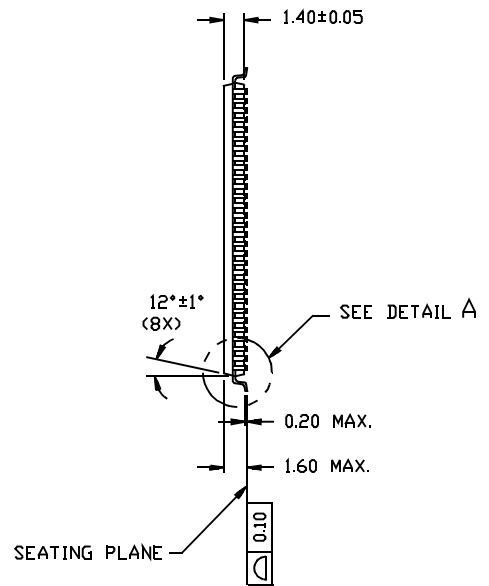
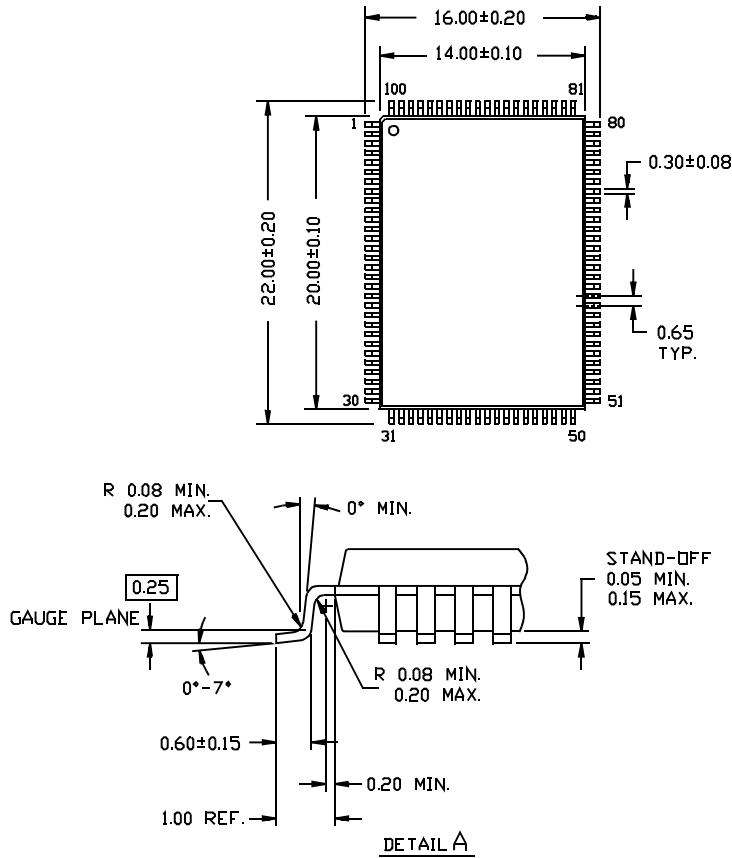
Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CY7C1386B-200AC	A101	100-Lead Thin Quad Flat Pack	Commercial
167	CY7C1386B-167AC			
150	CY7C1386B-150AC			
133	CY7C1386B-133AC			
200	CY7C1387B-200AC			
167	-167AC			
150	-150AC			
133	-133AC			
200	CY7C1386B-200BGC	BG119	119 BGA	
167	CY7C1386B-167BGC			
150	CY7C1386B-150BGC			
133	CY7C1386B-133BGC			
200	CY7C1387B-200BGC			
167	-167BGC			
150	-150BGC			
133	-133BGC			
200	CY7C1386B-200BZC	BB165A	165 FBGA	
167	CY7C1386B-167BZC			
150	CY7C1386B-150BZC			
133	CY7C1386B-133BZC			
200	CY7C1387B-200BZC			
167	-167BZC			
150	-150BZC			
133	-133BZC			
167	CY7C1386B-167AI	A101	100-Lead Thin Quad Flat Pack	Industrial
150	CY7C1386B-150AI			
133	CY7C1386B-133AI			
167	-167AI			
150	-150AI			
133	-133AI			
167	CY7C1386B-167BGI	BG119	119 BGA	
150	CY7C1386B-150BGI			
133	CY7C1386B-133BGI			
167	-167BGI			
150	-150BGI			
133	-133BGI			
167	CY7C1386B-167BZI	BB165A	165 FBGA	
150	CY7C1386B-150BZI			
133	CY7C1386B-133BZI			
167	-167BZI			
150	-150BZI			
133	-133BZI			

Shaded areas contain advance information.

Package Diagrams

100-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm)

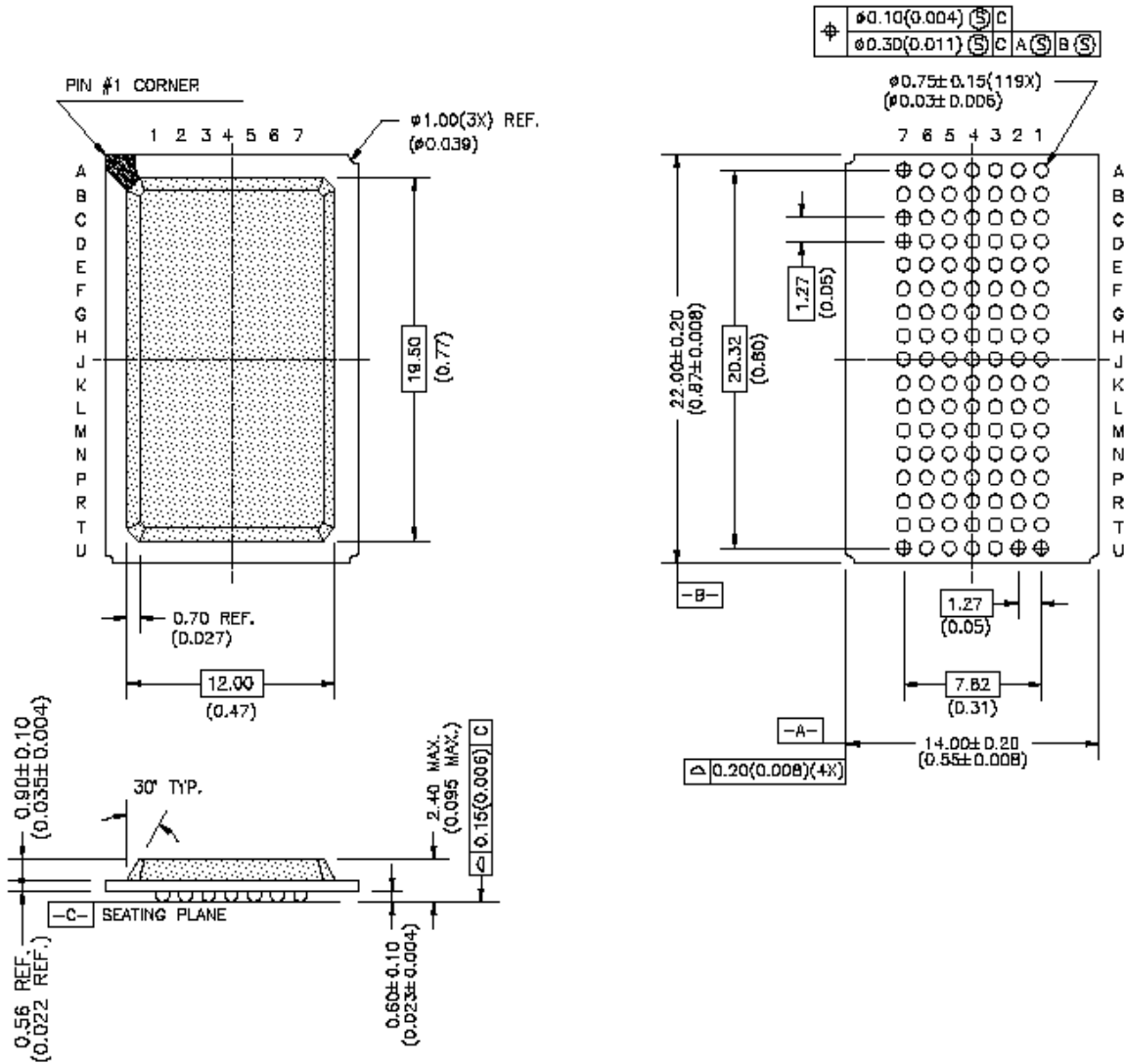
DIMENSIONS ARE IN MILLIMETERS.

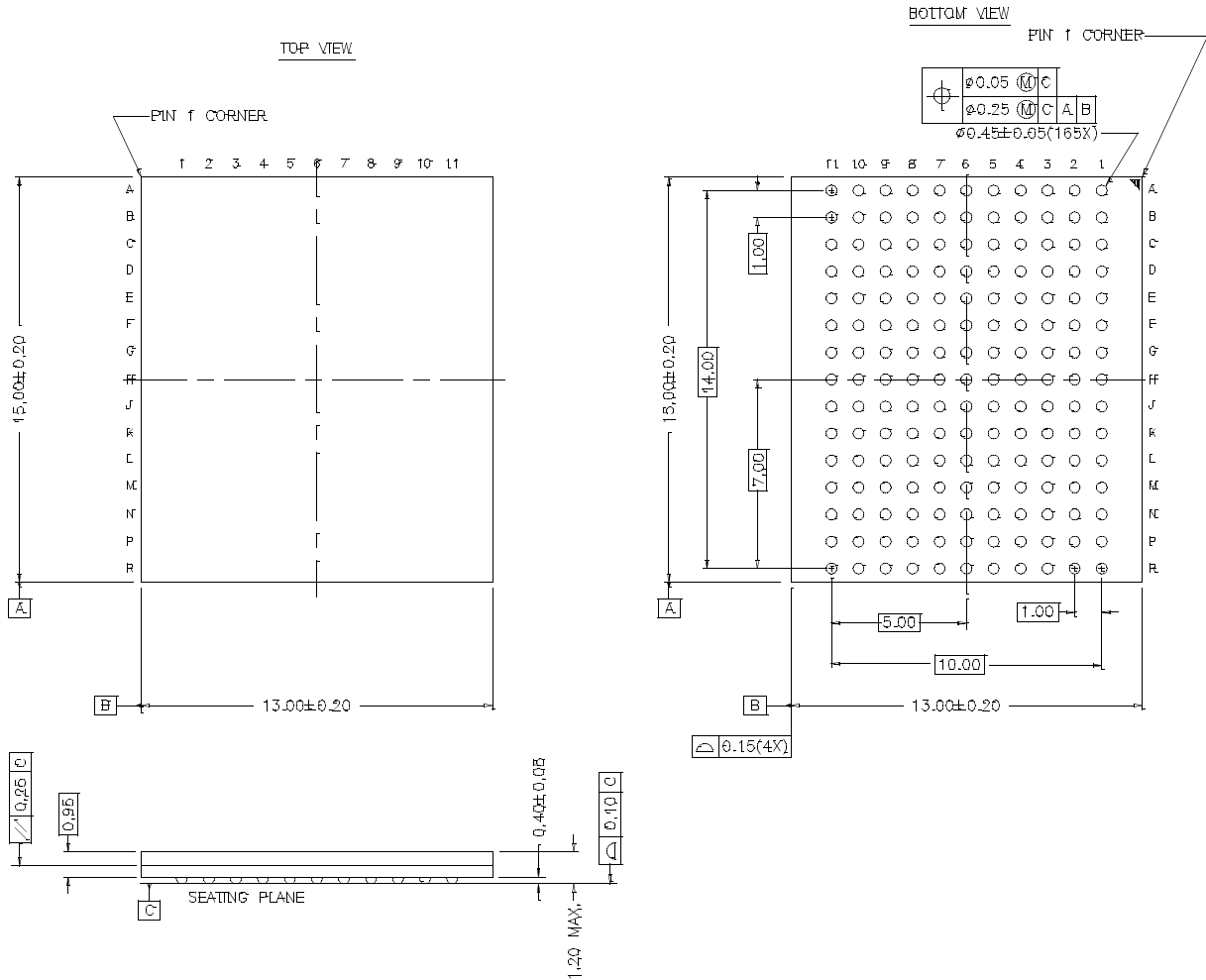


51-85050-A

Package Diagrams (continued)

DIMENSION IN MILLIMETERS (INCHES) 119-Ball BGA (14 × 22 × 2.4 mm)



**Package Diagrams (continued)**
**165-Ball FBGA (13 × 15 × 1.2 mm) BB165A**




**Revision History**

<b>Document Title: CY7C1386B/CY7C1387B 512K x 36/1M x 18 Pipelined DCD SRAM</b>				
<b>Document Number:38-05195</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>ISSUE DATE</b>	<b>ORIG. OF CHANGE</b>	<b>DESCRIPTION OF CHANGE</b>
**	112030	12/09/01	DSG	Change from Spec number: 38-01117 to 38-05195