3.3V VCXO and Low Noise PLL Clock Generator for Digital Video Applications

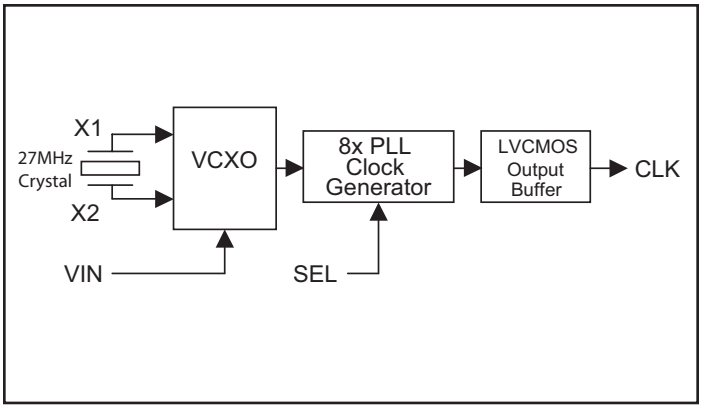
Features

- Fully integrated 24 to 30 MHz VCXO and low phase noise 8x PLL clock genereator
- Uses a SaRonix 27 MHz crystal for optimum performance
- Patented VCXO with wide pull range
- Low phase noise LVCMOS output
- Improved phase noise over the PI6CX230A
- LVCMOS output compatible
- 3.3V ±5% operating voltage
- Packaging (Pb-free & Green):
  —16-pin TSSOP (L)

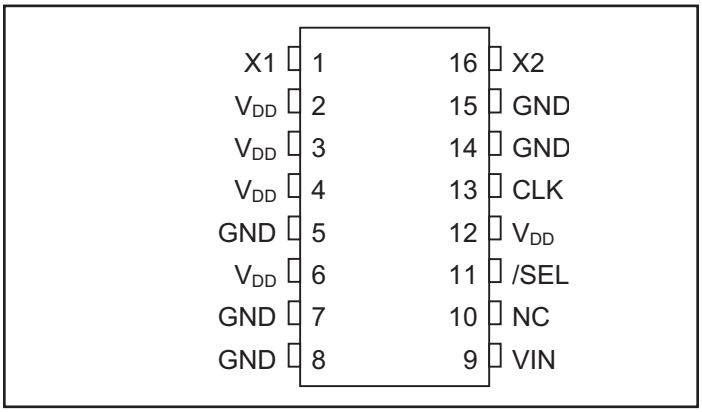
Description

The PI6CX230B is a 3.3V ±5% VCXO and low phase noise 8x PLL clock generator available in discrete IC form with external SaRonix crystal. The PI6CX230B features a low-noise 8x clock multiplication circuit with improved phase noise performance and LVCMOS output clock signal. The device accepts an external analog control voltage signal that pulls the output frequency by ±150 ppM. Contact Pericom/SaRonix for recommended crystal specifications. For applications that require LVDS output compatibility, see the PI6CX231A/B.

Block Diagram



Pin Configuration



Pin Functions

Pin Name	Number	Type	Description
X1, X2	1, 16	I	24 to 30MHz external crystal
V_{DD}	2, 3, 4, 6, 12	PWR	3.3V Positive power supply. Bypass with 0.1µF || 0.01µF capacitors and place as close to the V_{DD} pins as possible.
GND	5, 7, 8, 14, 15	PWR	Ground
VIN	9	I	Analog control VCXO voltage input
/SEL	11	I	Output select. When /SEL is logic HIGH, CLK is logic HIGH. When /SEL is logic LOW, CLK is in normal operation. Contains an internal 100KΩ pull-up.
CLK	13	O	Clock output
NC	10	—	No Connect

Maximum Ratings

Storage Temperature	–55°C to +125°C
Operating Temperature	0°C to +70°C
Supply Voltage V_{DD}	–0.5V to +7V
Inputs/Outputs Voltage	–0.5V to V_{DD} +0.5V
Output Current	50mA
Soldering Lead Temperature (10s)	+260°C
Junction Temperature	–50°C to +150°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

(Unless otherwise specified, V_{DD} = +3.3V ±5%, V_{IN} = 0.5V_{DD}, f_O = 27 MHz, C_{CLK} = 5pF, T_A = 0°C to +70°C)

Symbol	Description	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Operating Supply Voltage		+3.15	+3.3	+3.45	V
I_{DD}	Dynamic Supply Current	f_O = 27 MHz		45	55	mA
V_{IH}	Input HIGH Voltage		+2.0			V
V_{IL}	Input LOW Voltage				+0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -12 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = +12 mA			0.4	V
$R_{PULL-UP}$	Internal Pullup Resistance on SEL input			100		kΩ
f_O	Crystal Input Frequency		24	27	30	MHz

AC Electrical Characteristics

(Unless otherwise specified, V_{DD} = +3.3V ±5%, V_{IN} = 0.5V_{DD}, f_O = 27 MHz, C_{CLK} = 5pF, T_A = 0°C to +70°C)

Symbol	Description	Test Condition	Min.	Typ.	Max.	Units
f_O	Crystal Input Frequency		24	27	30	MHz
T_R/T_F	CLK Rise / Fall Time	Rise Time: 20% to 80% Fall Time: 80% to 20%		0.6	1.0	ns
T_{DC}	CLK Duty Cycle	at V_{DD}/2	48	50	52	%
T_{PN1}	CLK Phase Noise @ 1kHz offset			-104		dBc/Hz
T_{PN2}	CLK Phase Noise @ 10kHz offset			-118		dBc/Hz
T_{PN3}	CLK Phase Noise @ 100kHz offset			-120		dBc/Hz
T_{PN4}	CLK Phase Noise @ 1MHz offset			-116		dBc/Hz
T_{PN5}	CLK Phase Noise @ 10MHz offset			-140		dBc/Hz
T_S	Oscillator Start Time	V_{DD} = 0.9V_{DD}			12	ms
F_{CLK}	CLK Frequency		192	216	240	MHz

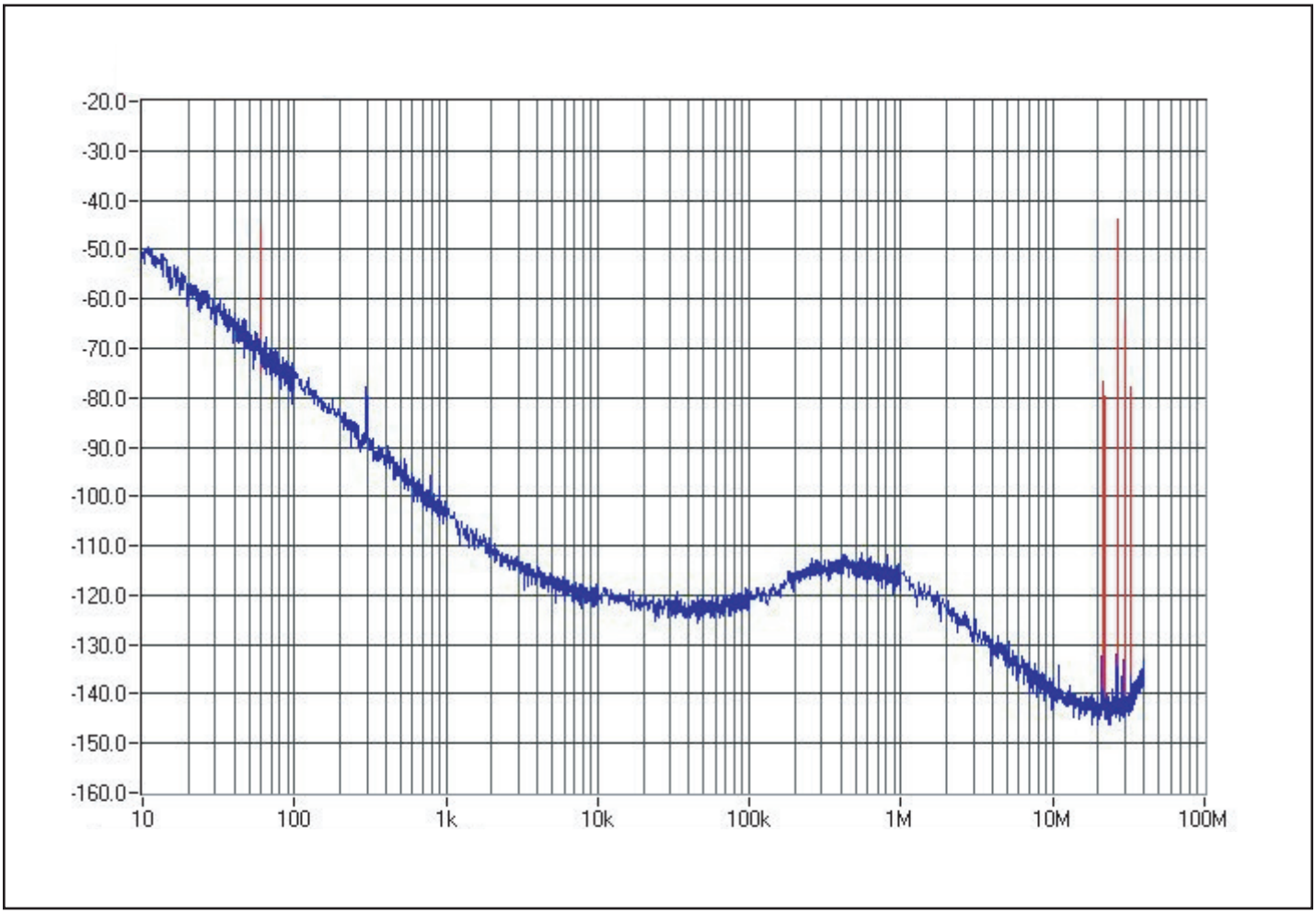
VCXO Electrical Characteristic

(Unless otherwise specified, V_{DD} = +3.3V ±5%, f_O = 27 MHz, C_{CLK} = 5pF, T_A = 0°C to +70°C)

Symbol	Description	Test Condition	Min.	Typ.	Max.	Units
V_{IN}	Control Voltage Input		0		V_{DD}	V
ΔF_{CLK}	Control Pull Range	V_{IN} = 0 to V_{DD}		±150		ppM
L_{IN}	Monotonic Linearity				10	%
MB	Modulation Bandwidth	V_{IN} = 0.5V_{DD}		20		kHz

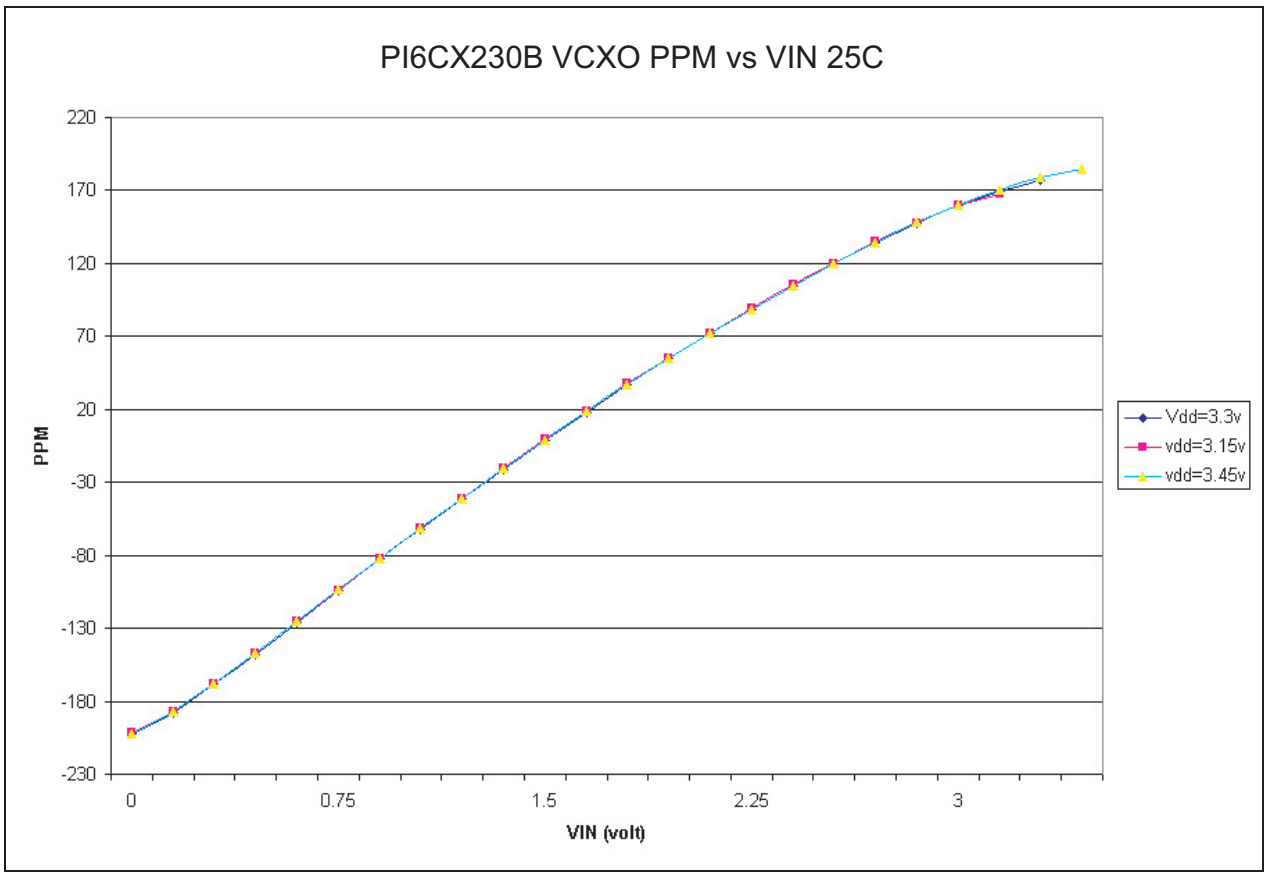
Typical Phase Noise

(Unless otherwise specified, V_{DD} = +3.3V ±5%, V_{IN} = 0.5V_{DD}, f_O = 27 MHz, T_A = 0°C to +70°C)



Typical Pull Characteristics

(Unless otherwise specified, V_{DD} = +3.3V ±5%, f_O = 27 MHz, C_{CLK} = 5pF, C_{LXTAL} = 14pF, T_A = 25°C)

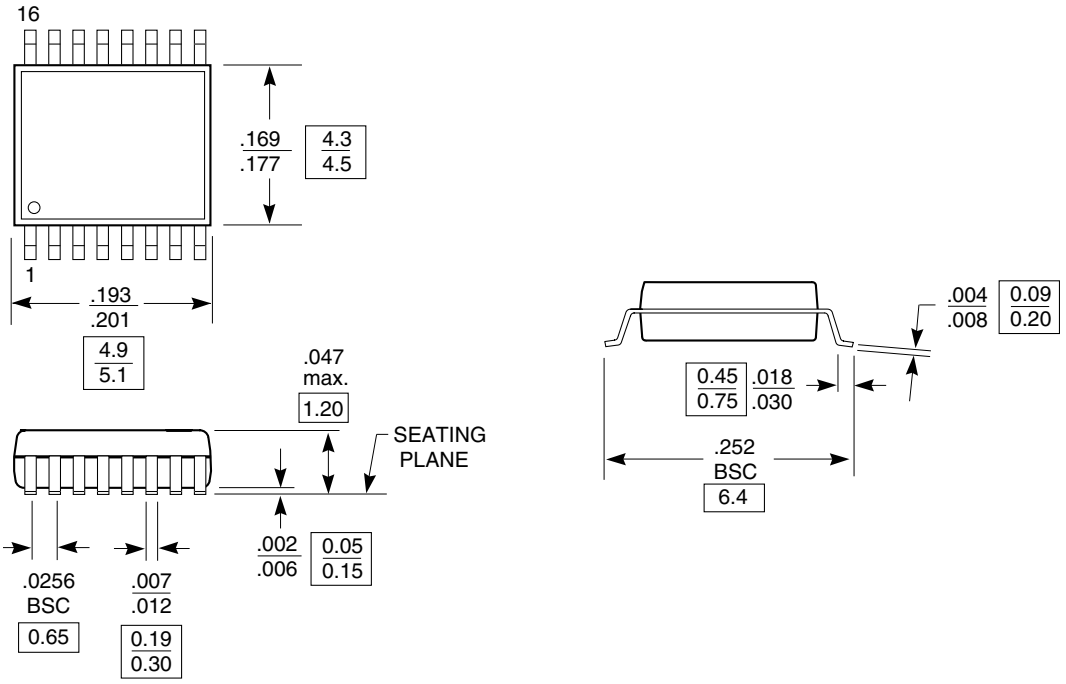


Recommended Crystal: Pericom/Saronix SRX7328 Crystal

The PI6X230B consists of an integrated 27 MHz VCXO and PLL circuit. The VCXO was designed to operate at 27.000 MHz (center frequency),with C_{LXTAL} = 14pF. C_{LXTAL} includes the on-chip + stray + external pull capacitance. The pull capacitors should be placed as close as possible to the PI6CX230B and should be placed on the same side of the board as the PI6CX230B. There should be no signal traces underneath or close to the crystal to prevent coupling of unwanted signals.

Description	Crystal
Mode of Oscillation and Cut	Fundamental AT
Frequency (as specified)	27 MHz
Frequency Tolerance	±20ppm
Temperature plus Aging Stability	±30ppm
C0 /C1	230
Load Capacitance (C_{LXTAL})	14pF
Equivalent Series Resistance (ESR)	25Ω (max.)

Packaging Mechanical: Plastic 16-pin TSSOP (L)



Ordering Information[1,2,3]

Ordering Code	Package Code	Crystal Input (MHz)	Clock Output (MHz)	Package Description
PI6CX230BLE	L	24 to 30	192 to 240 (Crystal x8)	Pb-free & Green, 16-pin TSSOP

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X Suffix = Tape/Reel