PI6C182
PI6C182A

Precision 1-to-10 Clock Buffer

Features

- Low noise non-inverting 1-to-10 buffer
- Supports frequency up to 125 MHz (PI6C182A)
- Supports up to four SDRAM DIMMs
- Low skew (<200ps) between any two output clocks
- I^2C Serial Configuration interface
- Multiple V_{DD} and V_{SS} pins for noise reduction
- 3.3V power supply voltage
- Separate Hi-Z state pin for testing
- Packaging (Pb-free & Green available):
  — 28-pin SSOP (H)

Description

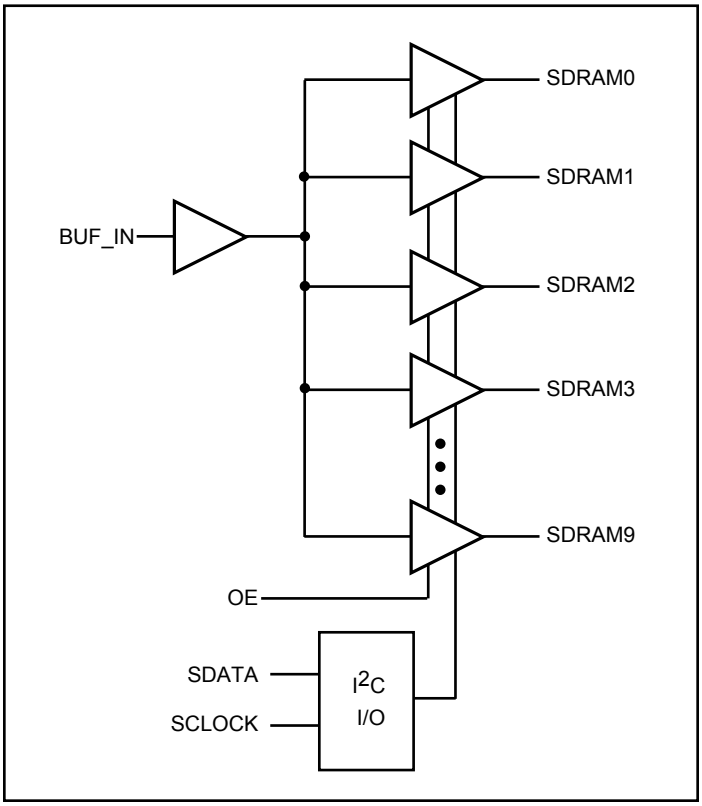
The PI6C182 is a high-speed low-noise 1-to-10 noninverting buffer designed for SDRAM clock buffer applications, supporting frequencies up to 110 MHz.

At power up all SDRAM output are enabled and active. The I^2C serial control may be used to individually activate/deactivate any driver.

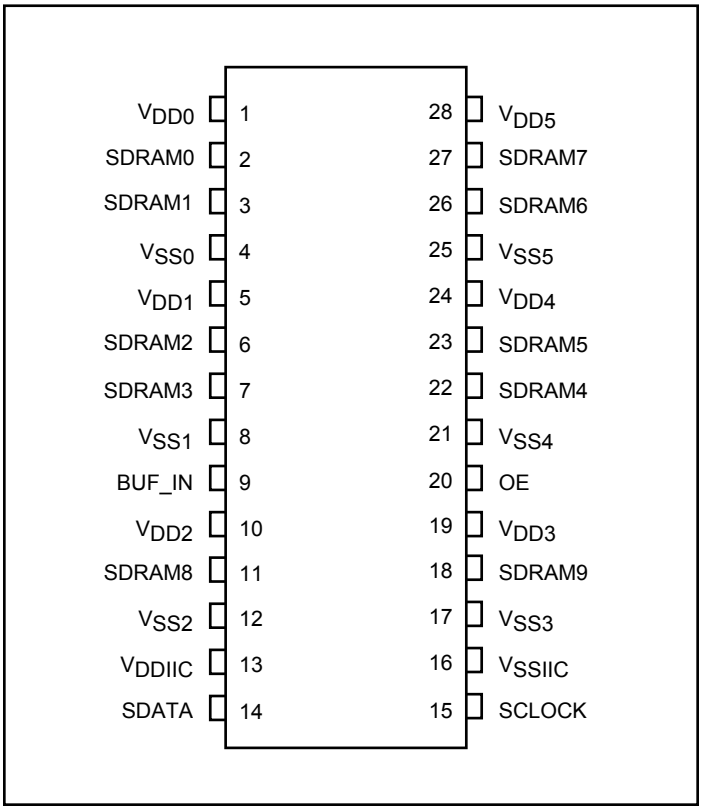
The output enable pin (OE) may be pulled LOW to tri-state all outputs.

Note:
Purchases of I^2C components from Pericom conveys a license of use in I^2C system defined by Philips Semiconductor.

Diagram



Pin Configuration



Pin Description

Pin	Symbol	Type	Qty	Description
2, 3, 6, 7	SDRAM[0-3]	O	4	SDRAM Byte 0 clock output
22, 23, 26, 27	SDRAM[4-7]	O	4	SDRAM Byte 1 clock output
11, 18	SDRAM[8-9]	O	2	SDRAM Byte 2 clock output
9	BUF_IN	I	1	Input for 1-20 buffer
20	OE	I	1	Hi-Z when LOW. Internal 100kΩ pull-up resistor.
14	SDATA	I/O	1	Data pin for I^2C curcuitry. Internal 100kΩ pull-up resistor.
15	SCLOCK	I/O	1	Clock pin I^2C circuitry. Internal 100kΩ pull-up resistor.
1, 5, 10, 19, 24, 28	VDD[0-5]	Power	6	3.3V power supply for SDRAM buffers
4, 8, 12, 17, 21, 25	VSS[0-5]	Ground	6	Ground for SDRAM buffers
13	VDDIIC	Power	1	3.3V power supply for I^2C circuitry
16	VSSIIC	Ground	1	Ground for I^2C circuitry

OE Functionality(1,2)

OE	SDRAM[0-9]
0	Hi-Z
1	BUF_IN

Notes:
1. Used for test purposes only
2. Buffers are non-inverting

I^2C Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	0

Serial Configuration Map(1)

Byte0: SDRAM Active/Inactive Register

(1 = enable, 0 = disable)

Bit	Pin	Description
7		NC (Initialize to 0)
6		NC (Initialize to 0)
5		NC (Initialize to 0)
4		NC (Initialize to 0)
3	7	SDRAM3 (Active/Inactive)
2	6	SDRAM2 (Active/Inactive)
1	3	SDRAM1 (Active/Inactive)
0	2	SDRAM0 (Active/Inactive)

Note:
1. Inactive means outputs are held LOW and are disabled from switching

2-Wire I²C Control

The I²C interface permits individual enable/disable of each clock output and test mode enable.

The PI6C182 is a slave receiver device. It can not be read back. Sub-addressing is not supported. All preceding bytes must be sent in order to change one of the control bytes.

Each byte on the SDATA line must be 8-bits long (MSB first), followed by an acknowledge bit generated by the receiver.
During normal data transfers SDATA changes only when SCLOCK is LOW. Exceptions: A HIGH to LOW transition on SDATA while SCLOCK is HIGH indicates a "start" condition. A LOW to HIGH transition on SDATA while SCLOCK is HIGH indicates a "stop" condition and indicates the end of a data transfer cycle.

Each data transfer is initiated with a start condition and ends with a stop condition. The first byte after a start condition is always a 7-bit address byte followed by a read/write bit. (HIGH = read from addressed device, LOW = write to addressed device). If the device's own address is detected, PI6C182 generates an acknowledge by pulling SDATA line LOW during ninth clock pulse, then accepts the following data bytes until another start or stop condition is detected.

Following acknowledgement of the address byte (D2), two more bytes must be sent:

1. "Command Code" byte
2. "Byte Count" byte.

Although the data bits on these two bytes are "don't care," they must be sent and acknowledged.

Byte1: SDRAM Active/Inactive Register

(1 = enable, 0 = disable)

Bit	Pin	Description
7	27	SDRAM7 (Active/Inactive)
6	26	SDRAM6 (Active/Inactive)
5	23	SDRAM5 (Active/Inactive)
4	22	SDRAM4 (Active/Inactive)
3		NC (Initialize to 0)
2		NC (Initialize to 0)
1		NC (Initialize to 0)
0		NC (Initialize to 0)

Byte2: Optional Register for Possible Future

Requirements (1 = enable, 0 = disable)

Bit	Pin	Description
7	18	SDRAM9 (Active/Inactive)
6	11	SDRAM8 (Active/Inactive)
5		(Reserved)
4		(Reserved)
3		(Reserved)
2		(Reserved)
1		(Reserved)
0		(Reserved)

Maximum Ratings

Storage Temperature.....–65°C to +150°C
Ambient Temperature with Power Applied.....–0°C to +70°C
3.3V Supply Voltage to Ground Potential .....–0.5V to +4.6V
DC Input Voltage.....–0.5V to +4.6V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Supply Current (V_{DD} = +3.465V, C_{LOAD} = Max.)

Symbol	Parameter	Test Condidtion	Min.	Typ.	Max.	Units
I_{DD}	Supply Current	BUF_IN = 0 MHz			2	mA
I_{DD}		BUF_IN = 66.66 MHz			180	
I_{DD}		BUF_IN = 100.00 MHz			240	
I_{DD}		BUF_IN = 133.00 MHz			360	

DC Operating Specifications (V_{DD} = +3.3V ±5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High voltage	V_{DD}	2.0		V_{DD} +0.3	V
V_{IL}	Input Low voltage		V_{SS} -0.3		0.8	
I_{IL}	Input leakage current	0 < V_{IN} < V_{DD}	-5		5	mA
V_{OH}	Output High voltage	I_{OH} = -1mA	2.4			V
V_{OL}	Output Low voltage	I_{OL} = 1mA			0.4	
C_{OUT}	Output pin capacitance			6		pF
C_{IN}	Input pin capacitance			5		
L_{PIN}	Pin Inductance			7		nH
T_A	Ambient Temperature	No Airflow	0		70	°C

SDRAM Clock Buffer Operating Specification

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 2.0V	-40			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			-36	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.0V	40			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			38	

AC Timing

Symbol	Parameter	66 MHz		100 MHz		125MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SDRISE}	SDRAM CLK rise time	1.5	4.0	1.5	4.0	1.5	4.0	V/ns
t_{SDFALL}	SDRAM CLK fall time	1.5	4.0	1.5	4.0	1.5	4.0	
t_{PLH}	SDRAM Buffer LH prop delay	1.0	5.5	1.0	5.5	1.0	5.5	ns
t_{PHL}	SDRAM Buffer HL prop delay	1.0	5.5	1.0	5.5	1.0	5.5	
t_{PZL}, t_{PZH}	SDRAM Buffer Enable delay(1)	1.0	8.0	1.0	8.0	1.0	8.0	
t_{PLZ}, t_{PHZ}	SDRAM Buffer DIsable delay(1)	1.0	8.0	1.0	8.0	1.0	8.0	
Duty Cycle	Measured at 1.5V	45	55	45	55	45	55	%
t_{SDSKW}	SDRAM Output-to-Output skew		250		250		200	ps

Note:
1. This Parameter specified at 5MHz input frequency.

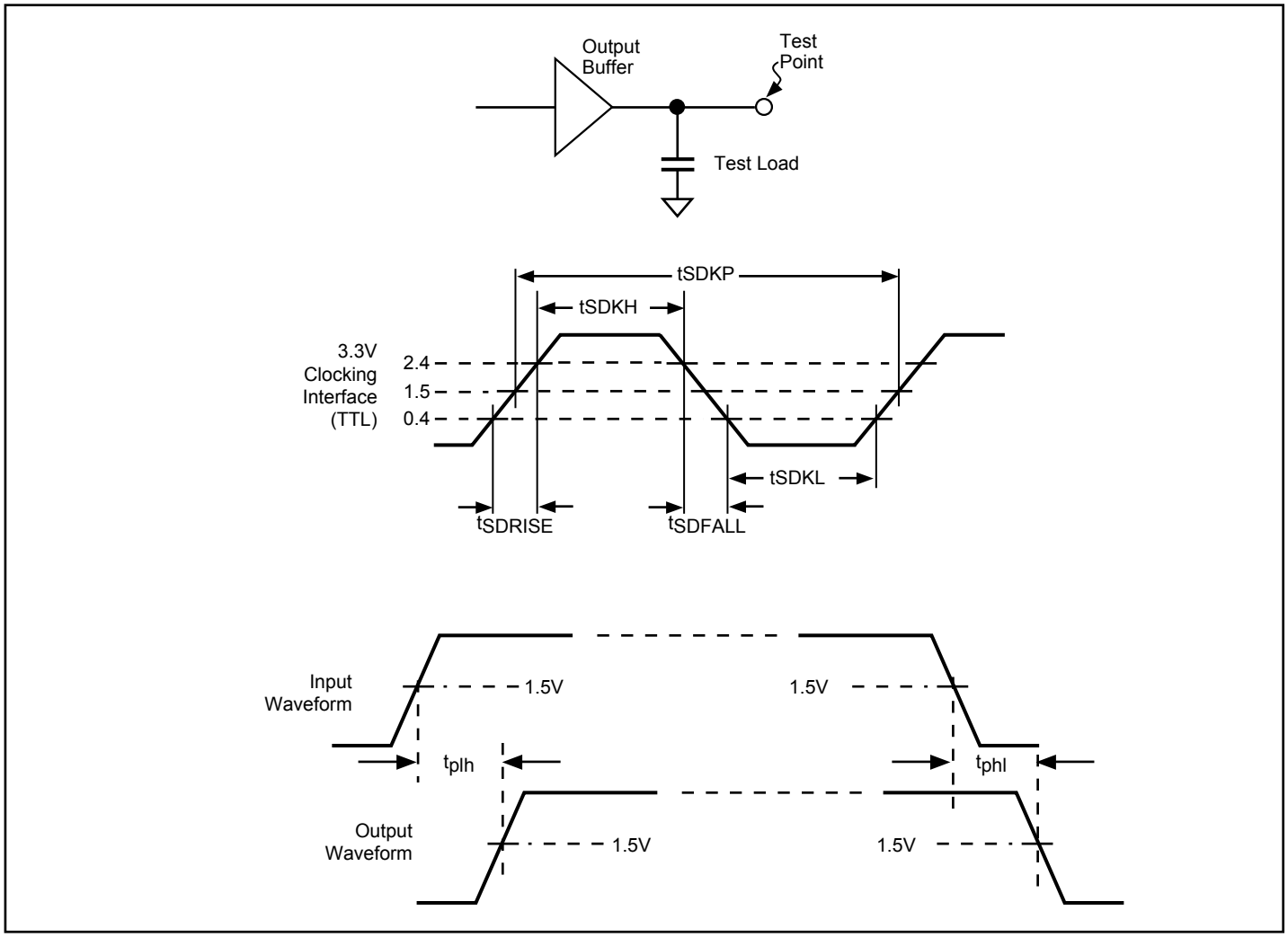


Figure 1. Clock Waveforms

Minimum and Maximum Expected (1,2,3) Capacitive Loads

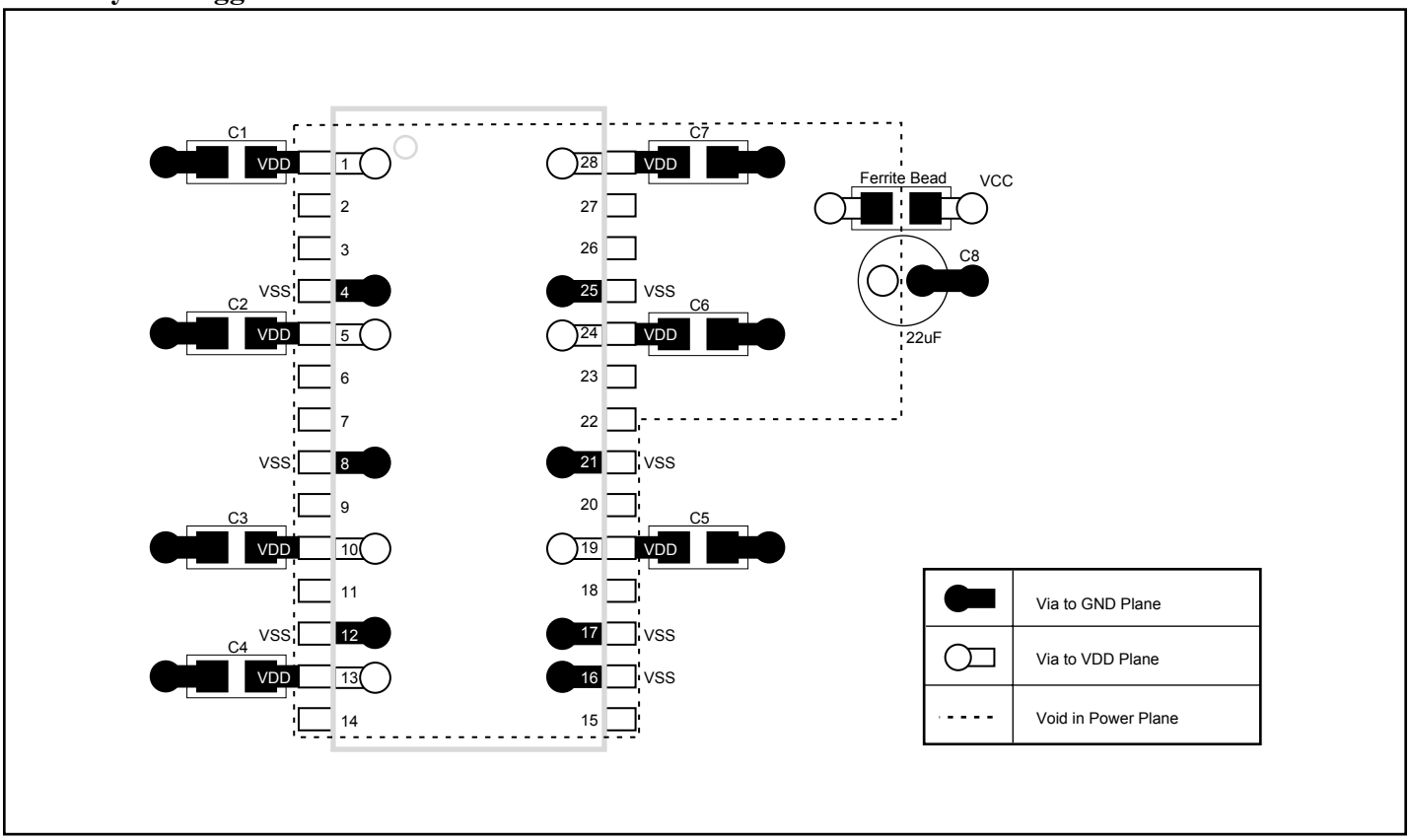
Clock	Min.	Max.	Units	Notes
SDRAM	20	30	pF	SDRAM DIMM Specificaion

Notes:
1. Maximum rise/fall times are guaranteed at maximum specified load.
2. Minimum rise/fall times are guaranteed at minimum specified load.
3. Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.

PCB Layout Suggestion(1,2,3)



Notes:

1. This is only a suggested layout.
2. C1-C7 should be placed as close as possible to their respective VDD.
3. Recommended capacitor values:
   C1-C7 = 0.1µF, ceramic
   C8 = 22µF

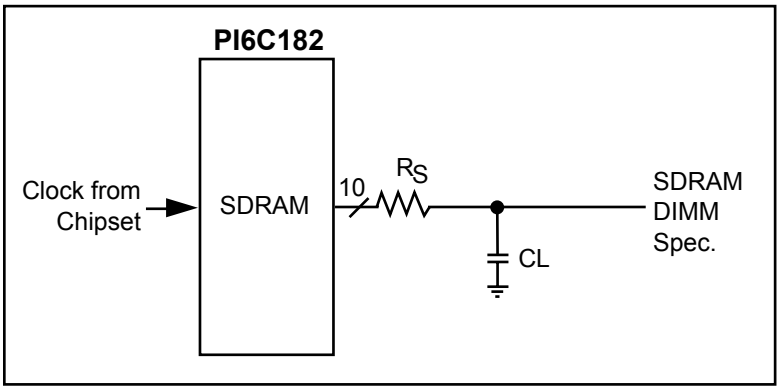
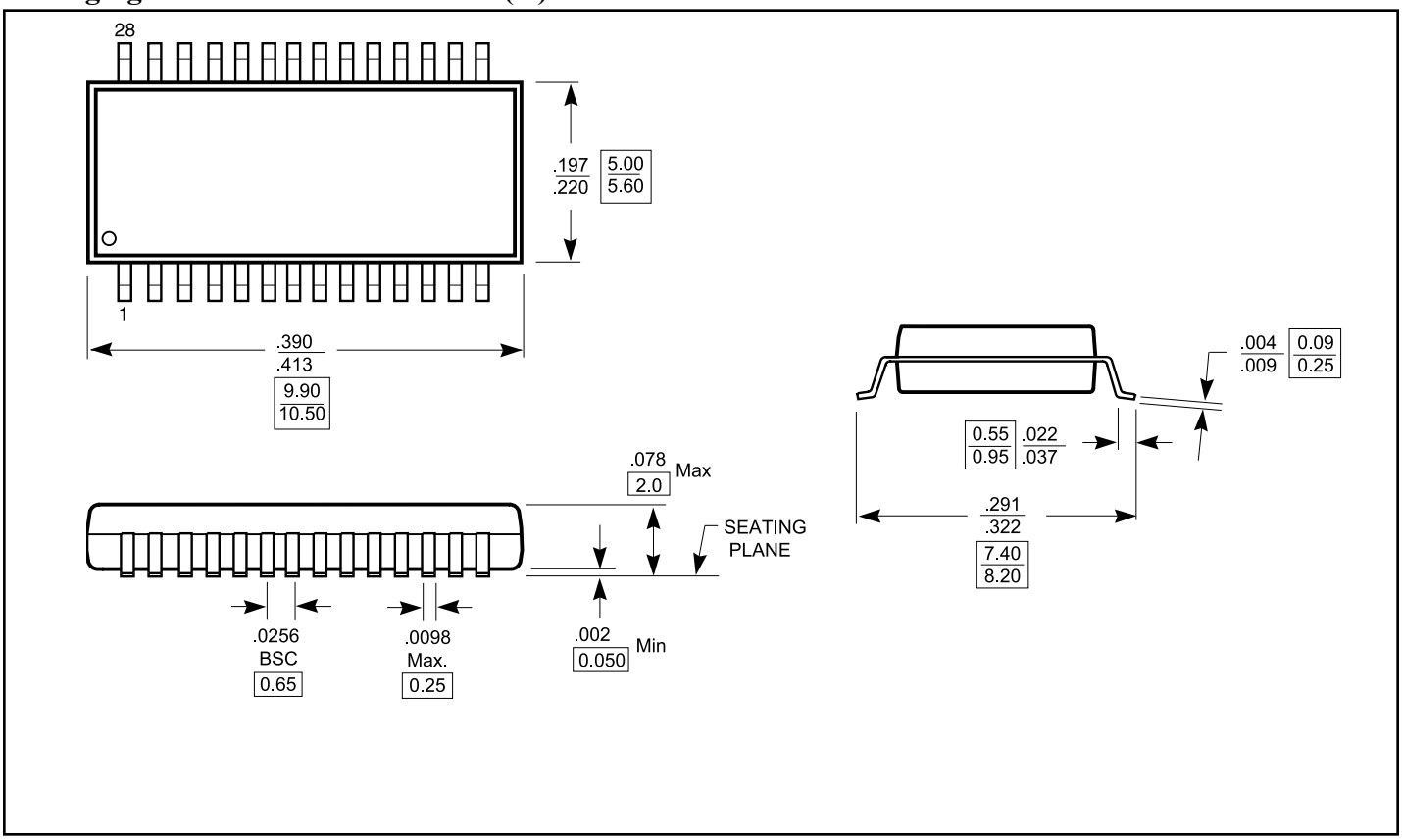


Figure 2. Design Guidelines

Packaging Mechanical: 28-Pin SSOP (H)



Ordering Information[1,2,3]

Ordering Code	Package Code	Package Type
PI6C182H	H	110 MHz 28-pin SSOP
PI6C182AHE	H	125 MHz 28-pin SSOP Pb-free & Green
PI6C182AHEX	H	125 MHz 28-pin SSOP Pb-free & Green, Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. X Suffix = Tape/Reel