PI6C484321

260MHz Crystal-to-3.3V Differential LVPECL Frequency Synthesizer

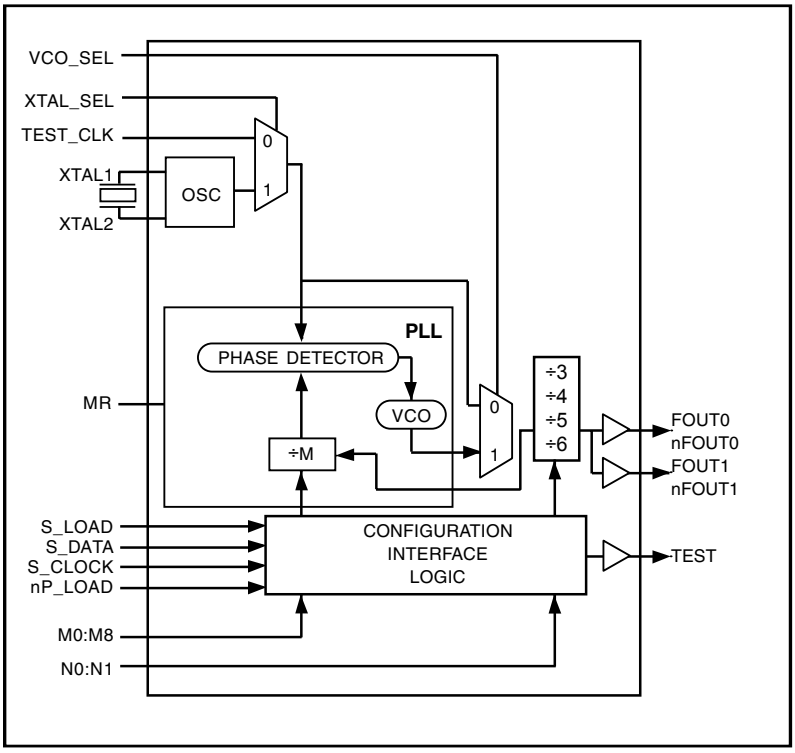
Product Features

- Dual differential 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL TEST_CLK
- Output frequency range: 53.33MHz to 366.67MHz
- Crystal input frequency range: 14MHz to 40MHz
  - TEST_CLK freqeuncy range: 10MHz to 50MHz
- VCO range: 320MHz to 1.1GHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 3ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Packages (Pb-free & Green available):
  - 32-pin LQFP (FB)

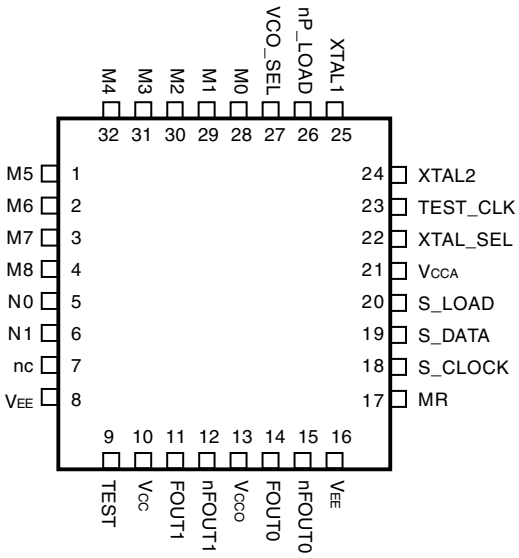
Description

The PI6C484321 is a dual output, 3.3V LVPECL Frequency Synthesizer using crystal as the input source. The input source is can be selected from either LVTTL/LVCMOS level input (TEST_CLK pin) or crystal inputs. The VCO operates at a frequency range of 320MHz to 1.1GHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed through a simple 2-wire serial interface or through 11-bit parallel interface. The low phase noise characteristics of the PI6C484321 make it an ideal clock source for Fibre Channel 1 (FC1), Fibre Channel 2 (FC2), 10 Gigabit Fibre Channel (10GFC), Gigabit Ethernet and 10 Gigabit Ethernet (10GbE) applications.

Block Diagram



Pin Configuration



Functional Description

The following functional description describes operations using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.

The PI6C484321 features a fully integrated PLL, thus requires no external components for setting the loop bandwidth. A fundamental crystal is the input to the internal oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz reference frequency to the phase detector. The actual VCO range of the PLL is 320MHz to 1.1GHz. The output of the M divider is used by the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some illegal values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable feature that selects the M divider and N output divider supports two modes: parallel and serial modes. Figure 1 shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

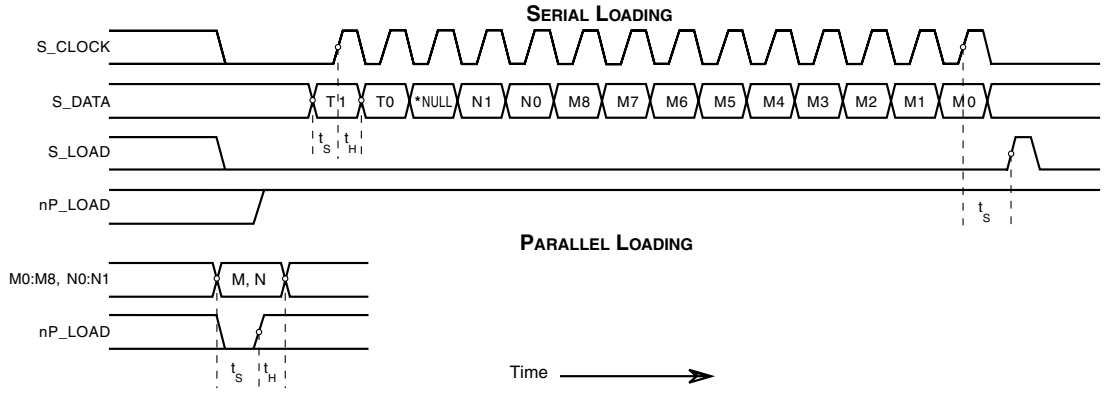
$$fVCO = fxtal \times M$$

The M value and the required values of M0 through M8 are shown in Table 3B to program the VCO Frequency Function Table. The output frequency is defined as follows:

$$fOUT = \frac{fVCO}{N} = fxtal \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data
1	0	Output of M divider
1	1	CMOS Fout



Parallel & Serial Load Operations

Pin Description

Number	Name	Type		Description
1	M5	Input	Pullup	M divider input. Data latched on LOW-to-HIGH transition of nP_ LOAD input. LVCMOS / LVTTL interface levels
2, 3, 4, 28, 29, 30, 31, 32	M6, M7, M8, M0, M1, M2, M3, M4	Input	Pulldown	
5, 6	N0, N1	Input	Pulldown	Determines N output divider value as defined in Table 3C Function table. LVCMOS / LVTTL interface levels
7	nc	unused		No connect
8, 16	V_{EE}	Power		Negative supply pins
9	TEST	Output		Test output. ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS interface levels
10	V_{CC}	Power		Positive supply pin
11, 12	FOUT1, nFOUT2	Output		Differential output for the synthesizer. LVPECL interface levels
13	V_{CCO}	Power		Output supply pin
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. LVPECL interface levels
17	MR	Input	Pulldown	Active High Master reset. When logic HIGH, the internal dividers are reset causing the true outputs FOUTx to go low and the inverted outputs nFOUTx to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
19	S_DATA	Input	Pulldown	Shirft register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
20	S_LOAD	Input	Pulldown	Control transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels
21	V_{CCA}	Power		Analog supply pin
22	XTAL_SEL	Input	Pullup	Selects between crystals or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS / LVTTL interface levels.
23	TEST_CLK	Input	Pulldown	Test clock input. LVCMOS / LVTTL interface levels
24, 25	XTAL1, XTAL2	Input		Crystal oscillator inputs
26	nP_LOAD	Input	Pulldown	Parallel load input to determine when data present at M8:M0 is loaded into M divider, and when data is present at N1:N0 sets the N output divider value. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Controls the clock synthesizer to be in PLL or bypass mode. LVCMOS /LVTTL interface levels

Notes

1. Pullup and Pulldown refer to internal input resistors. See Pin characterstics Table for typical values.

Pin Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance		4		pF
R_{PULLUP}	Input Pullup resistor		51		kΩ
$R_{PULLDOWN}$	Input Pulldown resistor		51		

Parallel and Serial Modes Function Table

Inputs							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset mode, forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N input passed directly to the M divider. TEST output forced LOW
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S-DATA on each rising edge of S_CLOCK
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider
L	H	X	X	↓	L	Data	M divider and N output divider values are latched
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers
L	H	X	X	H	↑	Data	S_Data passed directly to M divider as it is clocked

Notes: L = Low, H = High, X = Don't care, ↑ = Rising Edge, and ↓ = Falling edge Transition

Programmable VCO Frequency Example Based On 25MHz input

VCO Freq.	M Divider	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
625	25	0	0	0	0	1	1	0	0	1
650	26	0	0	0	0	1	1	0	1	0
675	27	0	0	0	0	1	1	0	1	1
775	31	0	0	0	0	1	1	1	1	1

Programmable Output Divider FunctionTable

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Min.	Max.
0	0	3	106.67	366.67
0	1	4	80	275
1	0	5	64	220
1	1	6	53.33	183.33

Notes:
Fout_min = Fvco_min / N = 320MHz / N
Fout_max = Fvco_max /N = 1100MHz / N

Absolute Maximum Ratings

Supply voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, V_O (LVPECL)	-0.5V to V_{DDO} + 0.5V
Outputs, I_O (LVCMOS)	
Continuous current	50mA
Surge current	100mA
Package Thermal Impedance, Theta JA	47.9ºC/W (0 lfpm)
Storage Temperature, T_{STG}	-65º C to 150ºC

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may effect product reliability.

Commonly Used Configuration Function Table

Input			Output Frequency (MHz)
Crystal (MHz)	M Divider Value	N Divider Value	
19.44	32	4	155.52
19.53125	32	4	156.25
25	25	4	156.25
25	25	5	125
25.50	25	3	212.50
25.50	25	4	159.375
25.50	25	6	106.25
38.88	16	4	155.52
20			75
20			83.33

LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, TA = 0°C to 70°C

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, N0:N1, S_DATA, S_CLOCK, M0:M8		2		V_{CC} +0.3V	V
		TEST_CLK		2		V_{CC} +0.3V	
V_{IL}	Input Low Voltage	VCO_SEL, XTAL_SEL, MR, S_LOAD, nP_LOAD, N0:N1, S_DATA, S_CLOCK, M0:M8		-0.3		0.8	
		TEST_CLK		-0.3		1.3	
I_{IH}	Input High Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	$V_{CC} = V_{IN} = 3.465V$			150	µA
		M5, XTAL_SEL, VCO_SEL	$V_{CC} = V_{IN} = 3.465V$			5	
I_{IL}	Input Low Current	M0-M4, M6-M8, N0, N1, MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			
		M5, XTAL_SEL, VCO_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			
V_{OH}	Output High Voltage	TEST(1)		2.6			V
V_{OL}	Output Low Voltage	TEST(1)				0.5	

Notes
1. Outputs terminated with 50Ω to $V_{CC}/2$. See Parameters Measurement Information table, 3.3V Output Load Test Circuit Figure.

Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, TA = 0°C to 70°C

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Positive supply voltage	3.135	3.3	3.465	V
V_{CCA}	Analog supply voltage	3.135	3.3	3.465	
V_{CCO}	Output supply voltage	3.135	3.3	3.465	
I_{EE}	Power supply current			180	mA
I_{CCA}	Analog supply current			30	

LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage(1)		V_{CCO} - 1.4		V_{CCO} -1.0	V
V_{OL}	Output low voltage(1)		V_{CCO} -2.0		V_{CCO} -1.7	
V_{SWING}	Peak-to-Peak output voltage swing		0.6		1.0	

Notes
1. Outputs terminated with 50Ω to V_{CC} -2V. See Parameter Measurement Section, 3.3V output load test circuit.

Input Frequency Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, T_A 0°C to 70°C

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
f_{IN}	Input Frequency	TEST_CLK (1)		14		40	MHz
		XTAL, XTAL2(1)		14		40	
		S_CLOCK				50	

Notes

1. For the input crystal and TEST_CLK frequency range, the M value must be set for the VCO to operate with in the 200MHz to 700MHz range. Using minimum input frequency of 12MHz, valid values of M are $17 \le M \le 58$. Using the maximun frequency of 25MHz, valid values of M are $8 \le M \le 28$.

Crystal Characteristics

Parameter	Test Condition	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental			
Frequency		14		40	MHz
Equivalent Series resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

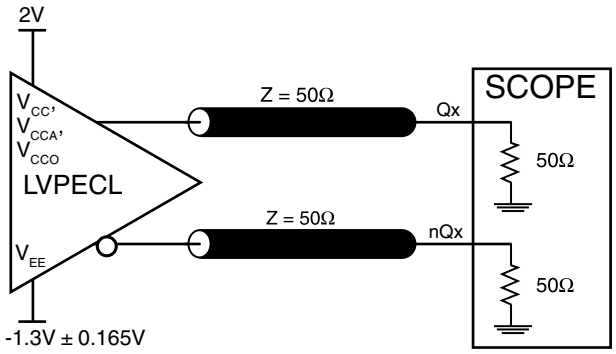
AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output frequency			103.3		260	MHz
tjit(per)	Period jitter, RMS(1, 3)				3	5	ps
tsk(o)	Output skew(2, 3)					15	ps
t_R	Output rise time		20% to 80%	200		700	ps
t_F	Output fall time		20% to 80%	200		700	
t_S	Setup time	Mx, Nx to nP_LOAD		5			ns
		S_DATA to S_CLOCK		5			
		S_CLOCK to S_LOAD		5			
t_H	Hold time	Mx, Nx to nP_LOAD		5			
		S_DATA to S_CLOCK		5			
		S_CLOCK to S_LOAD		5			
odc				45		55	%
t_{LOCK}	PLL lock time					1	ms

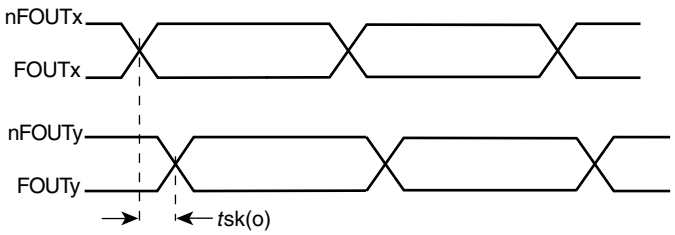
Notes:

1. Jitter performance using XTAL inputs.
2. Defined as skew between outputs with the same supply voltage and with equal load conditions. Measured at the output differential cross points.
3. This parameter is defined in accordance with JEDEC standard 65

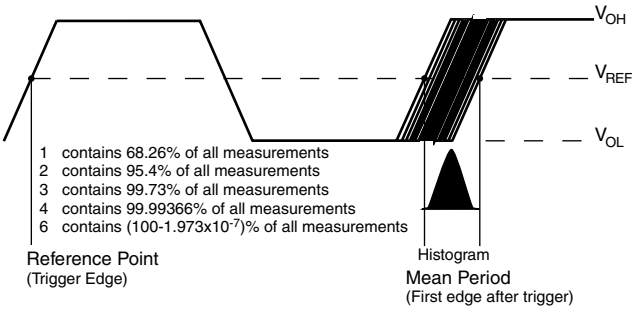
Paramater Measurement Information



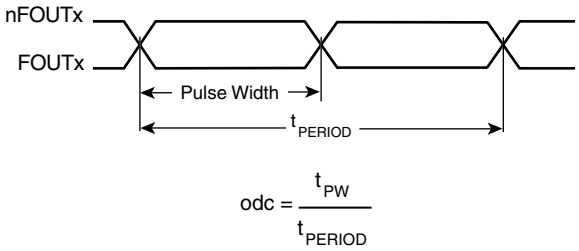
3.3V Output Load Test Circuit



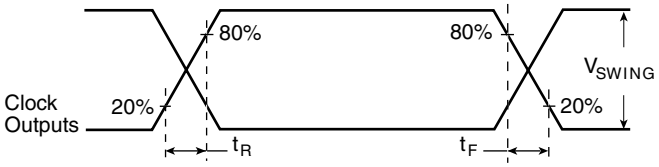
Output Skew



Period Jitter

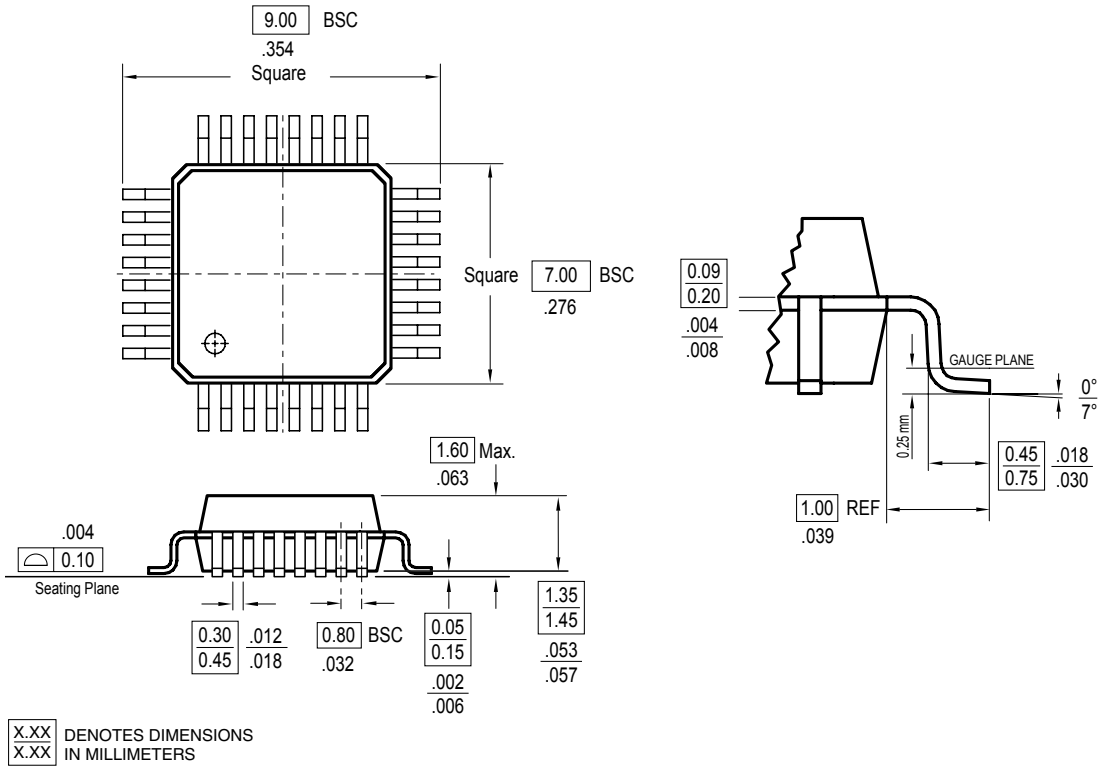


Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Packaging Mechanical: 32-pin LQFP (FB)



Ordering Information

Ordering Code	Package Code	PackageType
PI6C484321FB	FB	32-Pin LQFP
PI6C484321FBE	FB	Pb-free & Green, 32-Pin LQFP

Notes:

1. Thermal characteristics can be found on the company web site at http://www.pericom.com/packaging/