PI6C3991

3.3V High-Speed, Low-Voltage Programmable Skew Clock Buffer

SuperClock®

Features

- All output pair skew <100ps typical (250 Max.)
- 3.75 MHz to 80 MHz output operation
- User-selectable output functions
  - — Selectable skew to 18ns
  - — Inverted and Non-Inverted
  - — Operation at ½ and ¼ input frequency
  - — Operation at 2X and 4X input frequency (input as low as 3.75 MHz, x4 operation)
- Zero input-to-output delay
- 50% duty-cycle outputs
- LVTTL outputs drive 50-ohm terminated lines
- Operates from a single 3.3V supply
- Low operating current
- Available in 32-pin PLCC (J) package
- Jitter < 200ps peak-to-peak (< 25ps RMS)

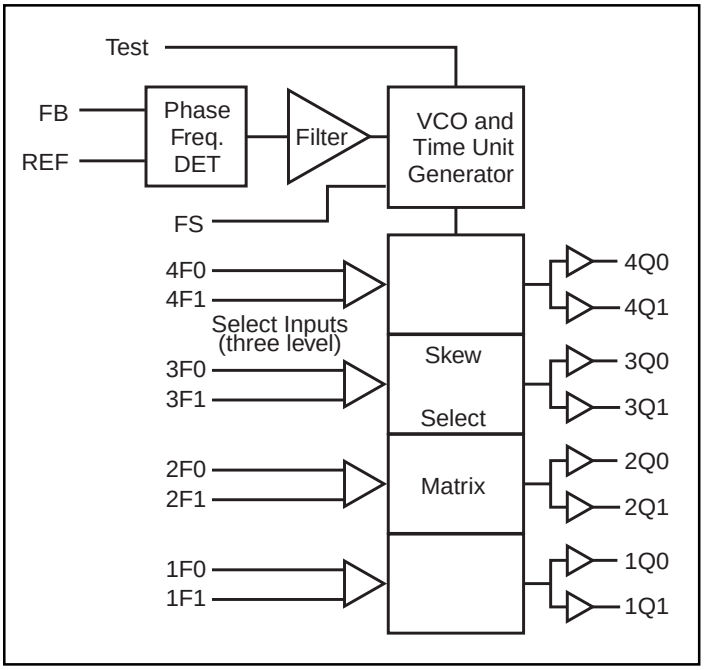
Description

PI6C3991 offers selectable control over system clock functions. These multiple-output clock drivers provide the system integrator with functions necessary to optimize the timing of high-performance computer systems. Eight individual drivers, arranged as four pairs of user-controllable outputs, can each drive terminated transmission lines with impedances as low as 50 ohms while delivering minimal and specified output skews and full-swing logic levels (LVTTL).

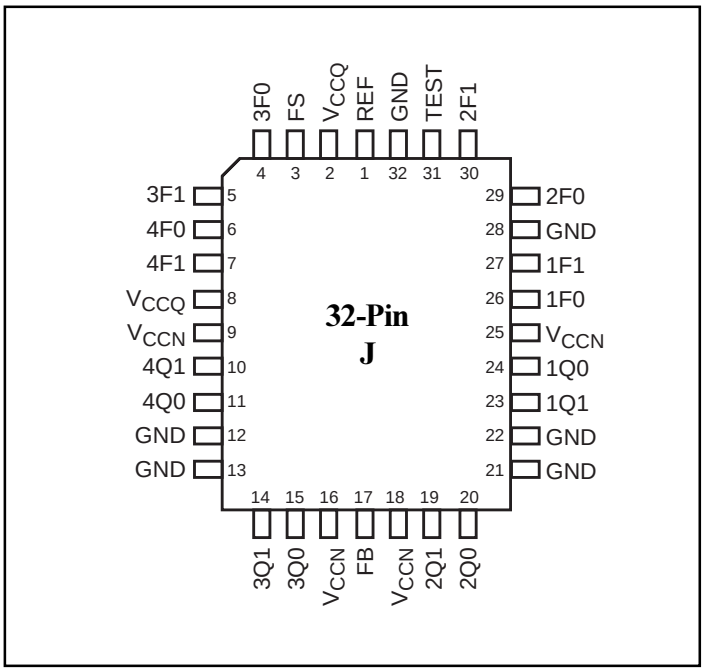
Each output can be hardwired to one of nine skews or function configurations. Delay increments of 0.7ns to 1.5ns are determined by the operating frequency with outputs able to skew up to ±6 time units from their nominal "zero" skew position. The completely integrated PLL allows external load and transmission line delay effects to be canceled. The user can create output-to-output skew up to ±12 time units.

Divide-by-two and divide-by-four output functions are provided for additional flexibility in designing complex clock systems. When combined with the internal PLL, these divide functions allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This feature allows flexibility and simplifies system timing distribution design for complex high-speed systems.

Logic Block Diagram



Pin Configuration



Pin Descriptions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs)
FS	I	Three-level frequency range select. see Table 1.
1F0, 1F1	I	Three-level function select inputs for output pair 1 (1Q0, 1Q1). See Table 2.
2F0, 2F1	I	Three-level function select inputs for output pair 2 (2Q0, 2Q1). See Table 2.
3F0, 3F1	I	Three-level function select inputs for output pair 3 (3Q0, 3Q1). See Table 2.
4F0, 4F1	I	Three-level function select inputs for output pair 4 (4Q0, 4Q1). See Table 2.
TEST	I	Three-level select. See test mode section under the block diagram descriptions
1Q0, 1Q1	O	Output pair 1. See Table 2
2Q0, 2Q1	O	Output pair 2. See Table 2
3Q0, 3Q1	O	Output pair 3. See Table 2
4Q0, 4Q1	O	Output pair 4. See Table 2
V_{CCN}	PWR	Power supply for output drivers
V_{CCQ}	PWR	Power supply for internal circuitry
GND	PWR	Ground

Table 1. Frequency Range Select and t_U Calculation(1)

FS(1,2)	F_{NOM} (MHz)		$t_U = \frac{1}{f_{NOM} \times N}$ where N=	Approximate Freq. (MHz) at which t_U= 1.0ns
	Min.	Max.		
LOW	15	30	44	22.7
MID	25	50	26	38.5
HIGH	40	80	16	62.5

Table 2. Programmable Skew Configurations(1)

Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

Notes:

1. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
2. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) and Time Unit Generator (see Logic Block Diagram). Nominal frequency (f_{NOM}) always appears at 1Q0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be $f_{NOM}/2$ or $f_{NOM}/4$ when the part is configured for a frequency multiplication by using a divided output as the FB input.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept input signals from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO and Time Unit Generator

The VCO accepts analog control inputs from the PLL filter block and generates a frequency that is used by the time unit generator to create discrete time units that are selected in the skew mix matrix. The operational range of the VCO is determined by the FS control pin. The time unit (t_U) is determined by the operating frequency of the device and the level of the FS pin as shown in Table 1.

Skew Select Matrix

The skew select matrix is comprised of four independent sections. Each section has two low-skew, high-fanout drivers (xQ0, xQ1), and two corresponding three-level function select (xF0, xF1) inputs. Table 2 shows the nine possible output functions for each section as determined by the function select inputs. All times are measured with respect to the REF input assuming that the output connected to the FB input has $0t_U$ selected.

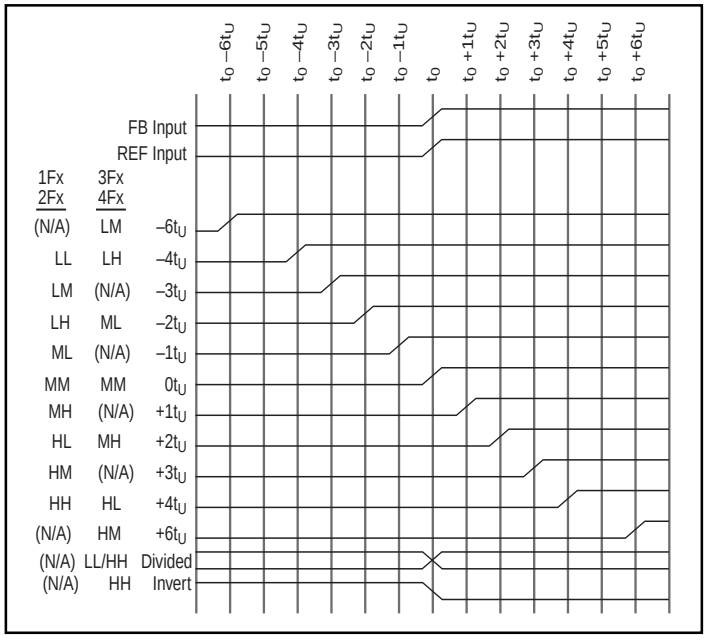


Figure 1. Typical Outputs with FB Connected to a Zero-Skew Output(3)

Test Mode

The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the PI6C3991 to operate as explained briefly above (for testing purposes, any of the three level inputs can have a removable jumper to ground, or be tied LOW through a 100 Ohm resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

In contrast with normal operation (TEST tied LOW). All outputs will function based only on the connection of their own function select inputs (xF0 and xF1) and the waveform characteristics of the REF input.

Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
Output Current into Outputs (LOW)	64mA
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2001V
Latch-Up Current	>200mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ±10%
Industrial	–40°C to +85°C	3.3V ±10%

Note:

3. FB connected to an output selected for "zero" skew (ie., xF1 = xF0 = MID).

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A= 25°C, f = 1MHz, V_{CC}= 3.3V	10	pF

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –12mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 35mA			0.45	
V_{IH}	Input HIGH Voltage (REF & FB inputs only)			2.0	V_{CC}	
V_{IL}	Input LOW Voltage (REF & FB inputs only)			–0.5	0.8	
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS, xFn)[4]	Min. ≤ V_{CC} ≤ Max.		0.87 V_{CC}	V_{CC}	
V_{IMM}	Three-Level Input MID Voltage (Test, FS, xFn)[4]	Min. ≤ V_{CC} ≤ Max.		0.47 V_{CC}	0.53 V_{CC}	
V_{ILL}	Three-Level Input LOW Voltage (Test, FS, xFn)[4]	Min. ≤ V_{CC} ≤ Max.		0.0	0.13 V_{CC}	
I_{IH}	Input HIGH Leakage Current (REF & FB inputs only)	V_{CC} = Max., V_{IN} = Max.			20	µA
I_{IL}	Input LOW Leakage Current (REF & FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V		–20		
I_{IHH}	Input HIGH Current (Test, FS, xFn)	V_{IN} = V_{CC}			200	
I_{IMM}	Input MID Current (Test, FS, xFn)	V_{IN} = V_{CC}/2		–50	50	
I_{ILL}	Input LOW Current (Test, FS, xFn)	V_{IN} = GND		–200		
I_{OS}	Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND (25°C only)			–200	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN} = V_{CCQ} = Max., All Input Selects Open	Com'l		95	
			Mil/Ind		100	mA
I_{CCN}	Output Buffer Current per Output Pair	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0mA All Input Selects Open, f_{MAX}			19	mA
PD	Power Dissipation per Output Pair	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0mA All Input Selects Open, f_{MAX}			104	mW

Notes:

4. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC}/2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.
5. PI6C3991 should be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.
6. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics PI6C3991 (Over the Operating Range)[2,7]

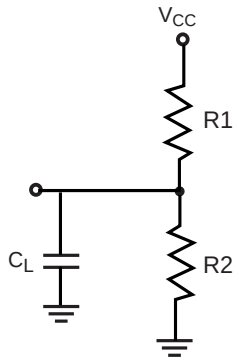
Parameter	Description		PI6C3991-2			PI6C3991-5			PI6C3991			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW [1,2]	15		30	15		30	15		30	MHz
		FS = MID [1,2]	25		50	25		50	25		50	
		FS = HIGH [1,2]	40		80	40		80	40		80	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			5.0			
t_U	Programmable Skew Unit		See Table 1			See Table 1			See Table 1			
t_{SKEWPR}	Zero Output Matched-Pair Skew (XQ0, XQ1) [9,10]			0.05	0.2		0.1	0.25		0.1	0.25	ns
t_{SKEW0}	Zero Output Skew (All Outputs) [9,11]			0.1	0.25		0.25	0.5		0.3	0.75	
t_{SKEW1}	Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) [9,13]			0.1	0.5		0.6	0.7		0.6	1.0	
t_{SKEW2}	Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided)[9,13]			0.5	1.0		0.5	1.0		1.0	1.5	
t_{SKEW3}	Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs)[9,13]			0.25	0.5		0.5	0.7		0.7	1.2	
t_{SKEW4}	Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted[9,13]			0.5	0.9		0.5	1.0		1.2	1.7	
t_{DEV}	Device-to-Device Dkew[8,14]				1.25			1.25			1.65	
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.25	0.0	+0.25	–0.5	0.0	+0.5	–0.7	0.0	+0.7	
t_{ODCV}	Output Duty Cycle Variation[15]		–0.65	0.0	+0.65	–1.0	0.0	+1.0	–1.2	0.0	+1.2	
t_{PWH}	Output HIGH Time Deviation from 50% [16]				2.0			2.5			3	
t_{PWL}	Output LOW Time Deviation from 50%[16]				1.5			3.0			3.5	
t_{ORISE}	Output Rise Time[16,17]		0.15	1.0	1.2	0.15	1.0	1.5	0.15	1.5	2.5	
t_{OFALL}	Output Fall Time[16,17]		0.15	1.0	1.2	0.15	1.0	1.5	0.15	1.5	2.5	
t_{LOCK}	PLL Lock Time[18]				0.5			0.5			0.5	ms
t_{JR}	Cycle-to-cycle Output Jitter	RMS[8]			25			25			25	ps
		Peak-to-peak[8]			200			200			200	

Notes:

7. Test measurement levels for the PI6C3991 are TTL levels (1.5V to 1.5V). Test conditions assume signal transition times of 2ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
8. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
9. SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 30pF and terminated with 50 Ohm to $V_{CC}/2$.
10. t_{SKEWPR} is defined as the skew between a pair of outputs (XQ0 and XQ1) when all eight outputs are selected for $0t_U$.
11. t_{SKEW0} is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted.
12. C_L = 0pF. For C_L = 30pF, t_{SKEW0} = 0.35ns.
13. There are three classes of outputs: Nominal (multiple of t_U delay), Inverted (4Q0 and 4Q1 only with 4F0 = 4F1 = HIGH), and Divided (3Qx and 4Qx only in Divide-by-2 or Divide-by-4 mode).
14. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{CC} ambient temperature, air flow, etc.)
15. t_{ODCV} is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW2} and t_{SKEW4} specifications.
16. Specified with outputs loaded with 30pF for the PI6C3991 and PI6C3991-5 devices. Devices are terminated through 50 Ohm to $V_{CC}/2$. t_{PWH} is measured at 2.0V. t_{PWL} is measured at 0.8V.
17. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V.
18. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

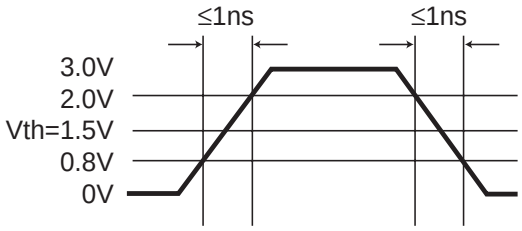
AC Test Loads and Waveforms

TTL AC Test Load

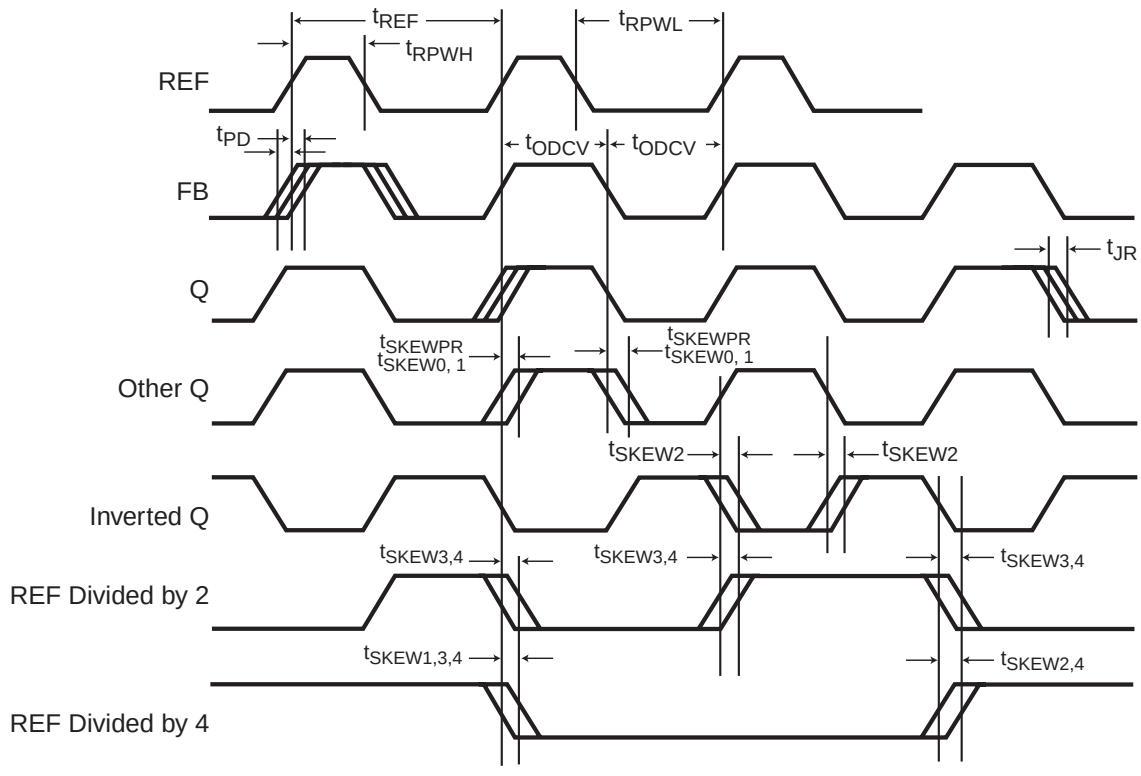


R1=100
R2=100
C_L=30pF
(Includes fixture and probe capacitance)

TTL Input Test Waveform



AC Timing Diagrams



Operational Mode Descriptions

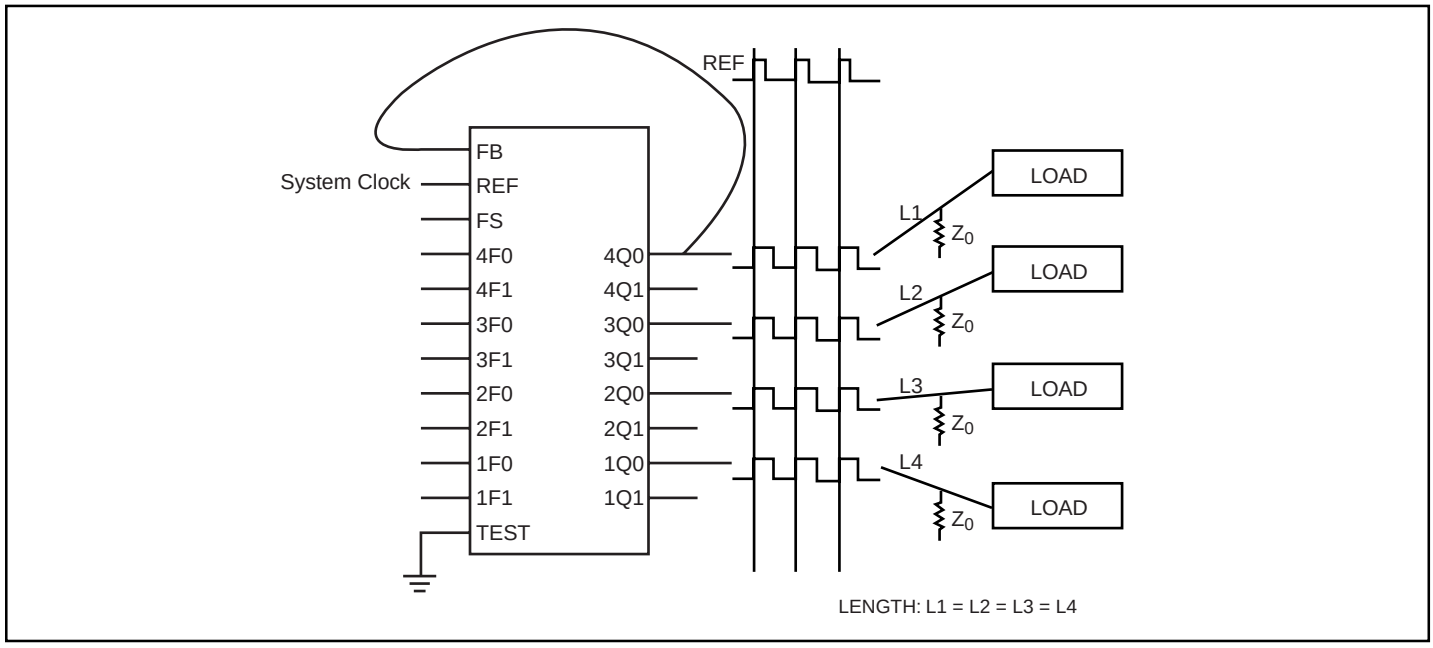


Figure 2. Zero-Skew and/or Zero-Delay Clock Driver

Figure 2 shows the SuperClock configured as a zero-skew clock buffer. In this mode the PI6C3991 can be used as the basis for a low-skew clock distribution tree. When all of the function select inputs (xF0, xF1) are left open, the outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output in this configuration and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 Ohm), allows efficient printed circuit board design.

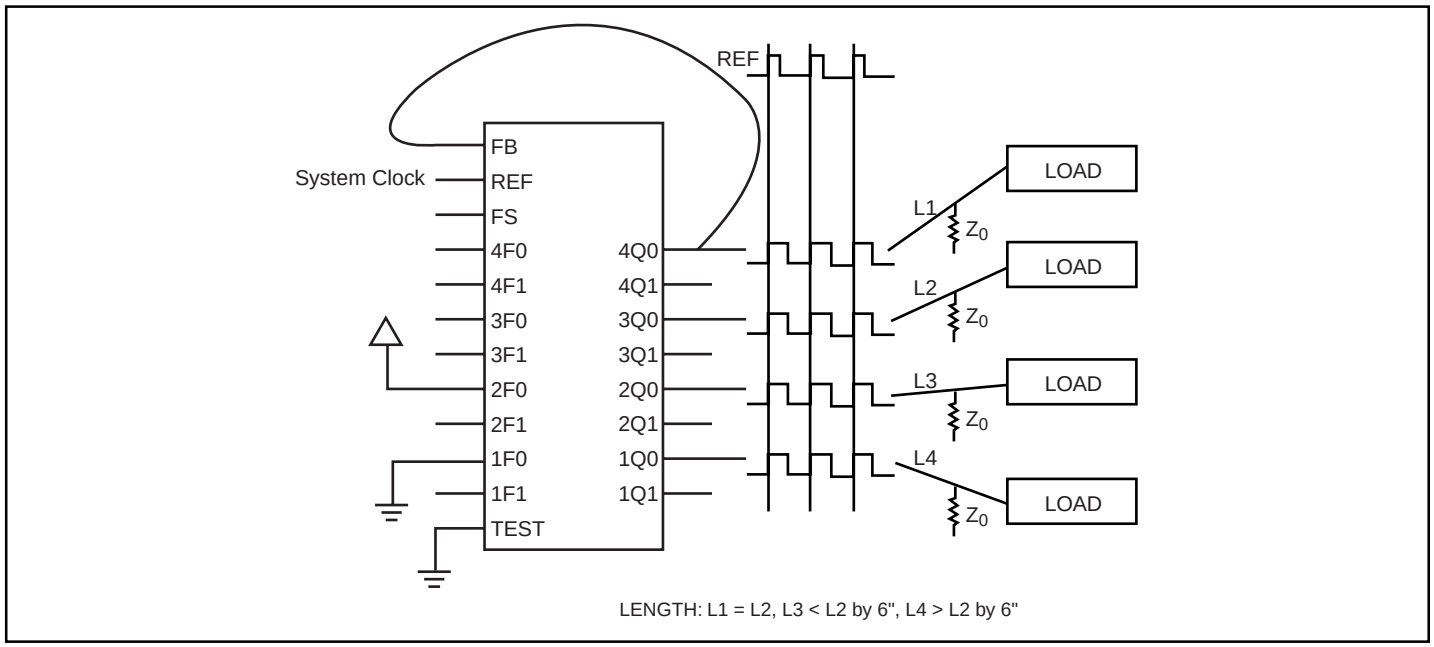


Figure 3. Programmable Skew Clock Driver

Figure 3 shows a configuration to equalize skew between metal traces of different lengths. In addition to low skew between outputs, the SuperClock can be programmed to stagger the timing of its outputs. The four groups of output pairs can each be programmed to different output timing. Skew timing can be adjusted over a wide range in small increments with the appropriate strapping of the function select pins. In this configuration the 4Q0 output is fed back to FB and configured for zero skew.

The other three pairs of outputs are programmed to yield different skews relative to the feedback. By advancing the clock signal on the longer traces or retarding the clock signal on shorter traces, all loads can receive the clock pulse at the same time.

In this illustration the FB input is connected to an output with 0ns skew (xF1, xF0 = MID) selected. The internal PLL synchronizes the FB and REF inputs and aligns their rising edges to insure that all outputs have precise phase alignment.

Clock skews can be advanced by ±6 time units (t_U) when using an output selected for zero skew as the feedback. A wider range of delays is possible if the output connected to FB is also skewed. Since "Zero Skew", $+t_U$, and $-t_U$ are defined relative to output groups, and since the PLL aligns the rising edges of REF and FB, it is possible to create wider output skews by proper selection of the xFn inputs. For example a $+10\ t_U$ between REF and 3Qx can be achieved by connecting 1Q0 to FB and setting 1F0 = 1F1 = GND, 3F0 = MID, and 3F1 = High. (Since FB aligns at $-4\ t_U$ and 3Qx skews to $+6\ t_U$, a total of $+10\ t_U$ skew is realized). Many other configurations can be realized by skewing both the output used as the FB input and skewing the other outputs.

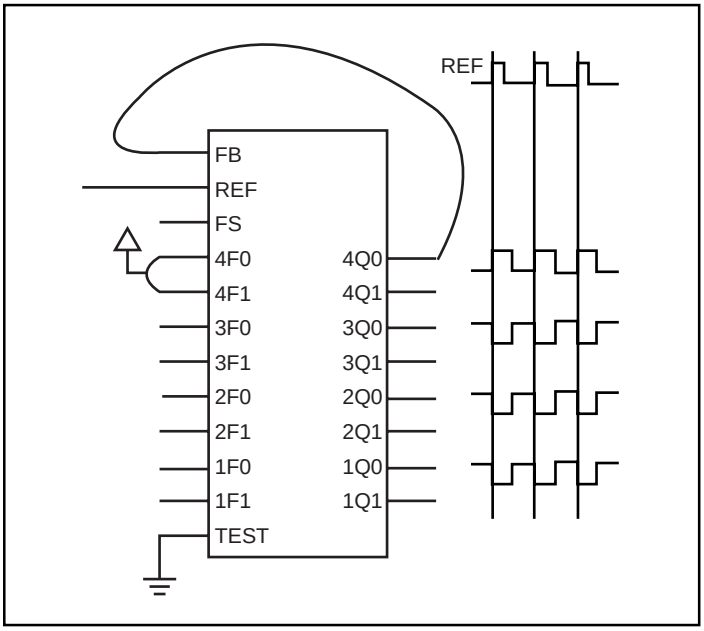


Figure 4. Inverted Output Connections

Figure 4 shows an example of the invert function of the SuperClock. In this example the 4Q0 output used as the FB input is programmed for invert (4F0 = 4F1 = HIGH) while the other three pairs of outputs are programmed for zero skew. When 4F0 and 4F1 are tied HIGH, 4Q0 and 4Q1 become inverted zero phase outputs. The PLL aligns the rising edge of the FB input with the rising edge of the REF. This causes the 1Q, 2Q, and 3Q outputs to become the "inverted" outputs with respect to the REF input. By selecting which output is connect to FB, it is possible to have 2 inverted and 6 non-inverted outputs or 6 inverted and 2 non-inverted outputs. The correct configura-tion would be determined by the need for more (or fewer) inverted outputs. 1Q, 2Q, and 3Q outputs can also be skewed to compensate for varying trace delays independent of inver-sion on 4Q.

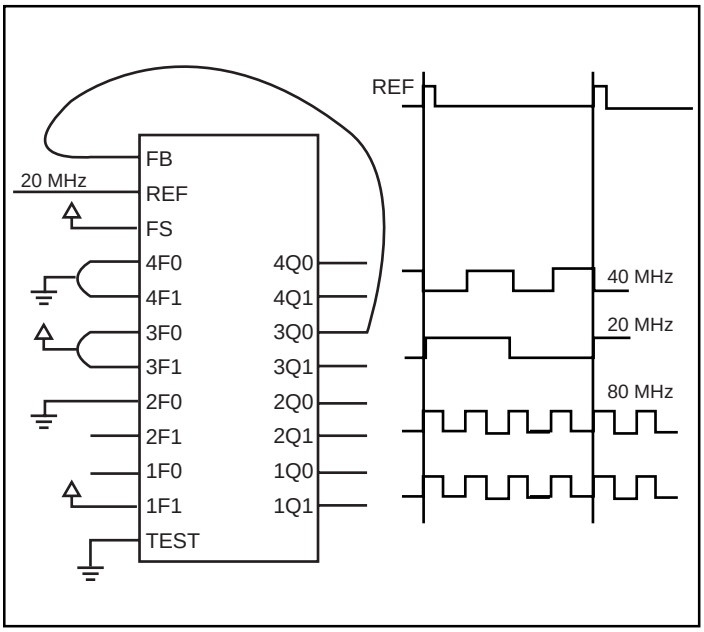


Figure 5. Frequency Multiplier with Skew Connections

Figure 5 illustrates the SuperClock configured as a clock multiplier. The 3Q0 output is programmed to divide by four and is fed back to FB. This causes the PLL to increase its frequency until the 3Q0 and 3Q1 outputs are locked at 20 MHz while the 1Qx and 2Qx outputs run at 80 MHz. The 4Q0 and 4Q1 outputs are programmed to divide by two, which results in a 40 MHz waveform at these outputs. Note that the 20 and 40 MHz clocks fall simultaneously and are out of phase on their rising edge. This will allow the designer to use the rising edges of the ½ frequency and ¼ frequency outputs without concern for rising-edge skew. The 2Q0, 2Q1, 1Q0, and 1Q1 outputs run at 80 MHz and are skewed by programming their select inputs accordingly. Note that the FS pin is wired for 80 MHz operation because that is the frequency of the fastest output.

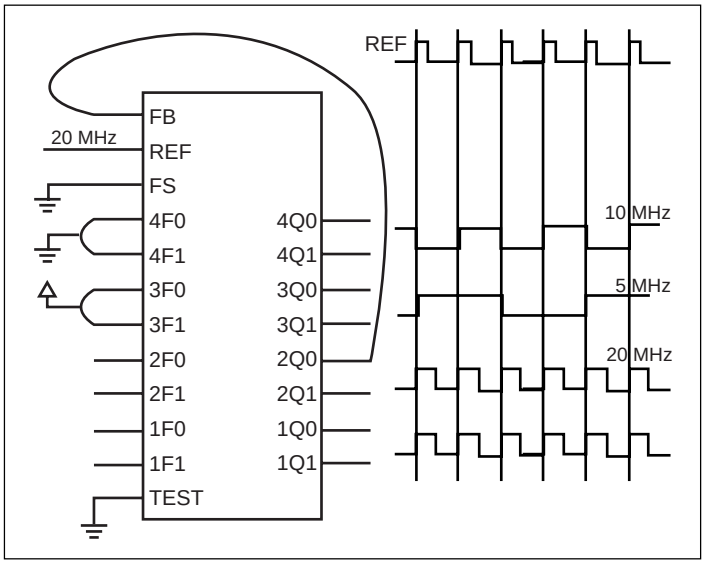


Figure 6. Frequency Divider Connections

Figure 6 demonstrates the SuperClock in a clock divider application. 2Q0 is fed back to the FB input and programmed for zero skew. 3Qx is programmed to divide by four. 4Qx is programmed to divide by two. Note that the falling edges of the 4Qx and 3Qx outputs are aligned. This allows use of the rising edges of the ½ frequency and ¼ frequency without concern for skew mismatch. The 1Qx outputs are programmed to zero skew and are aligned with the 2Qx outputs. In this example, the FS input is grounded to configure the device in the 15 to 30 MHz range since the highest frequency output is running at 20 MHz.

Figure 7 shows some of the functions that are selectable on the 3Qx and 4Qx outputs. These include inverted outputs and outputs that offer divide-by-2 and divide-by-4 timing. An inverted output allows the system designer to clock different sub-systems on opposite edges, without suffering from the pulse asymmetry typical of non-ideal loading. This function allows the two subsystems to each be clocked 180 degrees out of phase, but still to be aligned within the skew spec.

The divided outputs offer a zero-delay divider for portions of the system that need the clock to be divided by either two or four, and still remain within a narrow skew of the "1X" clock. Without this feature, an external divider would need to be add-ed, and the propagation delay of the divider would add to the skew between the different clock signals.

These divided outputs, coupled with the Phase Locked Loop, allow the SuperClock to multiply the clock rate at the REF input by either two or four. This mode will enable the designer to distribute a low-frequency clock between various portions of the system, and then locally multiply the clock rate to a more suitable frequency, while still maintaining the low-skew characteristics of the clock driver. The SuperClock can perform all of the functions described above at the same time. It can multiply by two and four or divide by two (and four) at the same time that it is shifting its outputs over a wide range or maintaining zero skew between selected outputs.

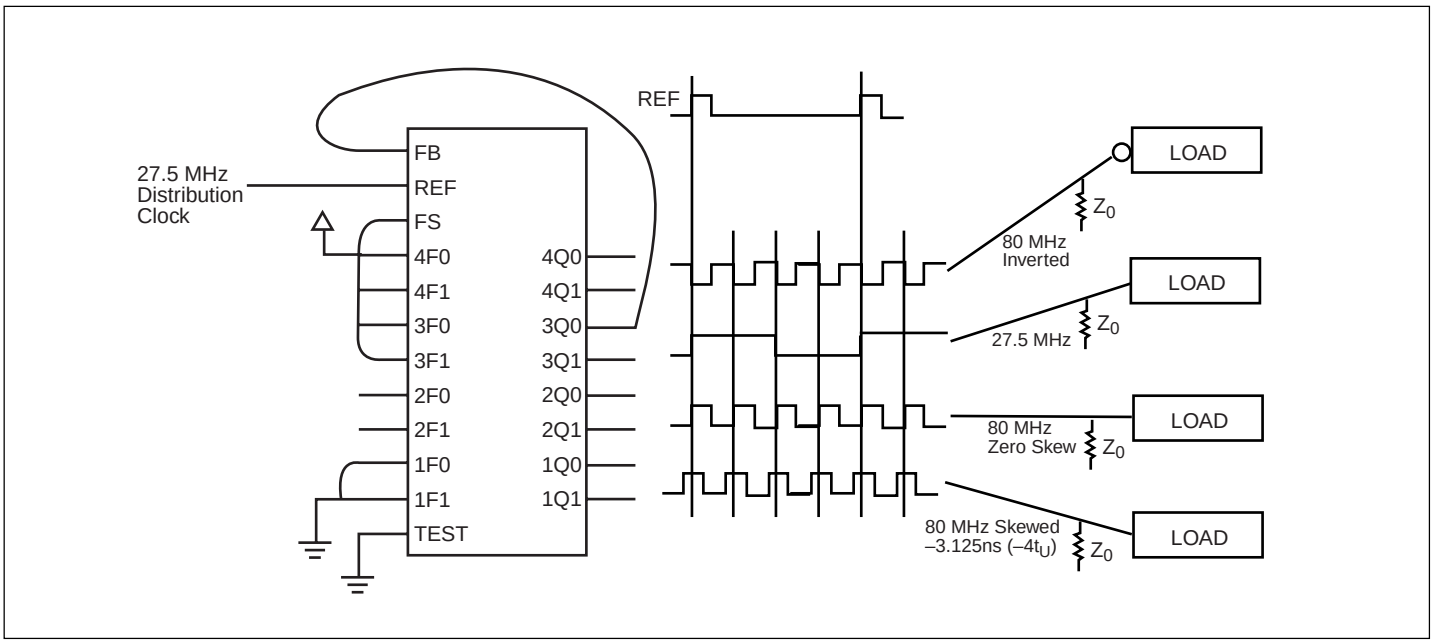


Figure 7. Multi-Function Clock Driver

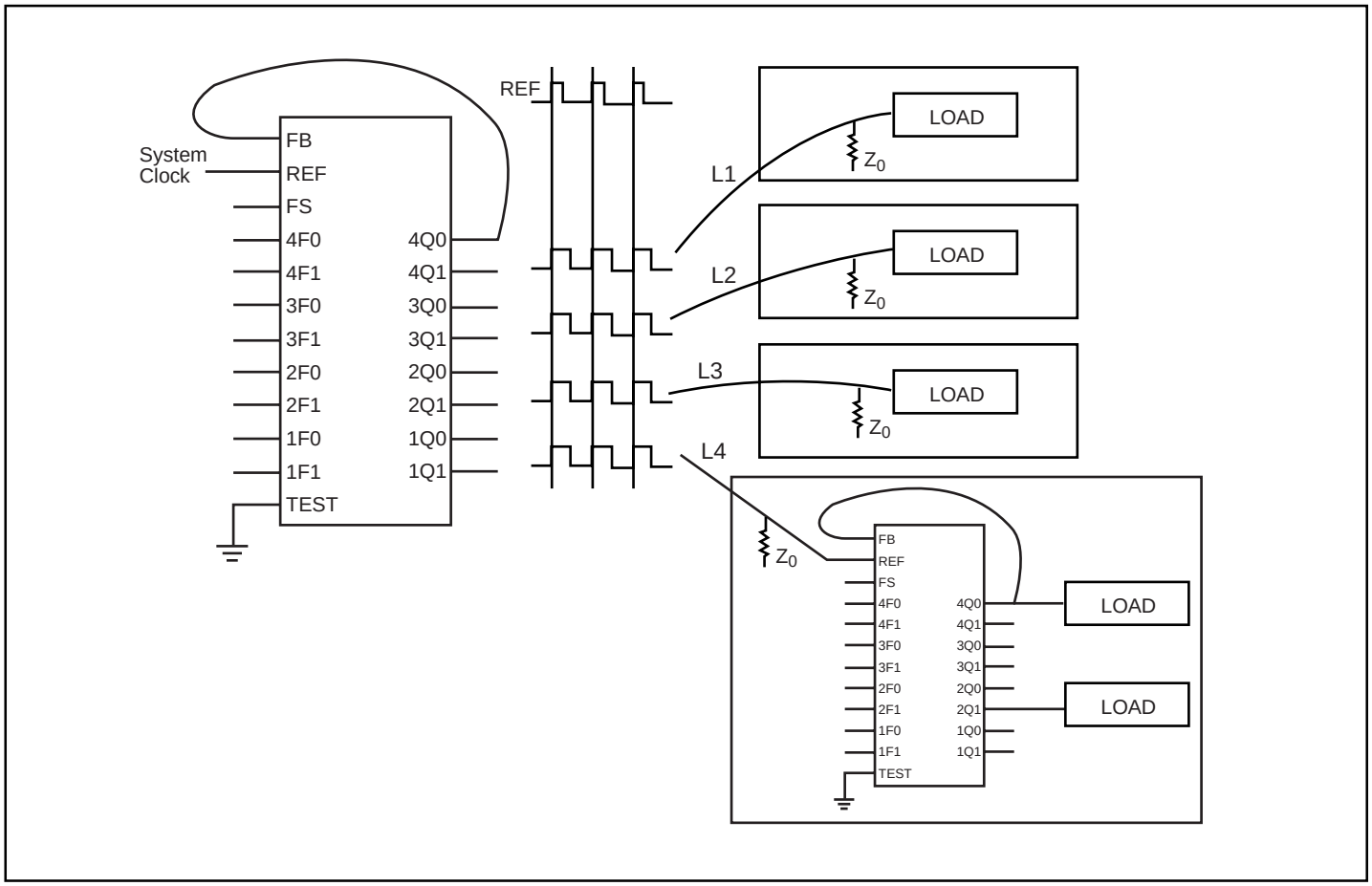
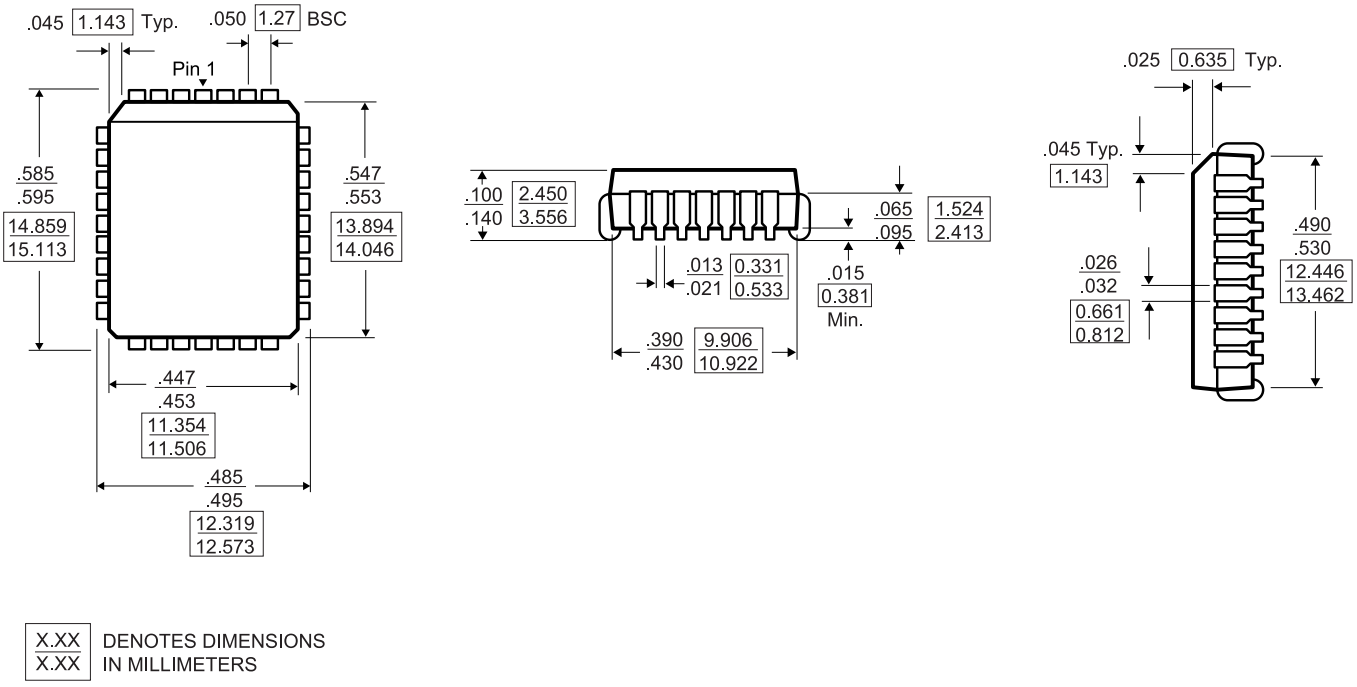


Figure 8. Board-to-Board Clock Distribution

Figure 8 shows the PI6C3991 connected in series to construct a zero skew clock distribution tree between boards. Delays of the down stream clock buffers can be programmed to compensate for the wire length (i.e., select negative skew equal to the wire delay) necessary to connect them to the master clock source, approximating a zero-delay clock tree. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is recommended that not more than two clock buffers be connected in series.

Package Diagram - 32-Pin PLCC (J)



Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
250	PI6C3991-2J	J32	32-Pin Plastic Leaded Chip Carrier	Commercial
500	PI6C3991-5J	J32	32-Pin Plastic Leaded Chip Carrier	Commercial
750	PI6C3991J	J32	32-Pin Plastic Leaded Chip Carrier	Commercial
500	PI6C3991-5IJ	J32	32-Pin Plastic Leaded Chip Carrier	Industrial
750	PI6C3991-IJ	J32	32-Pin Plastic Leaded Chip Carrier	