PERICOM®

PI6C3622

Low Power Spread Spectrum Frequency Multiplier
SSCG-GP Family

Features

- 20 to 40MHz input frequency range
- 1x frequency multiplication
- Operating voltages of 2.5 V or 3.3V
- Selectable Spreading Ratio : ±0.25%, ±0.50%, ±0.70%, ±1.0% and 0% typical at 27MHz input
- Modulation Rate: Fin /640(20 MHz≤ Fin ≤40 MHz)
- Spread Spectrum feature can be enabled/disabled at run-time and glitch-free
- Low power dissipation
- Low jitter
- 8-pin TSSOP Package

Applications

The PI6C3622 can be used in most multimedia applications and embedded systems including but not limited to the following:

- PDAs
- DSCs
- Printers/ MFPs
- Media players
- Portable-TVs
- Embedded digital video devices
- CD-ROM, VCD and DVD players
- LCD Panel Modules
- Automotive components
- Networking devices

Description

The PI6C3622 is a Low Power Spread Spectrum Frequency Multiplier and part of the Pericom SSCG-GP family. The part generates one 1x modulated output from a single clock source or a crystal, and is designed to reduce electromagnetic interference (EMI) by spreading the clock. This reduction in EMI can result in significant system cost saving and less design complexity by reducing the number of circuit board layers ferrite beads and shielding. In the absence of a spread spectrum clock, other EMI-reducing components are required in order to comply with regulatory agency requirements.

The Spreading Ratio is selectable using the selection pins. The PI6C3622 provides ±0.25%, ±0.50%, ±0.70%, ±1.0% diversified and 0% spread modulation through external logic stage setting. The Spread Spectrum feature can be enabled and disabled at run-time by setting the SSON pin. Other pins should be properly set before the system is initialized.

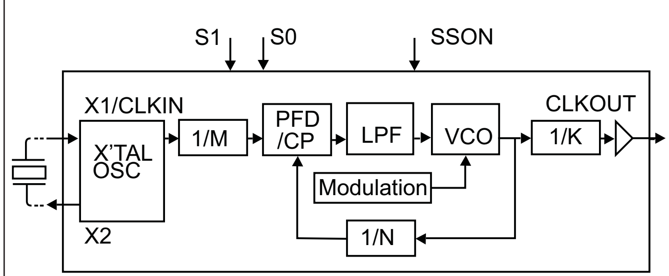
The chip is packaged in the 8-pin TSSOP. The reduced size of the package outlines can save precious board space and make layout easier.

PI6C3622 is one of the clock products provided by Pericom. If your application needs a clock product with a different specification not currently provided, please contact us for further information or custom design.

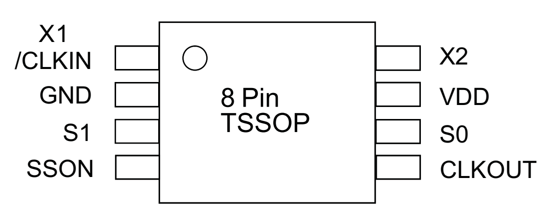
Benefits

- Reduction in EMI
- System cost saving
- Reduced system complexity
- Faster time to market

Block Diagram



Pin Configuration



Pin Description

Pin Name	Pin No.	IO Type	Description
X1/CLKIN	1	I	Crystal connection or reference frequency input. This pin has multiple functions. It can be connected either to an external crystal or an external reference clock.
GND	2	GND	Ground.
S1	3	I	Spreading Ratio Selection (0, 1); Default = 1; Internal 60K Ω pull–up included.
SSON	4	I	This pin enables/disables the Spread Spectrum feature; Default= 1 (enabled); Internal 60KΩ pull-up included
CLKOUT	5	O	Spread spectrum clock output.
S0	6	I	Frequecy Range Selection (0, 1); Default = 0; Internal 60K Ω pull-DOWN included
VDD	7	PWR	Power Supply
X2	8	O	Crystal connection. If using an external reference, this pin must be left unconnected.

Spreading Ratio Configuration

VDD = 2.5V ±5% / 3.3V ±10%, Ambient Temperature 25°C

Fin (MHz)	S1,S0 = (0,0) SSON=1	S1,S0 = (0,1) SSON=1	S1,S0 = (1,0) SSON=1	S1,S0 = (1,1) SSON=1	S1,S0 = 0/1 SSON=0	Modulation Rate (KHz)
	Center (%)	Center (%)	Center (%)	Center	No Spread	31.25~62.5
20	±0.30	±0.60	±0.80	±1.20	0	F_{in} /640
24	±0.28	±0.55	±0.75	±1.10	0	F_{in} /640
27	±0.25	±0.50	±0.70	±1.00	0	F_{in} /640
32	±0.25	±0.45	±0.65	±0.90	0	F_{in} /640
36	±0.23	±0.45	±0.60	±0.85	0	F_{in} /640
40	±0.20	±0.40	±0.55	±0.80	0	F_{in} /640

Timing Diagram

The following diagrams demonstrate the characteristics of the output signals when SSON Pin is switched off to disable the feature and switched on to enable to spread spectrum feature. The spreading ratio is set at ±1.0%, and the input frequency is 27MHz when the diagrams are generated.

Figure 1 and 2 demonstrate the responses of the output signal when then SSON pin is switched from high to low to disable the spread spectrum feature. When the feature is disabled, the output signal takes approximately 400us to re-lock from -1.0% to 0% frequency offset. When spread spectrum feature is disabled, the system must wait 1ms before the output signal can be used in order to maintain maximal system stability. This delay allows the output signal to settle properly to the required frequency.

Figure 1 and 3 demonstrates the responses of the output signal when then SSON pin is switched from low to high to enable the spread spectrum feature. The spreading ratio is twice of the expected value immediately after the switching. The spreading ratio then gradually settles to the expected value in approximately 400us. Figure 1 shows that it takes 400us for the spreading ratio to settle from ±2.0% to the expected ±1.0%. System designer should take this initial spreading ratio that is twice of the expected value into consideration when designing the system when designing the system in order to maintain maximal system stability.

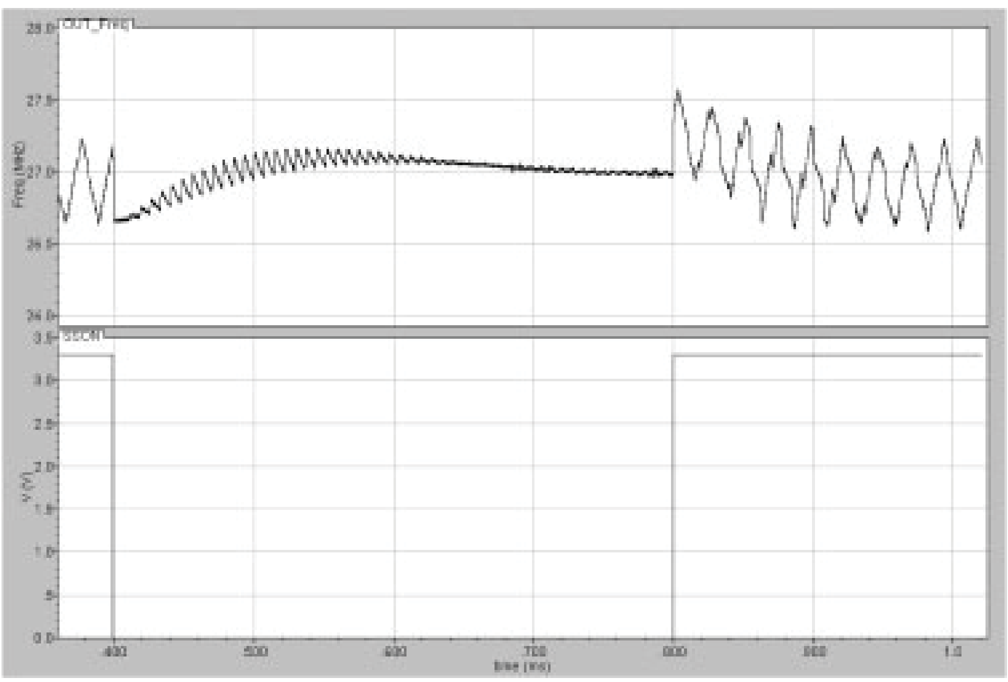


Figure 1. Frequency trend of the output signal when SSON is switched on and then off

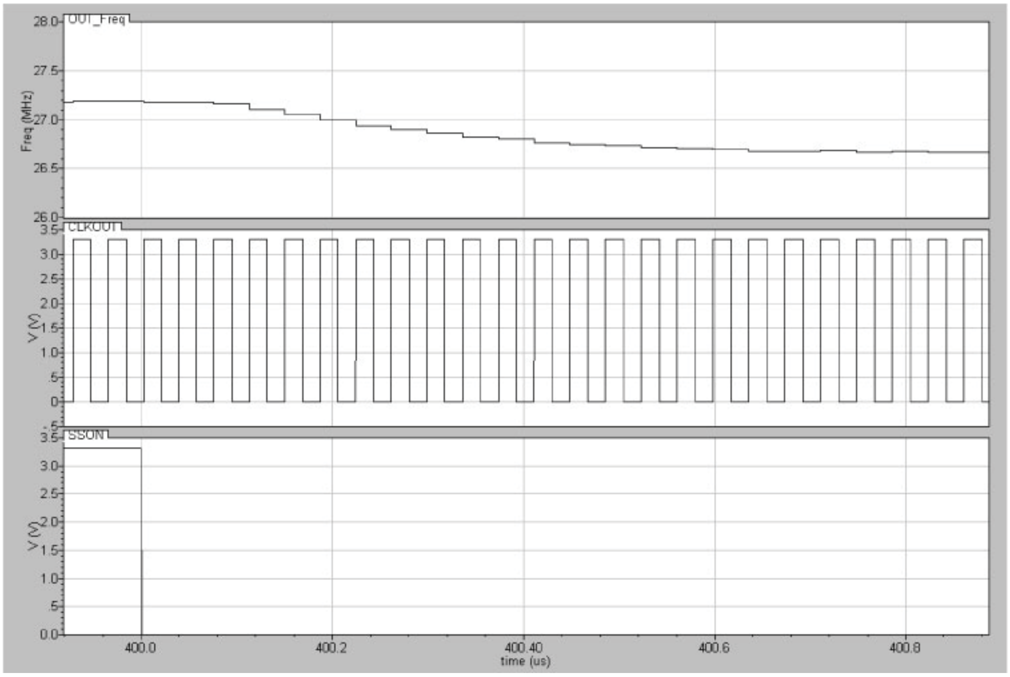


Figure 2. Frequency trend of the output signal when SSON is switched off

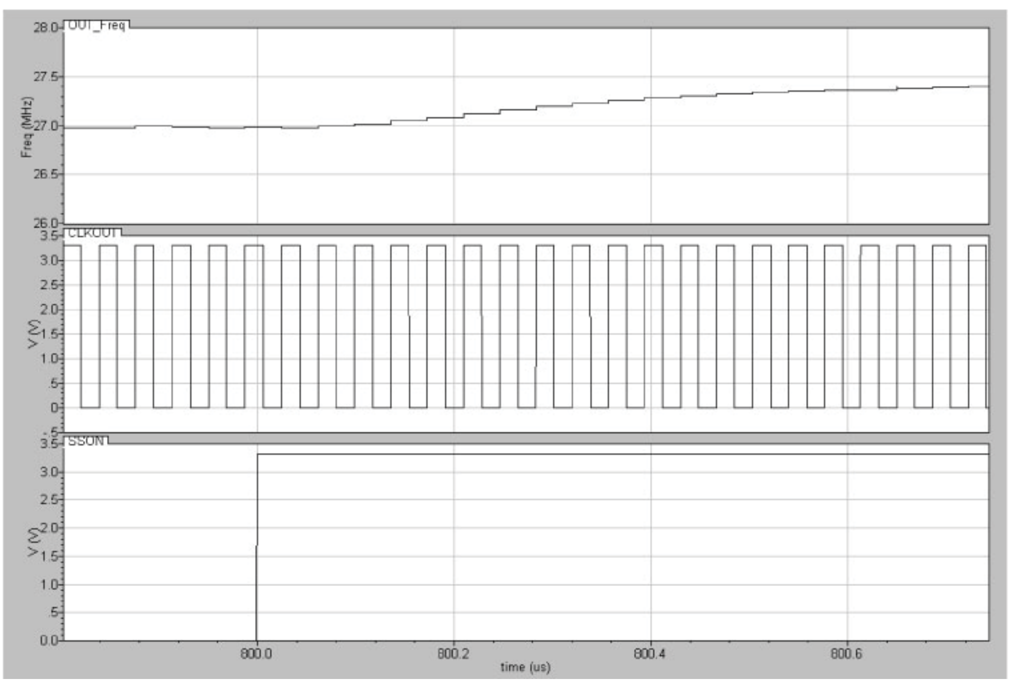


Figure 3. Frequency trend of the output signal when SSON is switched off

Electrical Specification

Maximum Ratings

Supply Voltage to Ground.. 5.5V
All Inputs and Outputs...–0.5V to VDD+0.5V
Storage Temperature ....–65 to +150°C
Junction Temperature...150°C
Soldering Temperature..260°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

DC Characteristics
VDD = 2.5V ±5%, Ambient Temperature 0 to +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{DD}	Operating voltage		2.375	2.5	2.625	V
V_{IH}	Input high voltage		2.0	–	–	V
V_{IL}	Input low voltage		–	–	0.8	V
V_{OH}	Output high voltage	I_{OH}=-8mA	1.8	–	–	V
V_{OL}	Output low voltage	I_{OL}= 8mA	–	–	0.6	V
I_{DD}	Supply current	27MHz input and no load	–	–	3.6	mA
Z_{OUT_DOWN}	Nominal output impedance	Down side buffer	–	50	–	Ω
Z_{OUT_UP}	Nominal output impedance	Up side buffer	–	50	–	Ω
C_{IN}	Input capacitance	X1 input pin	–	5	–	pF

AC Characteristics
VDD = 2.5V ±5%, Ambient Temperature 0 to +70°C , Fin=27MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
CLKIN	Input Frequency	20 MHz≤ Fin ≤40 MHz	20	27	40	MHz
CLKOUT	Output Frequency (1X)	20 MHz≤ Fin ≤40 MHz	20	27	40	MHz
S_{Ratio}	Spreading Ratio (SSON=1)	(S1,S0)=(0,0)		±0.25		%
		(S1,S0)=(0,1)		±0.50		
		(S1,S0)=(1,0)		±0.70		
		(S1,S0)=(1,1)		±1.00		
	Spreading Ratio (SSON=0)	(S1,S0)=(0/1, 0/1)		0		
t_{Rise}	Output rise time	Measured from 20% to 80% V_{DD}, 15pF load.	–	2.1	–	ns
t_{Fall}	Output fall time	Measured from 80% to 20% V_{DD}, 15pF load	–	1.9	–	ns
t_{J_Short}	Short term cycle to cycle jitter		–	200	300	ps
T_{SSON}	Spreading on/off settle time		–	600	–	µs
T_{DCIN}	Input duty cycle		40	50	60	%
T_{DCOUT}	Output duty cycle		45	50	55	%

DC Characteristics
V_{DD} = 3.3V ±10%, Ambient Temperature 0 to +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
V_{DD}	Operating voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage		2.0	–	–	V
V_{IL}	Input low voltage		–	–	0.8	V
V_{OH}	Output high voltage	I_{OH}=-8 mA	2.5	–	–	V
V_{OL}	Output low voltage	I_{OL} = 8mA	–	–	0.5	V
I_{DD}	Supply current	27MHz input and no load	–	–	5.3	mA
Z_{OUT_DOWN}	Nominal output impedance	Down side buffer	–	45	–	Ω
Z_{OUT_UP}	Nominal output impedance	Up side buffer	–	45	–	Ω
C_{IN}	Input capacitance	X1 input pins	–	5	–	pF

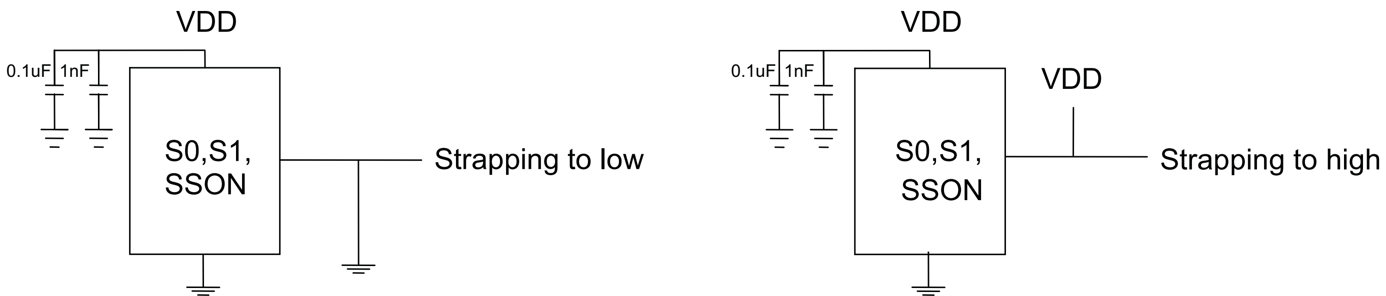
AC Characteristics
VDD = 3.3V ±10%, Ambient Temperature 0 to +70°C , Fin=27MHz

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
CLKIN	Input Frequency	20 MHz≤ Fin ≤40 MHz	20	27	40	MHz
CLKOUT	Output Frequency (1X)	20 MHz≤ Fin ≤40 MHz	20	27	40	MHz
S_{Ratio}	Spreading Ratio (SSON=1)	(S1,S0)=(0,0)		±0.25		%
		(S1,S0)=(0,1)		±0.50		
		(S1,S0)=(1,0)		±0.70		
		(S1,S0)=(1,1)		±1.00		
	Spreading Ratio (SSON=0)	(S1,S0)=(0/1, 0/1)		0		%
t_{Rise}	Output rise time	Measured from 20% to 80% V_{DD}, 15pF load.	–	1.7	–	ns
t_{Fall}	Output fall time	Measured from 80% to 20% V_{DD}, 15pF load	–	1.7	–	ns
t_{J_Short}	Short term cycle to cycle jitter		–	180	250	ps
T_{SSON}	Spreading on/off settle time		–	600	–	µs
T_{DCIN}	Input duty cycle		40	50	60	%
T_{DCOUT}	Output duty cycle		45	50	55	%

Application Information

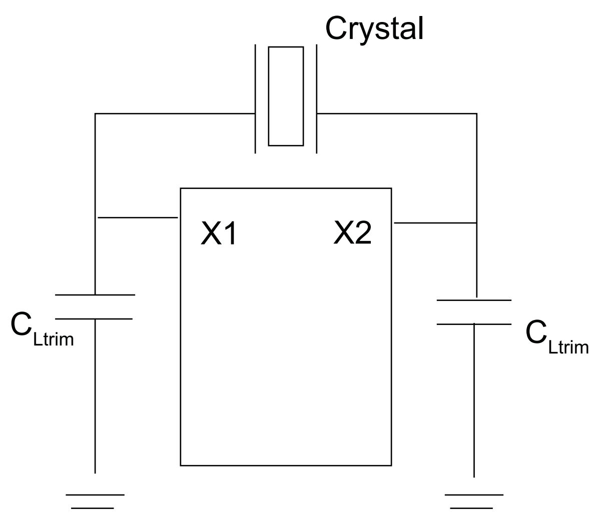
Decoupling Capacitor

Two decoupling capacitors of 0.1uF and 1nF must be connected in parallel between VDD and GND. To optimize device performance and to lower output noise, the coupling capacitors should be placed on the component side of the board as close to these pins as possible. There should be no vias placed between the decoupling capacitors and VDD pin. The PCB trace to VDD pin should be as short as possible, and no vias should be placed between VDD and the capacitors in the decoupling circuit.



Crystal Load Capacitor

If a crystal is used with the device, two external trim capacitors, CLtrim, are used to adjust the effective capacitance to match the required crystal load capacitance. The CLtrim value can be derived from formula CLtrim = 2*CL – (Cs + Ci). The typical CLtrim = 28pF when crystal load = 18pF, stray capacitance Cs = 3pF and XTAL pins capacitance = 5pF.

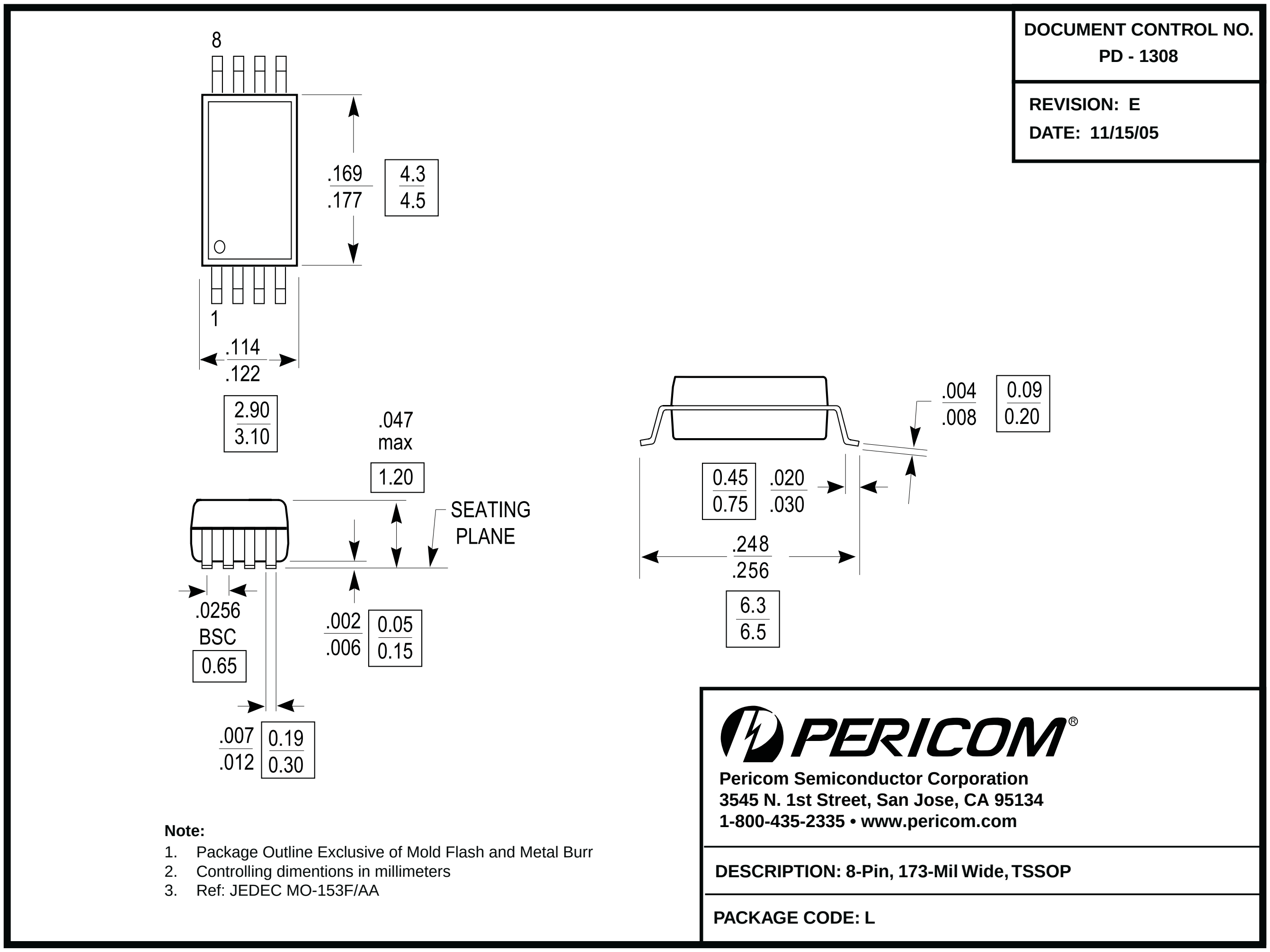


PCB Layout Recommendation

To optimize device performance, all components should be placed on the same side of the board and, therefore, no vias are used through other signal layers. The part should be kept away from other signal traces including ones just underneath the part or on layers adjacent to the ground plane layer used by the part. The PCB trace from the part to the ground via should be kept as short as possible.

Physical Dimensions

Packaging Mechanical: 8-pin, TSSOP



Ordering Information

Ordering Code	Package Code	Package Description
PI6C3622LE	L	Pb-Free & Green, 8-Pin TSSOP

Notes:

1. Thermal characteristics and package top marking information can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green Package
3. Adding an X suffix = Tape/Reel

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