

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

# TA8889AP

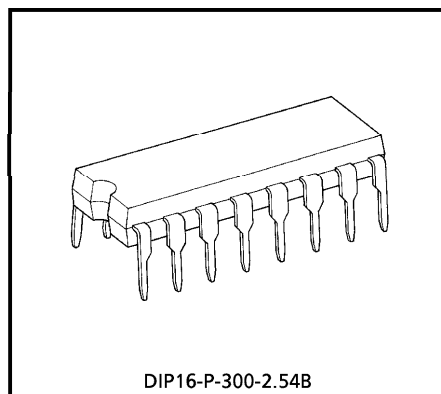
## RGB CUT OFF DRIVE CONTROL IC

The TA8889AP is 16pin DIP package IC which has RGB Cut off/Drive control circuit.

The feature of TA8889AP is controlled via via I<sup>2</sup>C bus.

### FEATURES

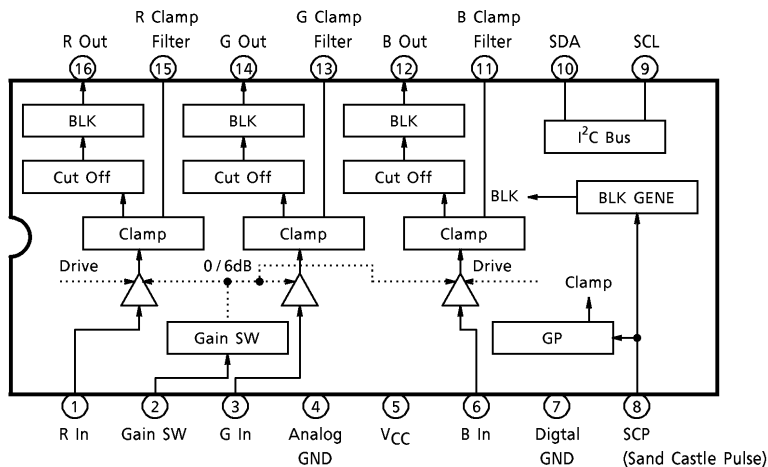
- 3 independents cut off control for 3 primary color.
- Independent drive control for blue and green color.
- 0dB / 6dB gain SW
- I<sup>2</sup>C bus interface circuit



DIP16-P-300-2.54B

Weight : 1.11g (Typ.)

### BLOCK DIAGRAM



961001EBA2

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TERMINAL FUNCTION

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
1 3 6	R In G In B In	These are primary color input terminals. The signal which pedestal DC level is 2V should be inputted.	
2	Gain SW	This is the switch terminal for gain 0dB / 6dB and blanking pulse. Please refer gain SW mode table for detail.	
4	Analog GND	This is the GND terminal for analog circuit.	—
5	VCC	This is common VCC terminal for analog and digital circuit. The coupling capacitor should be connected between this terminal and digital GND.	—
7	Digital GND	This is GND terminal for I <sup>2</sup> L circuit. The coupling capacitor should be connected between this terminal and digital GND.	—
8	S.C.P.	This is S.C.P. input terminal. The threshold level of clamp pulse is 6.5V and more (typ.), that of blanking pulse is 1.5V and less (typ.).	
9	SCL	This is SCL terminal for I <sup>2</sup> C bus. Because its is week for surge impulse, connect external devices for protection against surge if necessary.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
10	SDA	This is SDA terminal for I <sup>2</sup> C bus. Because its is week for surge impulse, connect external devices for protection against surge if necessary.	
15 13 11	R Clamp Filter G Clamp Filter B Clamp Filter	This is the clamp filter terminal for R /G /B signal which is the signal after cut off and drive circuit.	
16 14 12	R Out G Out B Out	This is the R /G /B signal output terminal. We recommend its connects L.P.F. for removing high frequency noise.	

**TERMINAL 2 (GAIN SW) OUTPUT MODE TABLE**

(V<sub>CC</sub> = 12V, Ta = ±3°C)

TERMINAL VOLTAGE	GAIN	BLANKING
V <sub>CC</sub> (9.7V~V <sub>CC</sub> )	6dB	Available
7.5V (6.7V~8.3V)		Not available
4.5V (3.7V~5.3V)	0dB	
GND (GND~2.3V)		

**I<sup>2</sup>C BUS CONTROL MAP**

- Slave address : 10011000 (98H)
- Sub address

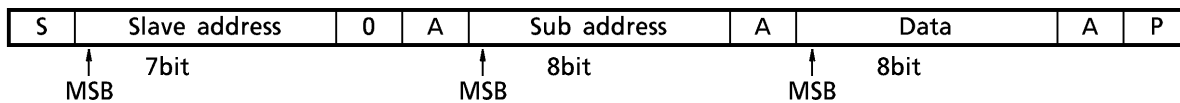
SUB ADDRESS		7	6	5	4	3	2	1	0	PRESET	
00	( I )	Red color cut off control (10bit)								LSB	00000000 (00H)
01	(II)	x	x	x	x	x	x	MSB ↑		00000000 (00H)	
02	( I )	Green color cut off control (10bit)								LSB	00000000 (00H)
03	(II)	x	x	x	x	x	x	MSB ↑		00000000 (00H)	
04	( I )	Blue color cut off control (10bit)								LSB	00000000 (00H)
05	(II)	x	x	x	x	x	x	MSB ↑		00000000 (00H)	
06	(III)	MSB	Red color drive control (8bit)						LSB	00000000 (00H)	
07	(III)	MSB	Blue color drive control (8bit)						LSB	00000000 (00H)	

(Note) x bit : don't care

**I<sup>2</sup>C BUS CONTROLLED FORMAT SUMMARY**

Bus controlled format of TA8889AP is based on I<sup>2</sup>C bus control format of Philips.

Data transfer format

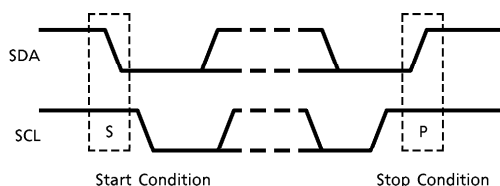


S : Start Condition

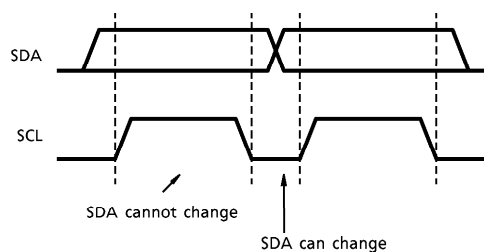
P : Stop Condition

A : Acknowledge

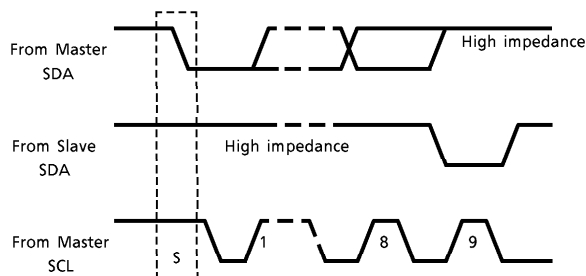
**(1) Start and stop condition**



**(2) Bit transfer**



**(3) Acknowledge**



**(4) Slave address**

A6	A5	A4	A3	A2	A1	A0	R / $\bar{W}$
1	0	0	1	1	0	0	0

Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

**MAXIMUM RATINGS** ( $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{CC}$	15	V
Power Dissipation	$P_D$ (Note 1)	1.4	W
Input Signal Voltage	$e_{in}$	7	$V_{p-p}$
Terminal Voltage	$V_{in}$ (Note 2)	$\text{GND} - 0.3 \sim V_{CC} + 0.3$	V
Operating Temperature	$T_{opr}$	$-20 \sim 65$	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-65 \sim 150$	$^\circ\text{C}$

(Note 1) When using the device at above  $T_a = 25^\circ\text{C}$ , decrease the power dissipation by 11.2mW for each increase of  $1^\circ\text{C}$ .

(Note 2) Rating of pin 9 and 10 is  $\text{GND} - 0.3\text{V} \sim 5.5\text{V}$ .

**RECOMMENDED SUPPLY VOLTAGE**

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
5	$V_{CC}$	10.8	12.0	13.2	V

**ELECTRICAL CHARACTERISTICS**

DC characteristics (Unless otherwise specified,  $V_{CC} = 12\text{V}$ ,  $T_a = 25 \pm 3^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Current	$I_{CC}$	—	Pin 1, 3, 6-DC 2V input Pin 8-S.C.P. input Pin 2-6dB MODE Sub address (I) = 00H (II) = 02H (III) = 80H	46	56	70	mA
Terminal Voltage	$V_{11}$	—		5.0	6.0	7.0	V
	$V_{12}$			2.8	3.0	3.2	
	$V_{13}$			5.0	6.0	7.0	
	$V_{14}$			2.8	3.0	3.2	
	$V_{15}$			5.0	6.0	7.0	
	$V_{16}$			2.8	3.0	3.2	

AC characteristics (Unless otherwise specified,  $V_{CC} = 12V$ ,  $T_a = 25 \pm 3^\circ C$ )

Drive circuit

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Frequency Characteristic	$f_c$	—	(Note 1)	10	20	30	MHz	
Cross-talk	$C_V$	—	(Note 2)	45	50	—	dB	
6dB Mode Gain	Max.	$G_{6MA}$	(Note 3)	SA (III) : FFH	9.0	10.0	11.5	dB
	Typ.	$G_{6TY}$		SA (III) : 80H	3.5	5.5	7.5	
	Min.	$G_{6MI}$		SA (III) : 00H	1.0	2.0	3.0	
0dB Mode Gain	Max.	$G_{0MA}$	(Note 4)	SA (III) : FFH	3.0	4.0	5.5	dB
	Typ.	$G_{0TY}$		SA (III) : 80H	1.5	-0.5	-2.5	
	Min.	$G_{0MI}$		SA (III) : 00H	-3.0	-4.0	-5.5	
Gain Control Range	Max.	$G_{VMA}$	(Max. Gain / Min. Gain) - (Typ. Gain) Both 0 / 6dB mode	3.0	5.0	6.0	dB	
	Min.	$G_{VMI}$		3.0	3.5	4.0		
Input Dynamic Range	Max. DC	$G_{IDA}$	(Note 5)	6.5	7.0	—	V	
	Min. DC	$G_{IDI}$		—	1.0	1.5		
Output Dynamic Range	Max. DC	$V_{ODA}$	(Note 6)	10.0	10.5	—	V	
	Min. DC	$V_{ODI}$		—	1.0	1.5		

Cut off circuit

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Min. Control Range	$V_{LSB}$	—	(Note 7)	—	3.0	5.0	mV	
DC Voltage Control Range	Max.	$V_{CVI}$	(Note 8)	(I) (II) : FF03H	4.25	4.5	—	V
	Min.	$V_{CVA}$		(I) (II) : 0000H	—	1.6	1.8	
	Range	$V_{CV}$		(Max) - (Min)	2.5	2.9	—	
Center Off-set	$V_{COF}$	—	(Note 9)	(I) (II) : 0002H	0.8	1.0	1.2	V
Max. Input DC Level	$V_{IMA}$	—	(Note 10)	(I) (II) : 0000H	—	4.5	5.0	V
Min. Input DC Level	$V_{IMI}$			(I) (II) : FF03H	0.3	0.5	—	
Max. Output DC Level	$V_{OMA}$			(I) (II) : FF03H	—	5.4	6.0	
Min. Output DC Level	$V_{OMI}$			(I) (II) : 0000H	1.2	1.5	—	
Non Linear Point Value	SA : 7F00	$V_{AC1}$	(Note 11)	—	—	3.0	mV	
	SA : FF00	$V_{AC2}$		—	—	3.0		
	SA : FF01	$V_{AC3}$		—	—	3.0		

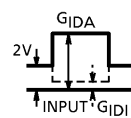
Threshold circuit

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
S.C.P. Threshold	GATE P	$V_{GP}$	—	6.2	6.5	6.8	V
	Hori. P	$V_{HP}$		1.2	1.5	1.8	
	Vert. P	$V_{VP}$		1.2	1.5	1.8	
Blanking Level	$V_{BLNK}$	$V_{BL}$	(Note 12)	0.20	0.25	0.30	V

**TEST CONDITION**

Drive circuit

NOTE No.	ITEM	TERMINAL 2 MODE	SUB ADDRESS & DATA			MEASUREMENT METHOD	
			(I)	(II)	(III)		
1	Frequency Characteristic	6dB (7.5V)	00H	02H	FFH	(1) Pin 1 (Pin 3, 6) : DC 4V. (2) Adjust the input voltage at Pin 15 (Pin 13, 11) to make Output voltage = 5.5V. (3) Pin 1 (Pin 3, 6) : 1MHz, 300mV <sub>p-p</sub> , DC 4V, sine wave. Measure the output level (vout). (4) Measure the input level to make Output level = (vout - 3dB)	
2	Cross-talk	0dB (GND)	↑	↑	80H	(1) The same as Note 1. (2) The same as Note 1. (3) Pin 1 (Pin 3, 6) : 5MHz, DC 4V, sine wave. (4) Measure the cross-talk.	
3	6dB Mode Gain	Max.	6dB (7.5V)	↑	↑	FFH	(1) Pin 8 : S.C.P. or Gate pulse. (2) Pin 1 (Pin 6) : signal = (pedestal level = 2V, amplitude 3V). (3) Measure the output level. Calculate the 20log (output level / input level).
		Typ.				80H	
		Min.				00H	
4	0dB Mode Gain	Max.	0dB (GND)	↑	↑	FFH	(1) The same as Note 3. (2) Pin 1 (Pin 6) : signal = (pedestal level = 2V, amplitude 1.5V). (3) The same as Note 3.
		Typ.				80H	
		Min.				00H	
5	Input Dynamic Range	Max. DC	↑	↑	↑	00H	(1) The same as Note 3. (2) Pin 1 (Pin 6) : signal = (under Fig.) (3) Make input signal larger to output signal saturation level. Measure the input level. →G DA (4) Make input signal smaller to output signal saturation level. Measure the input level. →G DI
		Min. DC					





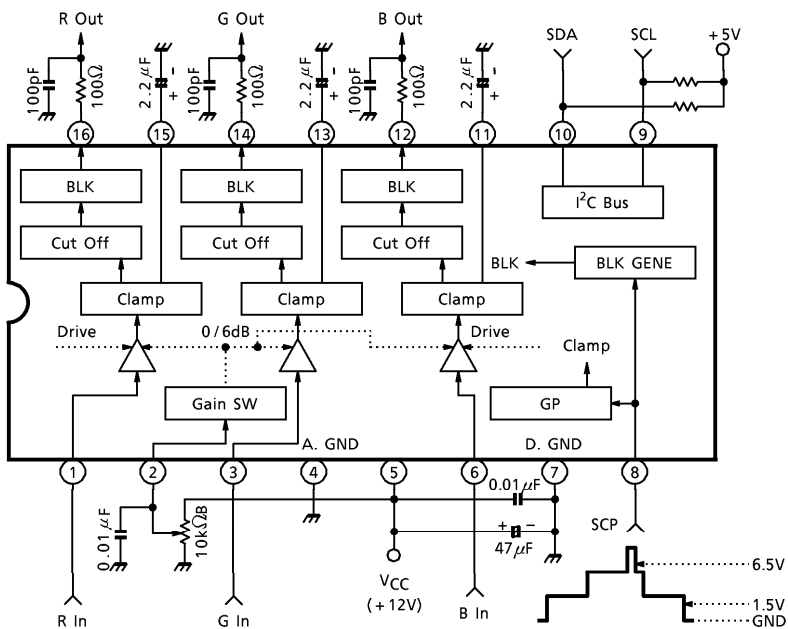
NOTE No.	ITEM		TERMINAL 2 MODE	SUB ADDRESS & DATA			MEASUREMENT METHOD
				(I)	(II)	(III)	
6	OUTPUT Dynamic Range	Max. DC	6dB (7.5V)	00H	02H	FFH	(1) Pin 8 : S.C.P. or Gate pulse. (2) Pin 1 (pin 6) : signal = (under Fig.) (3) Make input signal larger to output signal saturation level. Measure the output level. →G <sub>ODA</sub> (4) Make input signal smaller to output signal saturation level. Measure the output level. →G <sub>ODI</sub>
		Min. DC					

The diagram shows two waveforms. The first is labeled 'INPUT' and shows a square pulse with a peak-to-peak voltage of 2V. The second is labeled 'OUTPUT' and shows a square pulse with a peak-to-peak voltage of approximately 3V. The output pulse has two levels: a higher level labeled G<sub>ODA</sub> and a lower level labeled G<sub>ODI</sub>. Both waveforms are referenced to a common ground (GND).

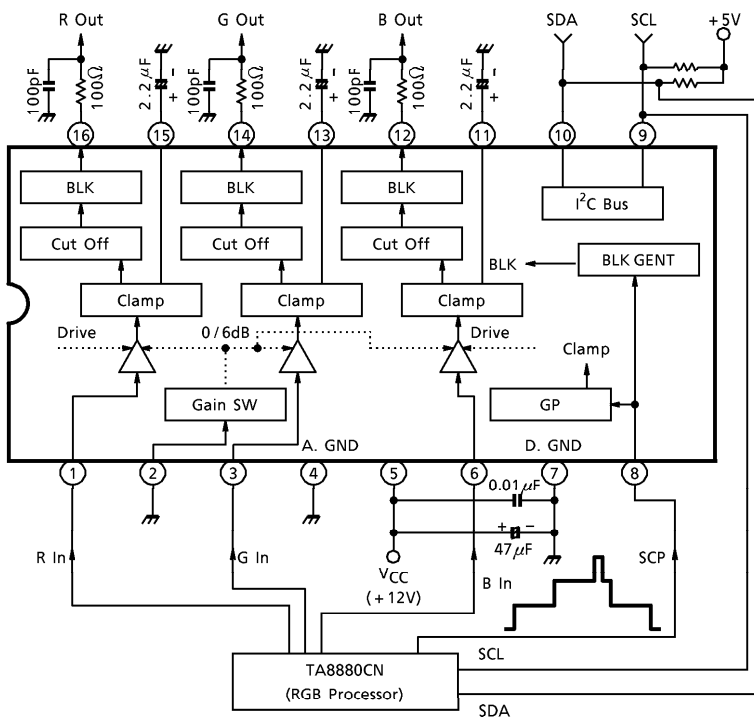
Cut off circuit

NOTE No.	ITEM		TERMINAL 2 MODE	SUB ADDRESS & DATA			MEASUREMENT METHOD
				(I)	(II)	(III)	
7	Min. Variable Range		0dB (GND)	00H ↓ 01H	00H	80H	(1) The same as Note 6. (2) Pin 1 (Pin 3, 6) : DC 2V. (3) Subaddress data (I) : 00H→01H. Measure the DC voltage gap of output DC level.
8	Control Range	Max.	↑	FFH	03H	↑	(1) The same as Note 6. (2) The same as Note 7. (3) SA (I) (II) : FF03H, 0000H ; Measure the output DC level of each DATA.
		Min.		00H	00H		
9	Center Off-set		↑	00H	02H	↑	(1) The same as Note 6. (2) The same as Note 7. (3) (Output DC level) – (Input DC level 2V)
10	Max. Input DC Level		↑	00H	00H	↑	(1) The same as Note 6. (2) SA (I) (II) : 0000H ; Increase input DC level to output DC saturation level, Measure the input DC level. →V <sub>I</sub> MA (3) Decrease input DC level to output DC saturation level, Measure the output DC level. →V <sub>O</sub> MI (4) SA (I) (II) : FF03H ; Decrease input DC level to output DC saturation level, Measure the input DC level. →V <sub>I</sub> MI (5) Increase input DC level to output DC saturation level, Measure the output DC level. →V <sub>O</sub> MA
	Min. Input DC Level		↑	FFH	03H	↑	
	Max. Output DC Level		↑	00H	03H	↑	
	Min. Output DC Level		↑	FFH	03H	↑	
11	Non Liner Point Value	SA : 7F00	↑	7F00H ↓ 8000H	↑	↑	(1) The same as Note 6. (2) Pin 1 (Pin 3, 6) : DC 2V. (3) SA (I) (II) : 7F00H→8000H, FF00H→0001H, FF01H→0002H ; Measure the DC voltage gap of each point.
		SA : FF00		7F00H ↓ 8000H			
		SA : FF01		7F00H ↓ 8000H			
12	Blanking Level		0dB (GND)	00H	02H	↑	(1) Pin 8 : S.C.P. or Gate pulse. (2) Pin 1 (Pin 3, 6) : DC 2V. (3) Measure The BLANKING LEVEL.

TEST CIRCUIT

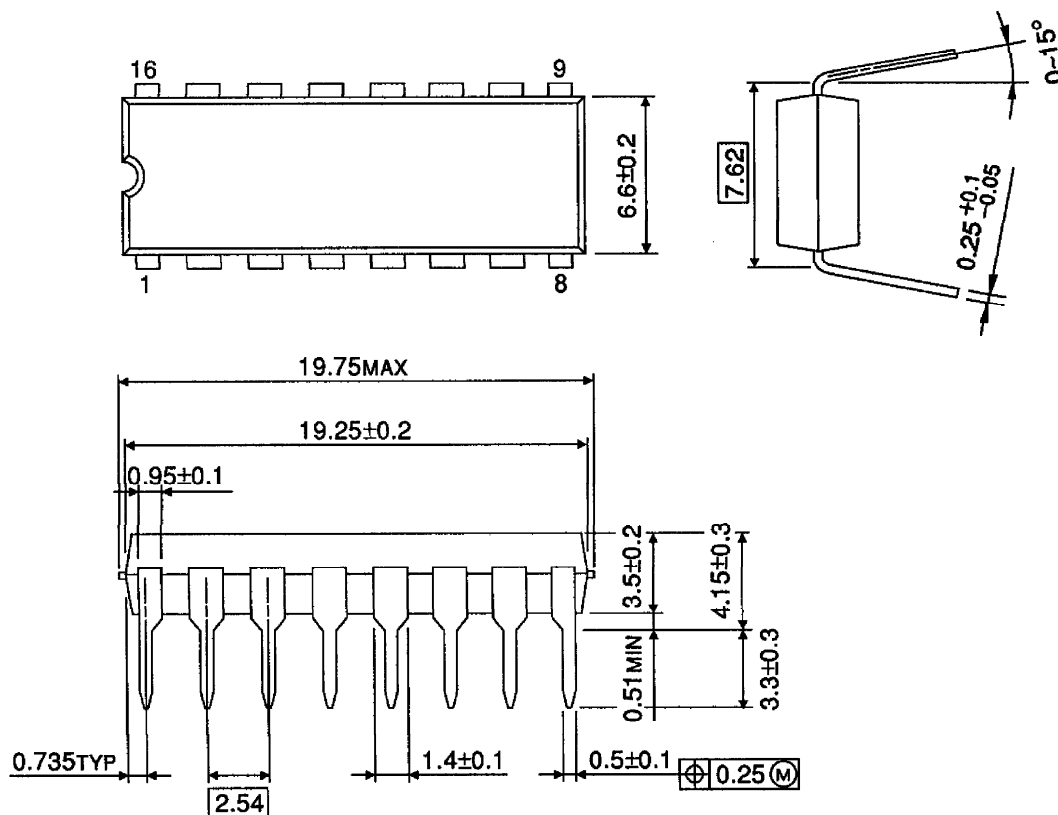


APPLICATION CIRCUIT



OUTLINE DRAWING  
DIP16-P-300-2.54B

Unit : mm



Weight : 1.11g (Typ.)