Shelly Associates Inc.

www.shellyinc.com

SPECIFICATION

CUSTOMER :

MODULE NO.: SCA0573EB-BD-FW-LW

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION: DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

VERSION	DATE	REVISED PAGE NO.	SUMMARY
B	2008.12.30	28	Correct con1.3

	MODLE NO :
RECORDS OF REVISION	DOC. FIRST ISSUE

VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2008.08.25		First issue
A	2008.11.11	28	Correct con3=up-side
B	2008.12.30	28	Correct con1.3

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1.Module Classification Information

SCA0573EB-BD-FW-LW
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ○9○10 ○11

① Brand：Shelly Associates Inc.
② Display Type：SCA →TFT Type
③ Display Size：5.7” TFT
④ Model serials no.
⑤ Backlight Type： LW→LED, White

⑥ LCD Polarize Type/ F→Transmissive,
Temperature range/ B→W. T, 6:00
View direction
⑦ B: TFT+FR+CONTROL BOARD

⑧ Solution: 320240

○9 D: Digital

○10 Version

○11 Special Code #:Fit in with ROHS directive regulations

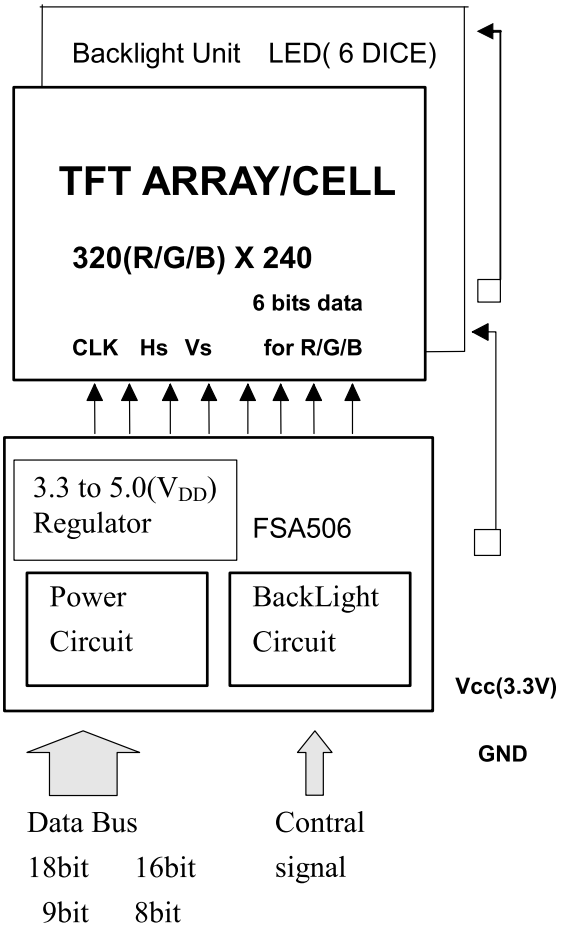
This product is composed of a TFT LCD panel, driver ICs, FPC, Control Board and a backlight unit. The following table described the features of SCA0573EB-BD-FW-LW.

Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	141.12x 101.55 x 5.8 (max)	mm
View area	126.0x 89.1	mm
Dot pitch	0.12 x 0.36	mm
Driving IC package	COG	
LCD type	TFT, Negative, Transmissive	
View direction	6 o'clock	
Backlight Type	LED,Normally White	
Controller IC	FSA506	

*Expose the IC number blaze (Luminosity over than 1 cd) when using the LCM may cause IC operating failure.

*Color tone slight changed by temperature and driving voltage.

2.Block Diagram



3.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VCC	-	3.0	3.3	3.6	V
Input High Volt.	V_{IH}	-	0.7 V_{CC}	-	V_{CC}	V
Input Low Volt.	V_{IL}	-	0	-	0.3Vcc	V
LCD Driving Supply Voltage	V_{GH} *1	Ta=25°C		15		V *3
	V_{GL}*2			-10		V
	VcomH		2.5		5.5	
	VcomL		-2.0		0	
Supply Current	I_{VDD}	V_{DD}=3.3V	-	5	8	mA

Notes:
*1) VGH is TFT Gate on operating Voltage.
*2) VGL is TFT Gate off operating Voltage, VGL signal must be fluctuates with same phase as Vcom when Storage on Gate structure.
*3) Vcom must be adjusted to optimize display quality_Crosstalk,Contrast Ratio and etc.

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	-	+70	°C
Storage Temperature	T_{ST}	-30	-	+80	°C
Power Supply Voltage	V_{GH}	-0.3	-	18	V
	V_{GL}	-15	-	0.3	V
	VCC	-0.3	-	6.0	V

5.Interface Pin Function

5-1 Pins Connection To Control Board

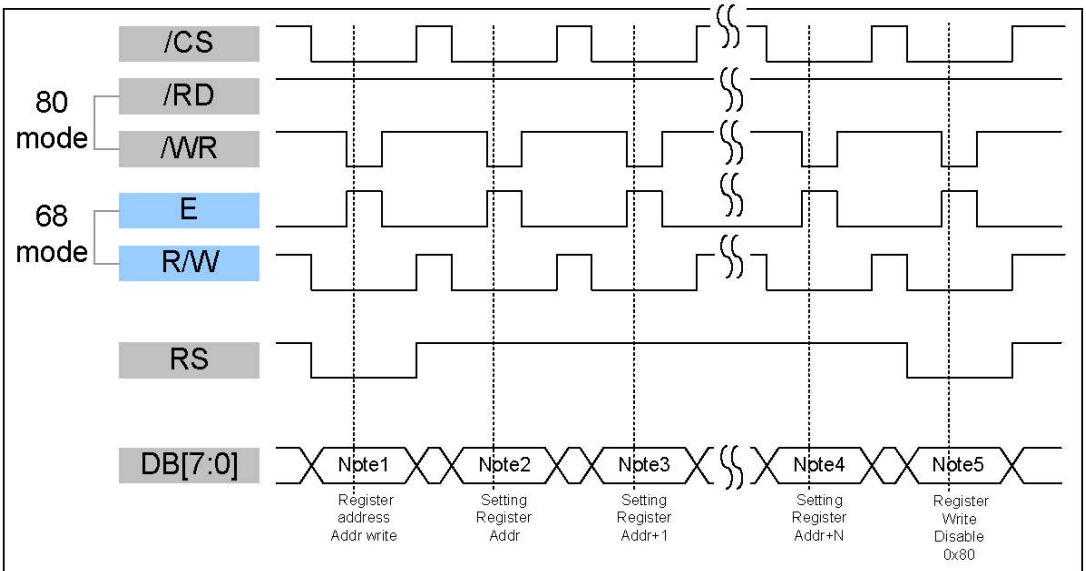
P/N	Symbol	8 B IT Function
1	GND	Ground
2	VCC	Power supply for Logic
3	NC	No connection
4	RS	
5	WR	8080 family MPU interface : Write signal
6	RD	8080 family MPU interface: Read signal
7	DB0	Data bus
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	CS	Chip select
16	RST	RESET
17	NC	No connection
18	RL	Scan direction
19	UD	Scan direction
20	NC	No connection

6. DC CHARATERISTICS

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Low level input voltage	V_{IL}	0	-	0.3 VCC	V	
Hight level input voltage	V_{IH}	0.7 VCC	-	VCC	V	

7. AC Characteristics

7.1 8Bit-80/68- Write to Command Register



Note1: DB[7:0] represent the the Register address Addr.

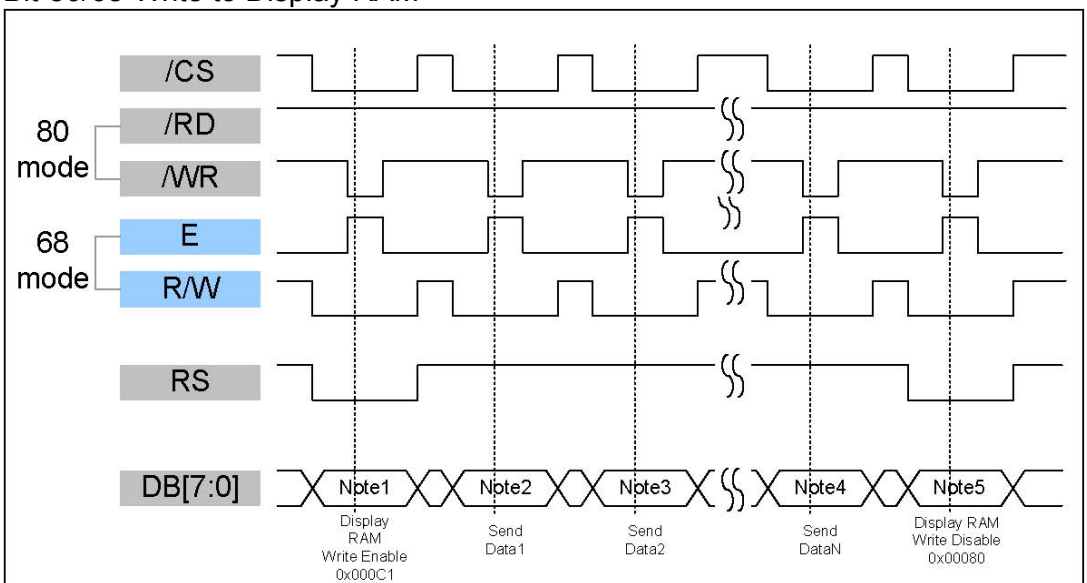
Note2: DB[7:0] represent the the setting value of the Addr.

Note3: DB[7:0] represent the the setting value of the Addr+1.

Note4: DB[7:0] represent the the setting value of the Addr+N.

Note5: DB[7:0] send 0x80 to Disable the Register write.

7.2 8Bit-80/68-Write to Display RAM



Note1: DB[7:0] send 0x000C1 to Enable the Display RAM write.

Note2: DB[7:0] represent the writing Data1 to Display RAM

Note3: DB[7:0] represent the writing Data2 to Display RAM

Note4: DB[7:0] represent the writing DataN to Display RAM

Note5: DB[7:0] send 0x00080 to Disable the Display RAM write.

8. Data transfer order Setting

8.1 8 bit interface 65K color (Pin 65K/262K =Low)
8.2 8 bit interface 262K color (Pin 65K/262K =High)

DB	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
2nd data	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R5	R4

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3
2nd data	X	X	X	X	X	X	X	G2	G1	G0	B5	B4	B3	B2	B1	B0

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3
2nd data	X	X	X	X	X	X	X	X	G2	G1	G0	B4	B3	B2	B1	B0

DB	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st data	X	X	X	X	X	X	X	X							R5	R4
2nd data	X	X	X	X	X	X	X	X	R3	R2	R1	R0	G5	G4	G3	G2
3rd data	X	X	X	X	X	X	X	X	G1	G0	B5	B4	B3	B2	B1	B0

9 Register Depiction

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0	0	MSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
1	0	LSB of X-axis start position								
Description	set the horizontals start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
2	1	MSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
3	3F	LSB of X-axis end position								
Description	set the horizontals end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
4	0	MSB of Y-axis start position								
Description	set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
5	0	LSB of Y-axis start position								
Description	Set the vertical start position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
6	0	MSB of Y-axis end position								
Description	set the vertical end position of display active region									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
7	EF	LSB of Y-axis end position								
Description	Set the vertical end position of display active region									

To simplify the address control of display RAM access, the window area address function allows for writing data only within a window area of display RAM specified by

registers REG[00]~REG[07] .

After writing data to the display RAM, the Address counter will be increased within setting window address-range which is specified by

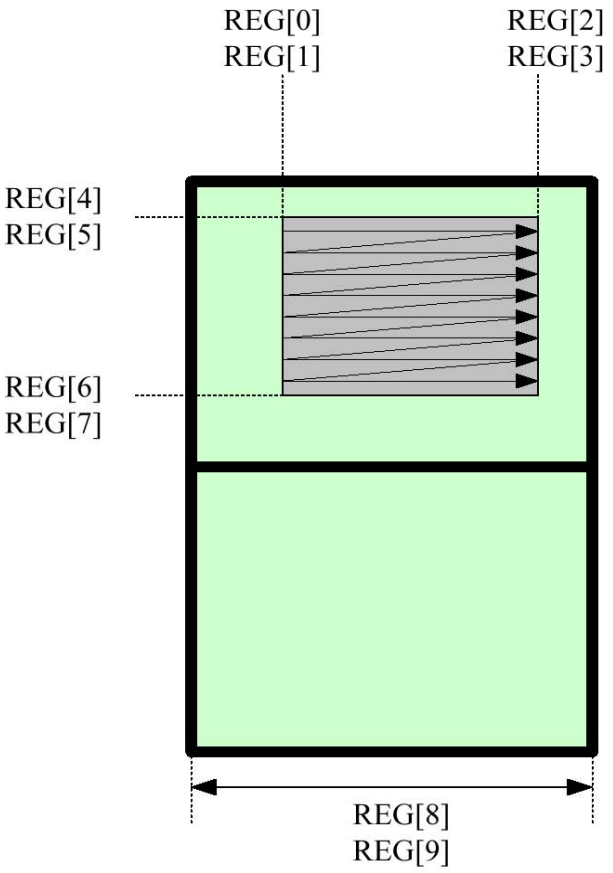
MIN X address (REG[0] & REG[1])

MAX X address (REG[2] & REG[3])

MIN Y address (REG[4] & REG[5])

MAX Y address (REG[6] & REG[7])

Therefore, data can be written consecutively without thinking the data address.



Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
8	1	X	X	X	X	X	X	_PanelXSize H_Byte[1:0]		
Description	Set the panel X size									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
9	40	_PanelXSize L_Byte[7:0]								

Description	Set the panel X size	

The register REG[08] and REG[09] is use to calculate the RAM address. If you want to use the TFT as Landscape mode (320x240), the REG[08] & RGE[09 must set to 320. If you want to use the TFT as Portrait mode (240x320), the REG[08] & RGE[09] must set to 240.

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0A	0	X	X	X	X	X	[17:16] bits of memory write start address			
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0B	0	[15:8] bits of memory write start address								
Description	Memory write start address									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0C	0	[7:0] bits of memory write start address								
Description	Memory write start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x10	0x0D	Bit_SWAP	OUT_TEST	BUS_SEL		Blanking	P/S_SEL	CLK_SEL		
Description	"0x10_Clk_sel[1:0]" : The TFT controller built-in 40Mhz PLL clock. These bits are for select the TFT panel dot clock frequency. 00 : 20Mhz 01: 10Mhz 02: 5 Mhz									
	"0x10_ps_sel[2]" : The TFT controller support parallel and serial RGB interface. These bits are for select the output timing. 0 : serial Panel 1: Parallel panel									
	"0x10_blanking_tmp[3]" 0 : OFF (blanking) 1: ON (normal operation)									
	"0x10_bus_sel[5:4]" : It only for serial Panel 00=R , 01=G , 10=B									
	"0x10_out_test[6]" : Self test 0 : normal operation 1: for test (don't use for normal operation) When set the bit to "1" , the Rout=(Reg 2a[6:0]) Gout=(Reg 2b[6:0]) Bout=(Reg 2c[6:0])									
	"0x10_bit_swap[7]" : 0-normal									
	The default setting is suitable for AM320240N1. Don't need to modify it.									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x11	0	X	X	EVEN			_ODD			
Description	" Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG **101: BGR** Others: reserved **Must Set to 0x05**									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x12	0					Hsync_stH_Byte[3:0]				

Description	For TFT output timing adjust: Hsync start position H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x13	0	Hsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync start position L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x14	0					Hsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync pulse width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x15	10	Hsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync pulse width L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x16	0					Hact_stH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse start position H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x17	38	Hact_stL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse start position L-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x18	1					Hact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: DE pulse width H-Byte									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x19	40	Hact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: DE pulse width L-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1A	1					HtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Hsync total clocks H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1B	B8	HtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Hsync total clocks H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1C	0					Vsync_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync start position H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1D	0	Vsync_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync start position L-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1E	0					Vsync_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vsync pulse width H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x1F	8	Vsync_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vsync pulse width L-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x20	0					Vact_stH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical DE pulse start position H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x21	12	Vact_stL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical DE pulse start position L-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x22	0					Vact_pwH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical Active width H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x23	F0	Vact_pwL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical Active width H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x24	1					VtotalH_Byte[3:0]				
Description	For TFT output timing adjust: Vertical total width H-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x25	9	VtotalL_Byte[7:0]								
Description	For TFT output timing adjust: Vertical total width L-Byte									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
26	0	X	X	X	X	X	[17:16] bits of memory read start address			
Description	Memory read start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
27	0	[15:8] bits of memory write start address								
Description	Memory read start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
28	0	[7:0] bits of memory write start address								
Description	Memory read start address									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
29	0	[7:1] Reversed								
Description	[0] Load output timing related setting (H sync., V sync. and DE) to take effect									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2A	0	X	TestPatternRout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Rout data equal to TestPatternRout[6:0]									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2B	0	X	TestPatternGout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Gout data equal to TestPatternGout[6:0]									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2C	0	X	TestPatternBout[6:0]							
Description	When " REG[0x10]_out_test[6]" : Self test =1 ; The Bout data equal to TestPatternBout[6:0]									

If you set the " REG[0x10]_out_test[6]" : Self test =1 , the TFT controller will skip the connect of the display RAM. The Output port will send the REG[2A] ,REG[2B],REG[2C] data.

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
0x2D	0	X	X	X	X	[3]	Rising/falling edge[2]	_rotate [1:0]		
Description	[3] Output pin X_DCON level control ; TFT Power ON/OFF control 0: TFT POWER circuit OFF 1: TFT POWER circuit ON									
	Rising/falling edge[2] : 0: The RGB out put data are on the Rising edge of the DCLK. 1: The RGB out put data are on the Falling edge of the DCLK.									
	_rotate [1:0]: 00 : rotate 0 degree 01 : rotate90 degree 10 : rotate 270 degree 11 : rotate 180 degree									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
30	0	X	X	X	X	X	_H byte H-Offset[3:0]			
Description	Set the Horizontal offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
31	0	_L byte H-Offset[7:0]								
Description	Set the Horizontal offset									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
32	0	X	X	X	X	X	_H byte V-Offset[3:0]			
Description	Set the Vertical offset									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
33	0	_L byte V-Offset[7:0]								
Description	Set the Vertical offset									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
34	0	[7:4] Reserved					_H byte H-def[3:0]			
Description	[3:0] MSB of image horizontal physical resolution in memory									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
35	40	_L byte H-def[7:0]								
Description	[7:0] LSB of image horizontal physical resolution in memory									

Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
36	1	[7:4] Reserved					_H byte V-def[3:0]			
Description	[3:0] MSB of image vertical physical resolution in memory									
Register Address (Hex)	Default (Hex)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Remark
37	E0	_L byte V-def[7:0]								
Description	[7:0] LSB of image vertical physical resolution in memory									

The total RAM size is 640x240x18bit. The user can arrange the Horizontal ram size by REG[34],REG[35] and the Vertical ram size by REG[36],REG[37].
EX: 320x480x18bit REG[34]=0x01 , REG[35]=0x40 , REG[36]=0x01 , REG[37]=0xE0
EX: 640x240x18bit. REG[34]=0x02 , REG[35]=0x80 , REG[36]=0x00 , REG[37]=0xF0

10. Reference Initial code :

```
void Initial_FSA506 (void)
{
    Command_Write(0x40,0x12);
    Command_Write(0x41,0x01);
    Command_Write(0x42,0x01);
    Command_Write(0x00,0x00);
    Command_Write(0x01,0x00);
    Command_Write(0x02,0x01);
    Command_Write(0x03,0x3F);
    Command_Write(0x04,0x00);
    Command_Write(0x05,0x00);
    Command_Write(0x06,0x00);
    Command_Write(0x07,0xEF);
    Command_Write(0x08,0x01);
    Command_Write(0x09,0x40);
    Command_Write(0x0A,0x00);
    Command_Write(0x0B,0x00);
    Command_Write(0x0C,0x00);
    Command_Write(0x10,0x0D);
    Command_Write(0x11,0x05);
    Command_Write(0x12,0x00);
    Command_Write(0x13,0x00);
    Command_Write(0x14,0x00);
    Command_Write(0x15,0x10);
    Command_Write(0x16,0x00);
    Command_Write(0x17,0x44);
    Command_Write(0x18,0x01);
    Command_Write(0x19,0x40);
    Command_Write(0x1A,0x01);
    Command_Write(0x1B,0xB8);
    Command_Write(0x1C,0x00);
    Command_Write(0x1D,0x00);
    Command_Write(0x1E,0x00);
    Command_Write(0x1F,0x08);
    Command_Write(0x20,0x00);
    Command_Write(0x21,0x13);
    Command_Write(0x22,0x00);
    Command_Write(0x23,0xF0);
    Command_Write(0x24,0x01);
    Command_Write(0x25,0x09);
    Command_Write(0x26,0x00);
    Command_Write(0x27,0x00);
    Command_Write(0x28,0x00);
    Command_Write(0x29,0x01);
    Command_Write(0x2D,0x08);
    Command_Write(0x30,0x00);
    Command_Write(0x31,0x00);
    Command_Write(0x32,0x00);
    Command_Write(0x33,0x00);
    Command_Write(0x34,0x01);
    Command_Write(0x35,0x40);
    Command_Write(0x36,0x00);
    Command_Write(0x37,0xF0);
}
//;*****************************************************************************
//;sed1330 funtion
Write_Reg(unsigned char command)
{
   R_D = 1; RS = 0; CS1 = 0; W_R  = 0;
   Data_BUS = command;
   W_R  = 1; RS = 1; CS1 = 1;
}
//;*****************************************************************************
Writ_Data(unsigned char data1)
{
```

```
    R_D = 1; RS = 1; CS1 = 0; W_R  = 0;
      Data_BUS = data1;
    W_R = 1; RS = 1; CS1 = 1;
}
//=====================================================
Command_Write(unsigned char REG,unsigned char VALUE)
{
Write_Reg(REG);
Writ_Data(VALUE);
}
```

11. OPTICAL CHARATERISTIC

Ta=25±2℃, ILED=20mA

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time		Tr	θ =0° 、Φ=0°	-	10		ms	Note 3,5
		Tf		-	15		ms	
Contrast ratio		CR	At optimized viewing angle	300	400	-	-	Note 4,5
Color Chromaticity	White	Wx	θ =0° 、Φ=0	(0.26)	(0.31)	(0.36)		Note 2,6,7
		Wy		(0.28)	(0.33)	(0.38)		
	Red	Rx	θ =0° 、Φ=0					
		Ry						
	Green	Gx	θ =0° 、Φ=0					
		Gy						
	Blue	Bx	θ =0° 、Φ=0					
		By						
Viewing angle	Hor.	ΘR	CR≧10	(50)	(60)		Deg.	Note 1
		ΘL		(50)	(60)			
	Ver.	ΦT		(40)	(50)			
		ΦB		(45)	(55)			
Brightness		-	-	200	250	-	cd/m^2	Center of display

Ta=25±2℃, I_L=20mA

Note 1: Definition of viewing angle range

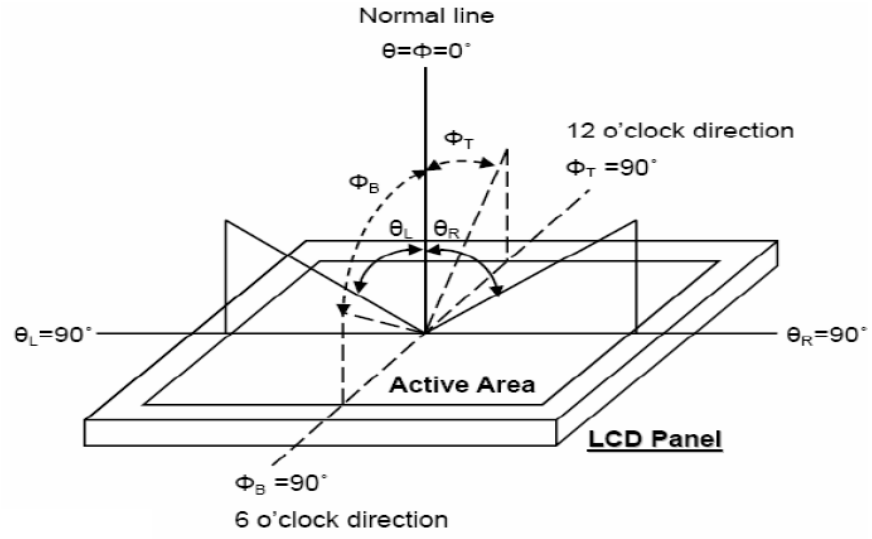


Fig. 8-1 Definition of viewing angle

Note 2: Test equipment setup:
After stabilizing and leaving the panel alone at a driven temperature for 10 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-7 luminance meter 1.0° field of view at a distance of 50cm and normal direction.

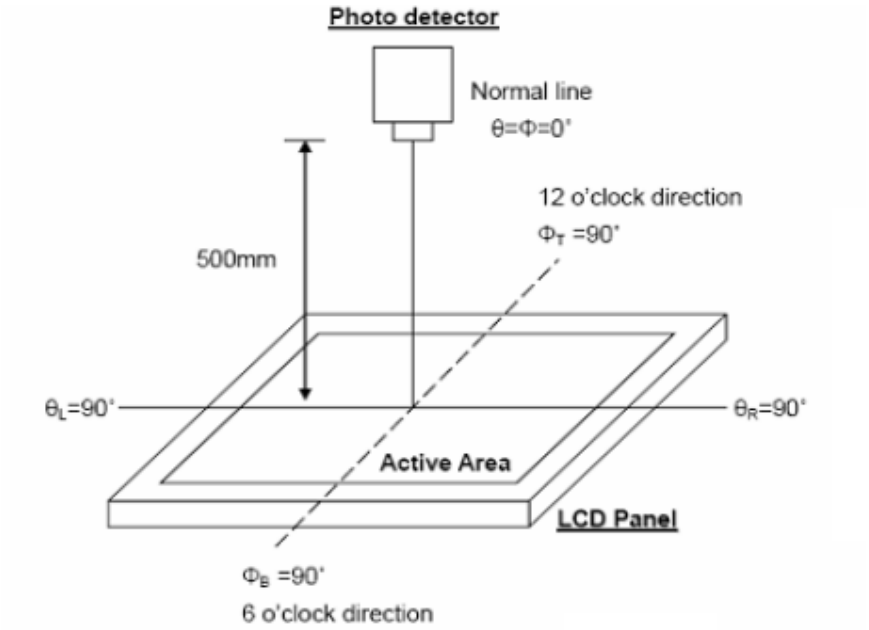


Fig. 8-2 Optical measurement system setup

Note 3: Definition of Response time:
The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time, Tr, is the time between photo detector output intensity changed from 90%to 10%. And fall time, Tf, is the time between photo detector output intensity changed from10%to 90%.

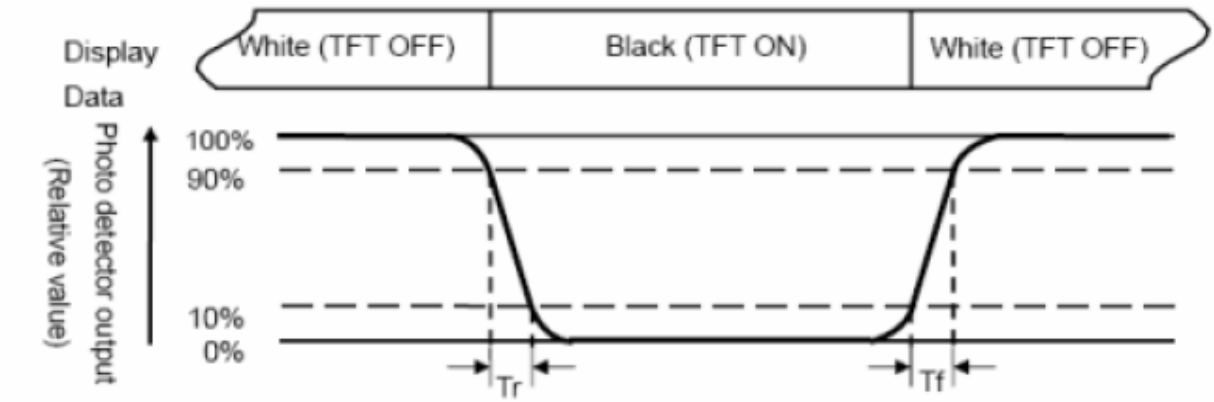


Fig. 3-3 Definition of response time

Note 4: Definition of contrast ratio:
The contrast ratio is defined as the following expression.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: White Vi = Vi50 ± 1.5V
Black Vi = Vi50 ± 2.0V
"±" means that the analog input signal swings in phase with VCOM signal.
"±" means that the analog input signal swings out of phase with VCOM signal.

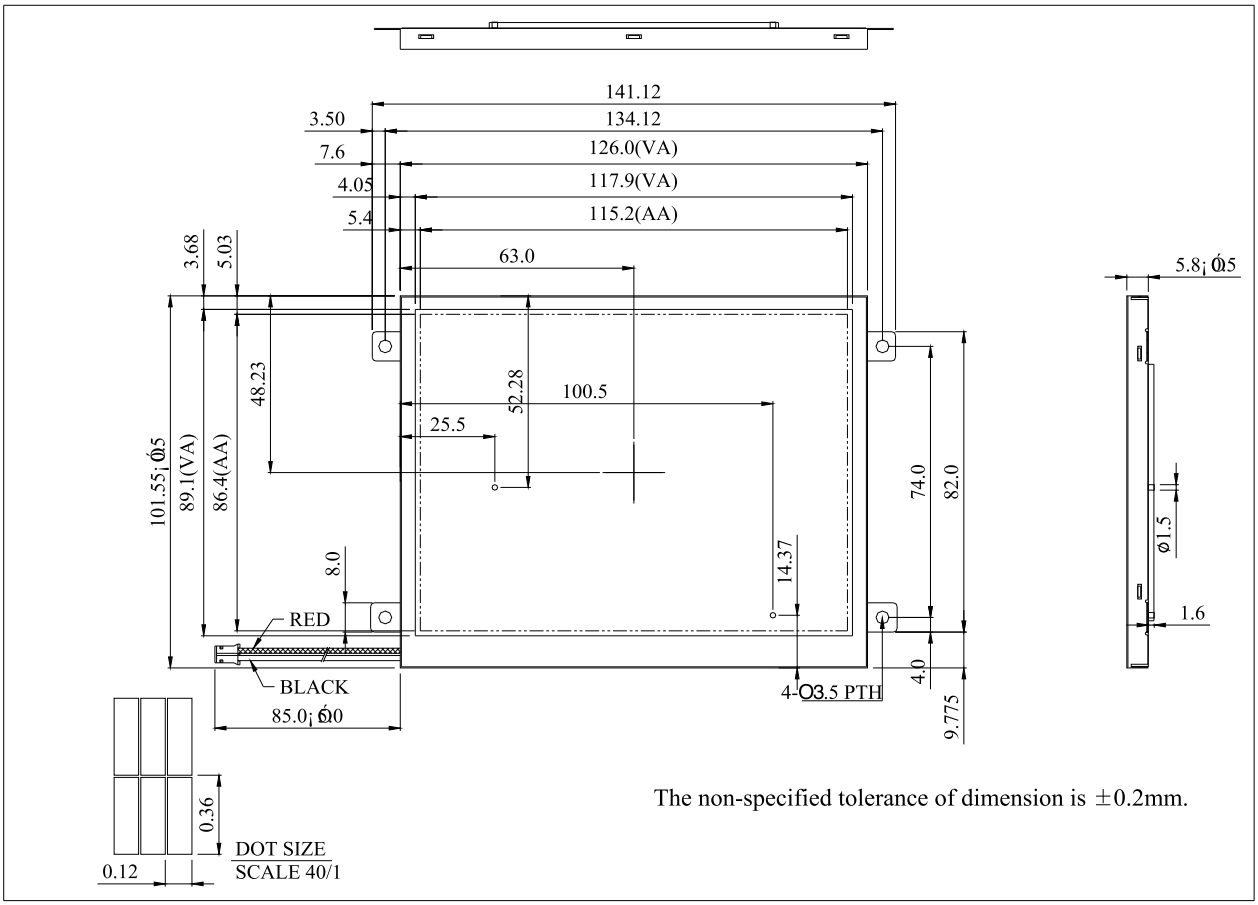
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

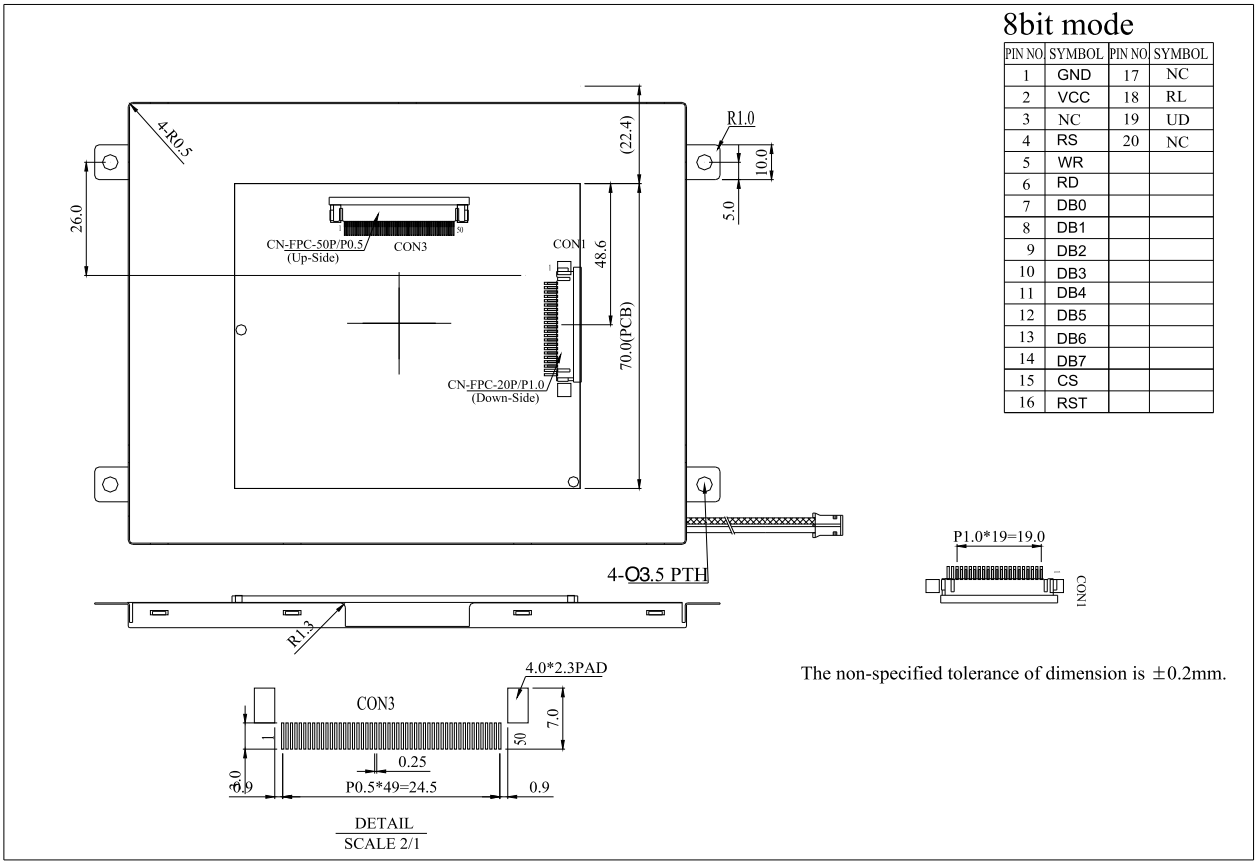
Note 6: Definition of color chromaticity (CIE 1931)
Color coordinates measured at the center point of LCD

Note 7: Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

$$\text{Note 8 : Uniformity (U)} = \frac{\text{Brightness (min)}}{\text{Brightness (max)}} \times 100\%$$

12.Contour Drawing

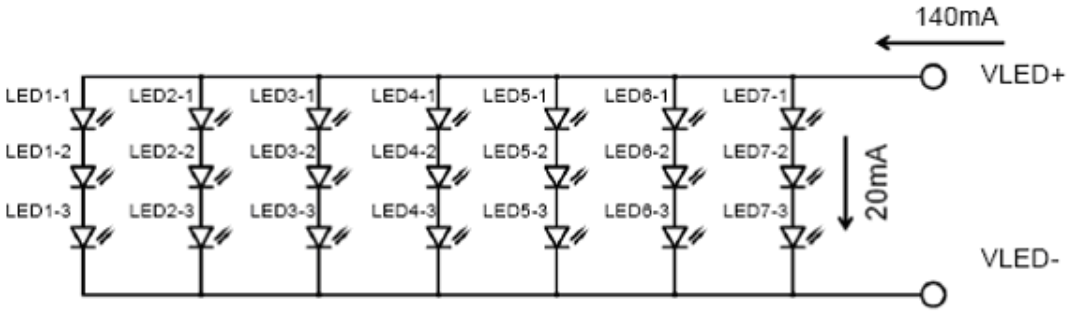




13. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_{LED}	----	140	210	mA	Note1
LED voltage	V_{LED}	9.0	----	10.5	V	
LED life Time	-	(10000)	----	----	-	Note 2,3
Luminous Intensity	IV	210.2	262.8	----	CD/M^2	Note 4

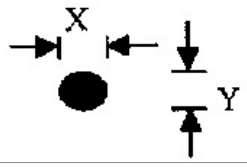
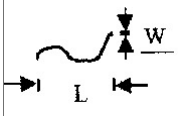
Note 1: There are 7 Groups LED shown as below, =9.9 V(Min)



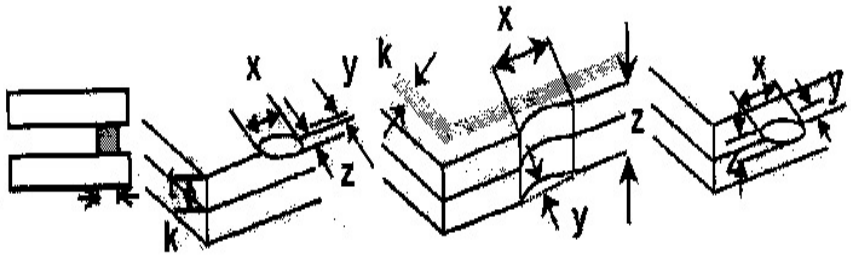
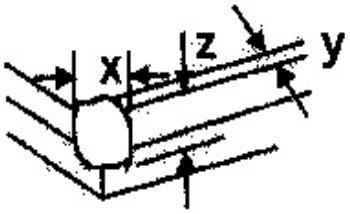
Note 2 : Ta = 25℃ ,
Note 3 : Brightess to be decreased to 50% of the initial value.

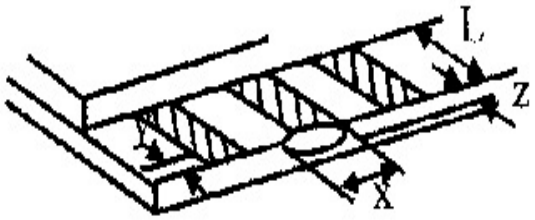
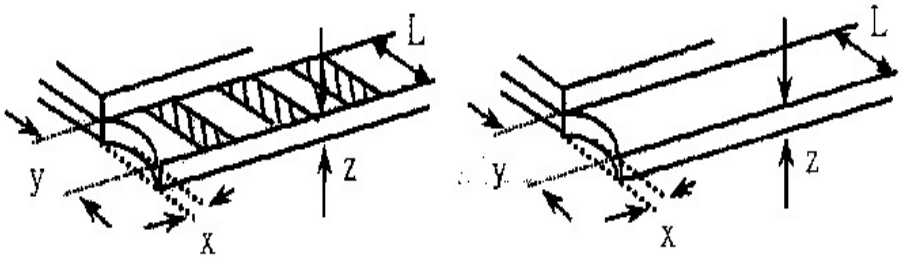
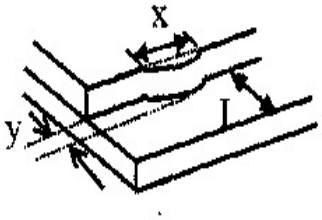
Note 4: The luminous is measured through LCD panel.

14. Inspection specification

NO	Item	Criterion	AQL
1	Electrical Testing	.1 Missing vertical, horizontal segment, segment contrast defect. .2 Missing character , dot or icon. .3 Display malfunction. .4 No function or no display. .5 Current consumption exceeds product specifications. .6 LCD viewing angle defect. .7 Mixed product types. .8 Contrast defect.	0.65
2	Black or white spots on LCD (display only)	2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present. 2.2 Densely spaced: No more than two spots or lines within 3mm	2.5
3	LCD black spots, white spots, contamination (non-display)	3.1 Round type : As following drawing Φ=(x + y) / 2 SIZE Acceptable Q TY Φ≦0.10 Accept no dense 0.10 < Φ≦0.20 2 0.20 < Φ≦0.25 1 0.25 < Φ 0 	2.5
		3.2 Line type : (As following drawing) Length Width Acceptable Q TY --- W≦0.02 Accept no dense L≦3.0 0.02 < W≦0.03 2 L≦2.5 0.03 < W≦0.05 --- 0.05 < W As round type 	2.5

4	Polarizer bubbles	Size Φ Acceptable Q TY Φ≦0.20 Accept no dense 0.20 < Φ≦0.50 3 0.50 < Φ≦1.00 2 1.00 < Φ 0 Total Q TY 3 If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.	2.5

NO	Item	Criterion	AQL
5	Scratches	Follow NO.3 LCD black spots, white spots, contamination	
6	Chipped glass	Symbols Define: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length: 6.1 General glass chip : 6.1.1 Chip on panel surface and crack between panels:  z: Chip thickness y: Chip width x: Chip length Z≦1/2t Not over viewing area x≦1/8a 1/2t < z≦2t Not exceed 1/3k x≦1/8a ⊙If there are 2 or more chips, x is total length of each chip. 6.1.2 Corner crack:  z: Chip thickness y: Chip width x: Chip length Z≦1/2t Not over viewing area x≦1/8a 1/2t < z≦2t Not exceed 1/3k x≦1/8a ⊙If there are 2 or more chips, x is the total length of each chip.	2.5

NO	Item	Criterion	AQL
6	Glass crack	Symbols : x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 6.2 Protrusion over terminal : 6.2.1 Chip on electrode pad :  y: Chip width x: Chip length z: Chip thickness y≦0.5mm x≦1/8a 0 < z ≦ t 6.2.2 Non-conductive portion:  y: Chip width x: Chip length z: Chip thickness y≦ L x≦1/8a 0 < z ≦ t ⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications. ⊙If the product will be heat sealed by the customer, the alignment mark not be damaged. 6.2.3 Substrate protuberance and internal crack. y: width x: length y≦1/3L x ≦ a  	2.5

NO	Item	Criterion	AQL
7	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
8	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
9	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 LCD pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

LCM Sample Estimate Feedback Sheet

Module Number：_____ **Page: 1**

1、Panel Specification：

1	Panel Type：	□ Pass	□ NG ,
2	View Direction：	□ Pass	□ NG ,
3	Numbers of Dots：	□ Pass	□ NG ,
4	View Area：	□ Pass	□ NG ,
5	Active Area：	□ Pass	□ NG ,
6	Operating Temperature：	□ Pass	□ NG ,
7	Storage Temperature：	□ Pass	□ NG ,
8	Others：		

2、Mechanical Specification：

1	PCB Size：	□ Pass	□ NG ,
2	Frame Size：	□ Pass	□ NG ,
3	Material of Frame：	□ Pass	□ NG ,
4	Connector Position：	□ Pass	□ NG ,
5	Fix Hole Position：	□ Pass	□ NG ,
6	Backlight Position：	□ Pass	□ NG ,
7	Thickness of PCB：	□ Pass	□ NG ,
8	Height of Frame to PCB：	□ Pass	□ NG ,
9	Height of Module：	□ Pass	□ NG ,
10	Others：	□ Pass	□ NG ,

3、Relative Hole Size：

1	Pitch of Connector：	□ Pass	□ NG ,
2	Hole size of Connector：	□ Pass	□ NG ,
3	Mounting Hole size：	□ Pass	□ NG ,
4	Mounting Hole Type：	□ Pass	□ NG ,
5	Others：	□ Pass	□ NG ,

4、Backlight Specification：

1	B/L Type：	□ Pass	□ NG ,
2	B/L Color：	□ Pass	□ NG ,
3	B/L Driving Voltage (Reference for LED Type)：	□ Pass	□ NG ,
4	B/L Driving Current：	□ Pass	□ NG ,
5	Brightness of B/L：	□ Pass	□ NG ,
6	B/L Solder Method：	□ Pass	□ NG ,
7	Others：	□ Pass	□ NG ,

> > Go to page 2 < <

5、Electronic Characteristics of Module：

1	Input Voltage：	□ Pass	□ NG ,
2	Supply Current：	□ Pass	□ NG ,
3	Driving Voltage for LCD：	□ Pass	□ NG ,
4	Contrast for LCD：	□ Pass	□ NG ,
5	B/L Driving Method：	□ Pass	□ NG ,
6	Negative Voltage Output：	□ Pass	□ NG ,
7	Interface Function：	□ Pass	□ NG ,
8	LCD Uniformity：	□ Pass	□ NG ,
9	ESD test：	□ Pass	□ NG ,
10	Others：	□ Pass	□ NG ,

6、Summary：

Sales signature：_____

Customer Signature：_____ **Date**：___/___/___