Ordering Information		
Part Numbers	**Description**	**Device Vendor**
SG25672RDDR6H2BGIC	256Mx72 (2GB), DDR, 184-pin DIMM, Registered, ECC, 128Mx4 Based, PC2700, DDR333B, 30.48mm, 18Ω DQ termination, Green Module (RoHS Compliant).	Qimonda, Rev. C HYB25D512400CF-5
SG25672RDDR6H2BGSC	256Mx72 (2GB), DDR, 184-pin DIMM, Registered, ECC, 128Mx4 Based, PC2700, DDR333B, 30.48mm, 18Ω DQ termination, Green Module (RoHS Compliant).	Samsung, Rev. C K4H510438C-ZCB3

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Revision History

- **July 5, 2007**
  Changed datasheet part number from SG25672RDDR6H2BGSC to SG25672RDDR6H2BGUU because of the addition of a new device vendor.
  Added SG25672RDDR6H2BGIC to the Ordering Information on page 1.

- **December 27, 2004**
  Datasheet released.

2GByte (256Mx72) DDR SDRAM Module - 128Mx4 Based 184-pin DIMM, Registered, ECC

Features

- Standard : JEDEC
- Configuration : ECC
- Cycle Time : 6.0ns
- CAS# Latency : 2.0, 2.5
- Burst Length : 2, 4, 8
- Burst Type : Sequential/Interleave
- No. of Internal Banks per SDRAM : 4
- Operating Voltage : 2.5V
- Refresh : 8K/64ms
- Device Physicals : FBGA
- Lead Finish : Gold
- Length x Height : 133.35mm x 30.48mm
- No. of sides : Double-sided
- Mating Connector (Examples)
  Vertical : AMP - 390241-1

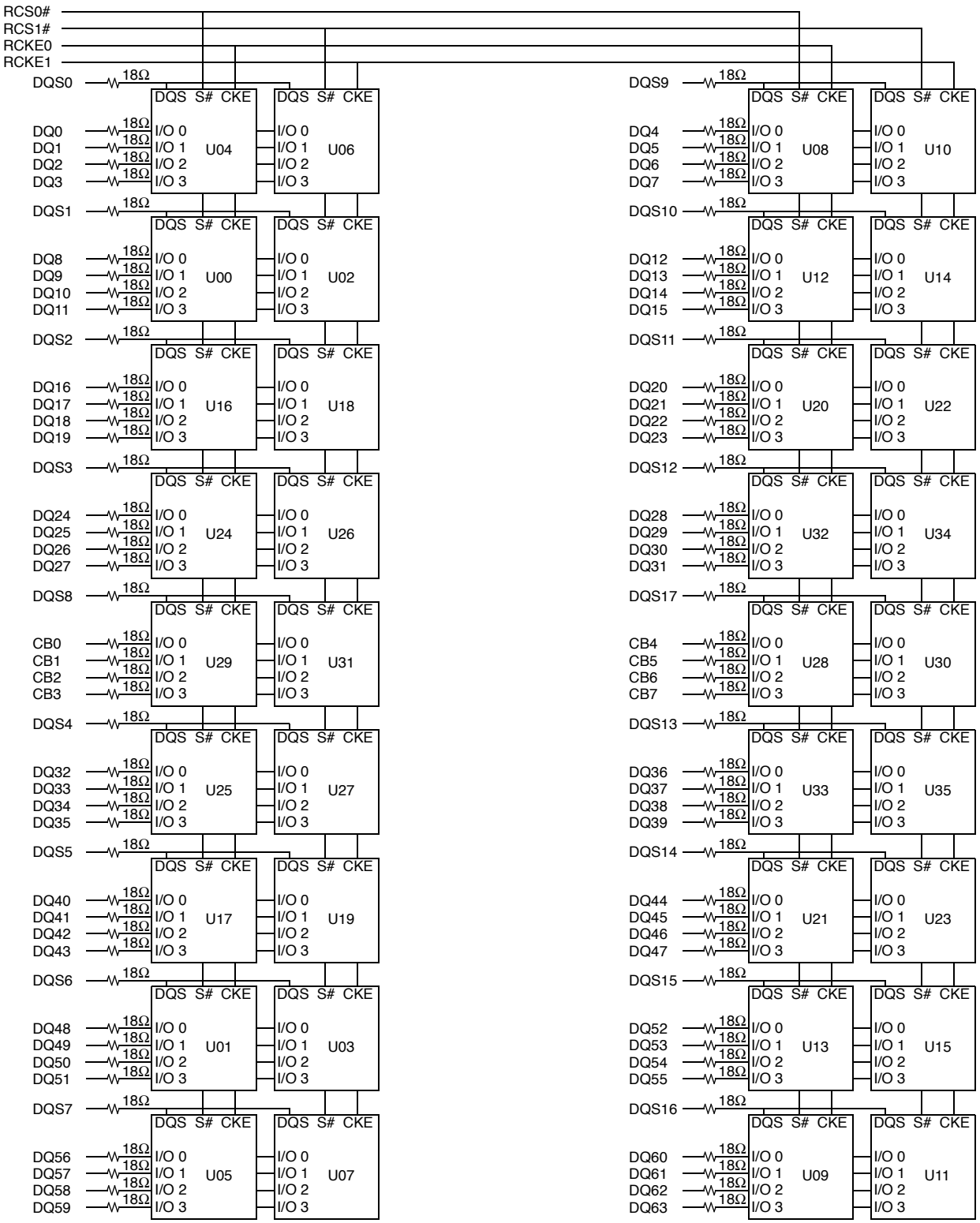
DDR 184-pin DIMM Pin List

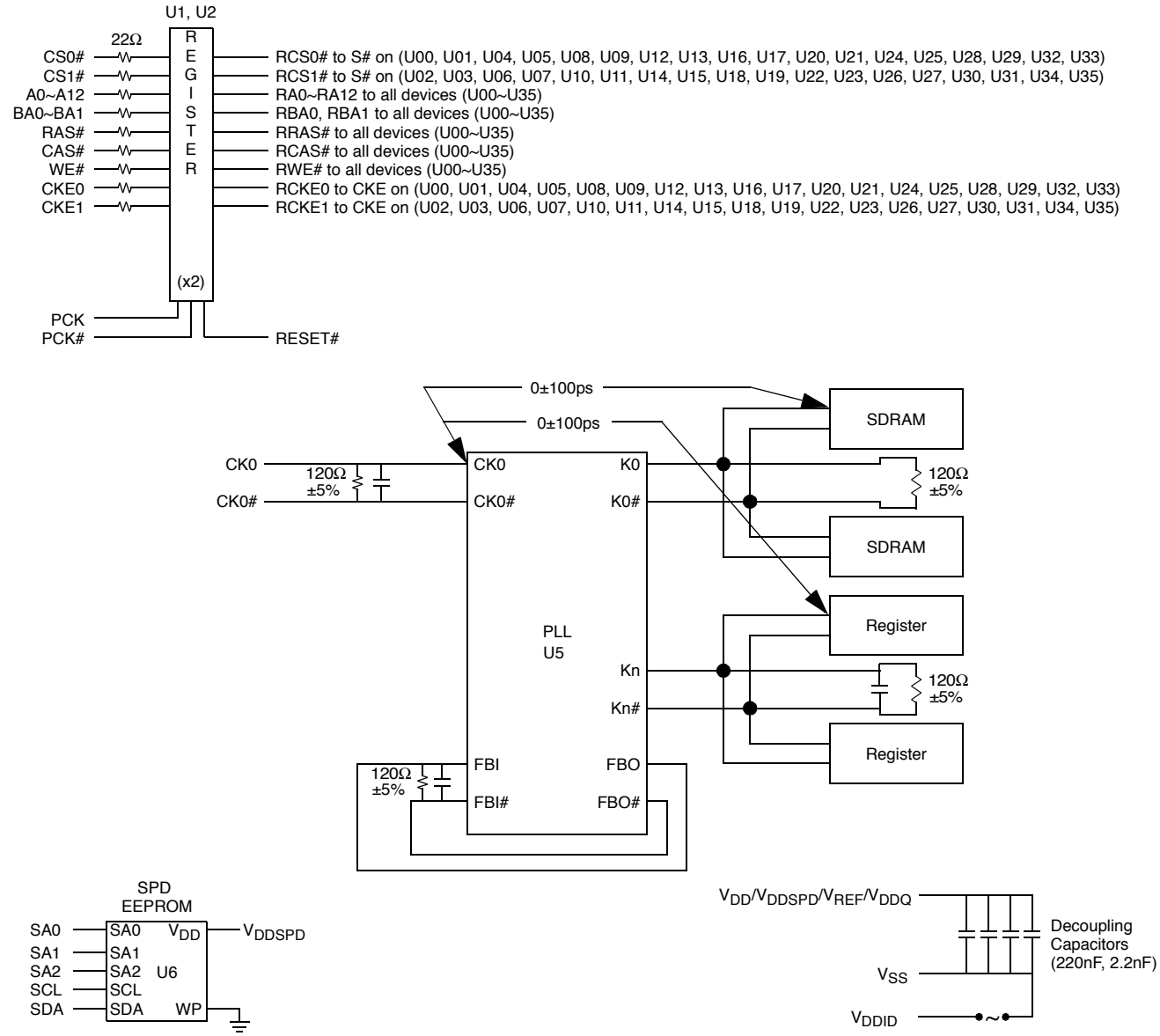
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{REF}	24	DQ17	47	DQS8	70	V_{DD}	93	V_{SS}	116	V_{SS}	139	V_{SS}	162	DQ47
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DQS17	163	NC
3	V_{SS}	26	V_{SS}	49	CB2	72	DQ48	95	DQ5	118	A11	141	A10	164	V_{DDQ}
4	DQ1	27	A9	50	V_{SS}	73	DQ49	96	V_{DDQ}	119	DQS11	142	CB6	165	DQ52
5	DQS0	28	DQ18	51	CB3	74	V_{SS}	97	DQS9	120	V_{DD}	143	V_{DDQ}	166	DQ53
6	DQ2	29	A7	52	BA1	75	NC	98	DQ6	121	DQ22	144	CB7	167	NC
7	V_{DD}	30	V_{DDQ}	53	DQ32	76	NC	99	DQ7	122	A8	145	V_{SS}	168	V_{DD}
8	DQ3	31	DQ19	54	V_{DDQ}	77	V_{DDQ}	100	V_{SS}	123	DQ23	146	DQ36	169	DQS15
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	V_{SS}	147	DQ37	170	DQ54
10	RESET#	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	V_{DD}	171	DQ55
11	V_{SS}	34	V_{SS}	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DQS13	172	V_{DDQ}
12	DQ8	35	DQ25	58	V_{SS}	81	V_{SS}	104	V_{DDQ}	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	V_{DDID}	105	DQ12	128	V_{DDQ}	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DQS12	152	V_{SS}	175	DQ61
15	V_{DDQ}	38	V_{DD}	61	DQ40	84	DQ57	107	DQS10	130	A3	153	DQ44	176	V_{SS}
16	NC	39	DQ26	62	V_{DDQ}	85	V_{DD}	108	V_{DD}	131	DQ30	154	RAS#	177	DQS16
17	NC	40	DQ27	63	WE#	86	DQS7	109	DQ14	132	V_{SS}	155	DQ45	178	DQ62
18	V_{SS}	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	V_{DDQ}	179	DQ63
19	DQ10	42	V_{SS}	65	CAS#	88	DQ59	111	CKE1	134	CB4	157	CS0#	180	V_{DDQ}
20	DQ11	43	A1	66	V_{SS}	89	V_{SS}	112	V_{DDQ}	135	CB5	158	CS1#	181	SA0
21	CKE0	44	CB0	67	DQS5	90	NC	113	NC	136	V_{DDQ}	159	DQS14	182	SA1
22	V_{DDQ}	45	CB1	68	DQ42	91	SDA	114	DQ20	137	CK0	160	V_{SS}	183	SA2
23	DQ16	46	V_{DD}	69	DQ43	92	SCL	115	A12	138	CK0#	161	DQ46	184	V_{DDSPD}

Pin Description Table

Symbol	Type	Polarity	Function
CK0	SSTL	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL. (All DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.)
CK0#	SSTL	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE0, CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#, CS1#	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	SSTL	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0, BA1	SSTL	-	Selects which of the four internal SDRAM banks is activated.
A0~A9, A10/AP, A11~A12	SSTL	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11-A12 defines the column address (CA0-CA9, CA11-CA12) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0~DQ63 CB0~CB7	SSTL	-	Data and Check Bit Input/Output pins.
DQS0~DQS17	SSTL	Negative & Positive Edge	Data strobe for input and output data.
SA0~SA2	LVTTL	-	These signals are tied on the system to either V_{SS} or V_{DD} to configure the serial SPD.
SDA	LVTTL	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected on the system board from the SDA bus line to V_{DD} to act as a pullup.
SCL	LVTTL	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected on the system board from the SCL bus line to V_{DD} to act as a pullup.
RESET#	LV-CMOS	Active Low	This signal is asynchronous and driven low to the register to guarantee that the register outputs are low.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V_{REF}	Supply	-	Reference voltage for SSTL2 inputs.
V_{DDQ}	Supply	-	Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports both 2.3 Volt and 3.3 Volt operation).
NC	-	-	No Connect.

Block Diagram



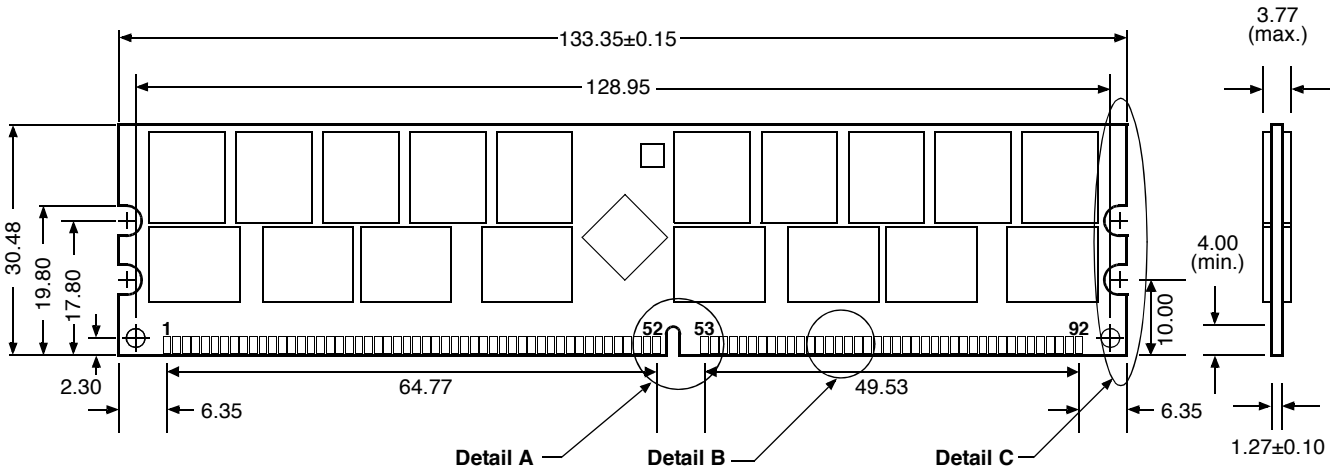


Notes:

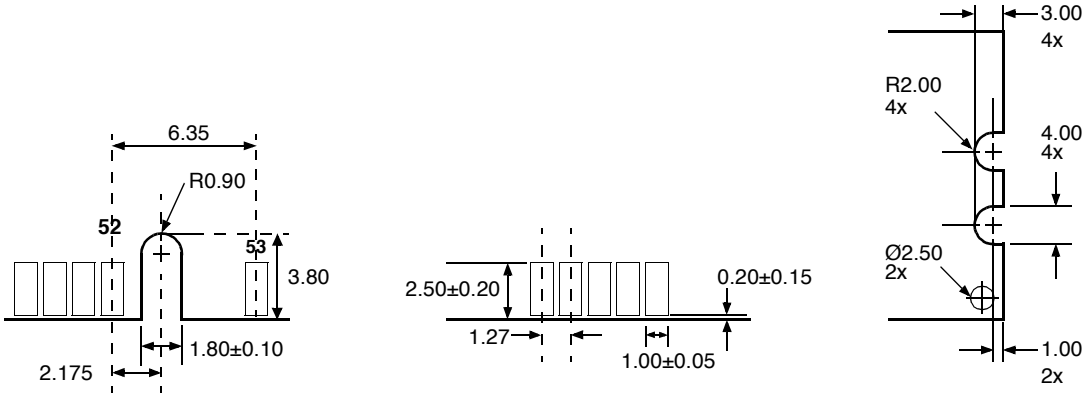
1. Data bits may be swapped within a device. However, DQ/DQS relationship is maintained as shown.
2. DM (Data Mask) pin of all the SDRAM devices is connected to GND on the module.
3. Only one PLL output is shown above. Any additional PLL outputs will be wired in a similar manner.
4. V_{DDID} Definition:
   Strap In (V_{SS}): $V_{DD} \neq V_{DDQ}$
   Strap Out (Open): $V_{DD} = V_{DDQ}$

Physical Dimensions

184-pin DIMM Module



Front View



Detail A **Detail B** **Detail C**

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Serial Presence Detect Table (SG2567RDDR6H2BGIC/SC)

Byte No.	Byte Description	Value Supported	Value in Hex
0	# of bytes written into serial memory at module manufacturer	128 Bytes	80h
1	Total # of bytes of SPD memory device	256 Bytes	08h
2	Fundamental memory type	SDRAM DDR	07h
3	# of row address on this assembly	13	0Dh
4	# of column address on this assembly	12	0Ch
5	# of module rows on this assembly	2	02h
6	Data width of this assembly	72	48h
7	.....Data width of this assembly	-	00h
8	Voltage interface standard of this assembly	SSTL	04h
9	SDRAM cycle time from clock @ CAS latency of 2.5	6.0ns	60h
10	SDRAM access time from clock @ CAS latency of 2.5	0.70ns	70h
11	DIMM configuration type	ECC	02h
12	Refresh rate & type	SR, 7.8	82h
13	Primary SDRAM width	4	04h
14	Error checking SDRAM width	4	04h
15	Minimum clock delay for back-to-back random column address	1	01h
16	SDRAM device attributes : Burst lengths supported	2, 4, 8	0Eh
17	SDRAM device attributes : # of banks on SDRAM device	4	04h
18	SDRAM device attributes : CAS latency	2.0, 2.5	0Ch
19	SDRAM device attributes : CS latency	CS# Latency = 0	01h
20	SDRAM device attributes : Write latency	WE# Latency = 1	02h
21	SDRAM module attributes	Diff. CK, PLL w/ registered control	26h
22	SDRAM device attributes : General	V_{DD} ± 0.2V	C0h
23	SDRAM cycle time from clock @ CAS latency of 2.0	7.5ns	75h
24	SDRAM access time from clock @ CAS latency of 2.0	0.70ns	70h
25	SDRAM cycle time from clock @ CAS latency of 1.5	-	00h
26	SDRAM access time from clock @ CAS latency of 1.5	-	00h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Value in Hex
27	Minimum row precharge time (=tRP)	18ns	48h
28	Minimum row active to row active delay (=tRRD)	12ns	30h
29	Minimum RAS to CAS delay (=tRCD)	18ns	48h
30	Minimum activate precharge time (=tRAS)	42ns	2Ah
31	Module row density	1GB	01h
32	Command and Address signal input setup time	0.75ns	75h
33	Command and Address signal input hold time	0.75ns	75h
34	Data signal input setup time	0.45ns	45h
35	Data signal input hold time	0.45ns	45h
36~40	Reserved for VCSDRAM	Not used	00h
41	Device Minimum activate/auto-refresh time (=tRC)	60ns	3Ch
42	Device Minimum auto-refresh to active/auto-refresh time (=tRFC)	72ns	48h
43	Maximum device cycle time (=tCK max)	12ns	30h
44	Device DQS-DQ skew for DQS and associated DQ signals (=tDQSQ max)	0.45ns	2Dh
45	Device read data hold skew factor (=tQHS)	0.55ns	55h
46~61	Superset Information (reserved for future use)	-	00h
62	SPD data revision code	1.0	10h
63	Checksum for bytes 0~62		E6h
64	Manufacturer JEDEC ID code	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	SMART's ID	94h
66~71	.....Manufacturer JEDEC ID code	Not Used	00h
72	Manufacturing location	See Note 1	01h
73~90	Manufacturer part #	SG25672RDDR6H2BGUU	P. No
91	Manufacturer revision code	Rev. 0	00h
92	.....Manufacturer revision code	None	00h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Value in Hex
93	Manufacturing data (Year)	Date	Date
94	Manufacturing data (Week)	Date	Date
95~98	Assembly serial #	Serial Number	S. No
99~125	Manufacturer specific data	SMART Modular Technologies	
126~127	Unused storage locations		00h
128~255	Unused storage locations		FFh

Note:

1. Manufacturing Location:
   00h - Undefined,
   01h - Fremont, USA,
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia,
   05h - Bangalore, India,
   06h - Sao Paulo, Brazil,
   07h - Aguadilla, Puerto Rico,
   08h - Mayaguez, Puerto Rico,
   09h - Santo Domingo, Dominican Republic,
   0Ah - Dongguan, China,

Mode Register Table Definition

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in the table below. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing). In the table below, note that n = 11 for 128Mb devices, n = 12 for 256Mb and 512Mb devices, and n = 13 for 1Gb devices.

Address Bus	BA1	BA0	An	..	..	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register Bits	Mn+2	Mn+1	Mn	..	..	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
	0	0	Operating Mode						CAS Latency			BT	Burst Length		

M2	M1	M0	Burst Length
0	0	1	2
0	1	0	4
0	1	1	8

M3	Burst Type
0	Sequential
1	Interleave

M6	M5	M4	CAS Latency
0	1	0	2.0
1	1	0	2.5

Mn	..	..	M9	M8	M7	Operating Mode
0	0	0	0	0	0	Normal Operation
0	0	0	0	1	0	Reset DLL

Extended Mode Register Table Definition

The Extended Mode Register is used to control functions beyond those controlled by Mode Register. This definition includes DLL Enable/Disable, Output Drive Strength, and QFC Enable/Disable as shown in table below. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a MODE REGISTER SET Command to the Mode Register (with BA0 = 0 and BA1 = 0) to reset the DLL. In the table below, note that n = 11 for 128Mb devices, n = 12 for 256Mb and 512Mb devices, and n = 13 for 1Gb devices. QFC# option is not currently supported.

Address Bus	BA1	BA0	An	..	..	..	..	..	..	..	A4	A3	A2	A1	A0
Mode Register Bits	En+2	En+1	En	..	..	..	..	..	..	..	E4	E3	E2	E1	E0
	0	1	Operating Mode										QFC#	DS	DLL

E0	DLL
0	Enable
1	Disable

E1	Drive Strength
0	Normal
1	Weak

En	..	..	E5	E4	E3	Operating Mode
0	0	0	0	0	0	Normal Operation
-	-	-	-	-	-	All other states reserved

Commands

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

Truth Table - Commands

Name (Function)	CS#	RAS#	CAS#	WE#	ADDR	Notes
Deselect (NOP)	H	X	X	X	X	9
No Operation (NOP)	L	H	H	H	X	9
Active (Select bank and activate Row)	L	L	H	H	Bank/Row	3
Read (Select bank and column and start Read burst)	L	H	L	H	Bank/Col	4
Write (Select bank and column and start Write burst)	L	H	L	L	Bank/Col	4
Burst Terminate	L	H	H	L	X	8
Precharge (Deactivate Row in bank or banks)	L	L	H	L	Code	5
Auto Refresh or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	6, 7
Load Mode Register	L	L	L	L	Op-Code	2

Truth Table - DM Operation (Note 10)

Name (Function)	DM	DQS
Write Enable	L	Valid
Write Inhibit	H	X

Note:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the Mode Register or the Extended Mode Register (BA0 = 0, BA1 = 0 selects the Mode Register; BA0 = 1, BA1 = 0 selects the Extended Mode Register; other combinations of BA0-BA1 are reserved; A0-An provide the op-code to be written to the selected Mode Register).
3. BA0-BA1 provide bank address and A0-An provide row address.
4. BA0-BA1 provide bank address; A0-Ai provide column address; A10 HIGH enables the autoprecharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0-BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0-BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write date; DM should be asserted in the same cycle as DQ that needs to be masked.

DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-1.0 ~ 3.6	V
Voltage on V_{DDSPD} relative to V_{SS}	V_{DDSPD}	-1.0 ~ 5.5	V
Power Dissipation	P_T	58	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Short Circuit Output Current	I_{OS}	50	mA

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	2.3	2.5	2.7	V
I/O Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V
I/O Reference Voltage	V_{REF}	0.49*V_{DDQ}	-	0.51*V_{DDQ}	V
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
SPD Voltage	V_{DDSPD}	2.3	-	5.5	V
Input High Voltage	$V_{IH(DC)}$	V_{REF} + 0.15	-	V_{DD} + 0.3	V
Input Low Voltage	$V_{IL(DC)}$	-0.3	-	V_{REF} - 0.15	V
Input Voltage Level, CK and CK#	$V_{IN(DC)}$	-0.3	-	V_{DDQ} + 0.3	V
Input Differential Voltage, CK and CK#	$V_{ID(DC)}$	0.36	-	V_{DDQ} + 0.6	V
Ground	V_{SS}	0	0	0	V

Notes:

1. V_{REF} is expected to track variation in V_{DDQ}. V_{REF} = 0.5 x V_{DDQ}.
2. Peak to peak noise on V_{REF} may not exceed 2% V_{REF}.
3. V_{TT} is not used on the module. It is the voltage used on the system board to terminate all the signals. However, this supply should track the variations in DC level of V_{REF}.

Capacitance
(V_{DD} = 2.5V±0.2V, T_A = +25°C, f = 1MHz)

Parameter	Symbol	Max	Unit
Input Capacitance (Address & Control)	C_{I1}	10	pF
Input Capacitance (CK0, CK0#)	C_{I2}	10	pF
Input Capacitance (DQS0~DQS17)	C_{I3}	10	pF
Input/Output Capacitance (DQ0~DQ63, CB0~CB7)	$C_{I/O}$	10	pF

(V_{DD} = 2.5V±0.2V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Test conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{DD}$	-4	4	μA
Output Leakage Current	I_{OZ}	$0V \le V_{out} \le V_{DD}$ DQ's are disabled	-10	10	μA
Output High Current	I_{OH}	$V_{OUT} = V_{TT} + 0.84V$	-16.8	-	mA
Output Low Current	I_{OL}	$V_{OUT} = V_{TT} - 0.84V$	16.8	-	mA

AC Operating Conditions
(V_{DD} = 2.5V±0.2V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Input High Logic Voltage	$V_{IH(AC)}$	V_{REF} + 0.31	-	V	1, 2
Input Low Logic Voltage	$V_{IL(AC)}$	-	V_{REF} - 0.31	V	1, 2
Input differential voltage, CK and CK# inputs	$V_{ID(AC)}$	0.62	V_{DDQ} + 0.6	V	1, 2, 3
Input crossing point voltage, CK and CK# inputs	$V_{IX(AC)}$	$0.5*V_{DDQ}$ - 0.2	$0.5*V_{DDQ}$ + 0.2	V	1, 2, 3

Notes:
1. Input slew rate is 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The value of V_{IX} is expected to equal $0.5*V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

DC Characteristics (Contd.)
(V_{DD} = 2.5V±0.2V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Max	Unit	Notes
		6.0ns CL 2.5		
OPERATING CURRENT: One Bank; Active-Precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cyle; address and control inputs changing once per clock cycle.	IDD0	3150	mA	1
OPERATING CURRENT: One Bank; Active-Read-Precharge; Burst = 2; tRC = tRC MIN; CL = 2.5; tCK = tCK MIN; Iout = 0 mA; Address and control inputs changing once per clock cycle.	IDD1	3690	mA	1
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD2P	480	mA	2
IDLE STANDBY CURRENT: CS# ≥ Vih (MIN); All banks idle; CKE ≥ Vih (MIN); tCK = tCK MIN; Address and other control inputs changing once per clock cycle	IDD2N	1530	mA	2
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; power-down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD3P	1650	mA	1
ACTIVE STANDBY CURRENT: CS# ≥ Vih (MIN); CKE ≥ Vih (MIN); One bank; Active-Precharge; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle.	IDD3N	2070	mA	1
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = tCK MIN; Iout = 0mA	IDD4R	3780	mA	1
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle	IDD4W	3960	mA	1
AUTO REFRESH CURRENT: tRC = tRFC (MIN)	IDD5	4950	mA	3
SELF REFRESH CURRENT: CKE ≤ 0.2 V	IDD6	180	mA	
OPERATING CURRENT: Four Bank operation;Four bank interleaving READs (BL = 4) with auto precharge. tRC= MIN tRC allowed; tCK =tCK MIN; Address and control inputs change only during Active READ, or WRITE commands.	IDD7	7740	mA	1

Notes:
1. One module rank is active. Second module rank is in active standby.
2. All module ranks are idle.
3. One module rank is in refresh. Second module rank is in active standby.
4. IDD specifications are valid after the SDRAMs are properly initialized.

Device AC Characteristics

Parameter		Symbol	6.0ns @ CL 2.5 DDR333B		Unit	Notes
			Min	Max		
Row Cycle Time		t_{RC}	60	-	ns	
Refresh row cycle time		t_{RFC}	72	-	ns	
Row active time		t_{RAS}	42	70K	ns	
RAS# to CAS# delay		t_{RCD}	18	-	ns	
Row precharge time		t_{RP}	18	-	ns	
Row active to Row active delay		t_{RRD}	12	-	ns	
Write recovery time		t_{WR}	15	-	t_{CK}	
Internal write to read command delay		t_{WTR}	1	-	t_{CK}	
Clock cycle time	CL=2.0	t_{CK}	7.5	12	ns	
	CL=2.5		6.0	12	ns	
Clock high level width		t_{CH}	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	t_{CK}	
DQS-out access time from CK/CK#		t_{DQSCK}	-0.60	+0.60	ns	
Output data access time from CK/CK#		t_{AC}	-0.70	+0.70	ns	
DQS-DQ skew (DQS and associated DQ signals)		t_{DQSQ}	-	+0.45	ns	
Read Preamble		t_{RPRE}	0.9	1.1	t_{CK}	
Read Postamble		t_{RPST}	0.4	0.6	t_{CK}	
Data out high impedence time from CK/CK#		t_{HZ}	-	+0.70	ns	7
Data out high impedence time from CK/CK#		t_{LZ}	-0.70	+0.70	ns	7
CK to valid DQS-in		t_{DQSS}	0.75	1.25	t_{CK}	
Write preamble setup time		t_{WPRES}	0	-	ns	2
Write preamble		t_{WPRE}	0.25	-	t_{CK}	
DQS write postamble time		t_{WPST}	0.4	0.6	t_{CK}	3

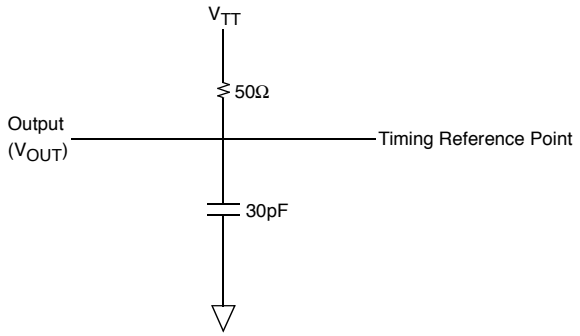
Device AC Characteristics (Cont'd)

Parameter	Symbol	6.0ns @ CL 2.5 DDR333B		Unit	Notes
		Min	Max		
Mode register set cycle time	t_{MRD}	12	-	ns	
Address and Control Input setup time	t_{IS}	0.75	-	ns	6
Address and Control Input hold time	t_{IH}	0.75	-	ns	6
DQ & DM setup time to DQS	t_{DS}	0.45	-	ns	
DQ & DM hold time to DQS	t_{DH}	0.45	-	ns	
DQS-in high level width	t_{DQSH}	0.35	-	t_{CK}	
DQS-in low level width	t_{DQSL}	0.35	-	t_{CK}	
DQS falling edge to CK setup time	t_{DSS}	0.2	-	t_{CK}	
DQS falling edge to CK hold time	t_{DSH}	0.2	-	t_{CK}	
DQ & DM input pulse width	t_{DIPW}	1.75	-	ns	6
Address & Control input pulse width	t_{IPW}	2.2	-	ns	6
Exit self refresh to bank active command	t_{XSNR}	75	-	ns	4
Exit self refresh to read command	t_{XSRD}	200	-	t_{CK}	
Refresh Interval	t_{REF}	-	7.8	μs	1
Data hold skew factor	t_{QHS}	-	0.55	ns	
DQ/DQS Output hold time	t_{QH}	t_{HP}min - t_{QHS}	-	ns	8
Clock half period	t_{HP}	Min(t_{CL}, t_{CH})	-	ns	6
Auto precharge write recovery + Precharge time	t_{DAL}	t_{WR}/t_{CK} + t_{RP}/t_{CK}	-	t_{CK}	

Notes:

1. Maximum burst refresh of 8.
2. The specific requirement is that DQS be valid(HIGH or LOW) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic low. If a previous write was in progress, DQS could be HIGH, LOW or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
3. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. Min(t_{CL},t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device.
6. These parameters guarantee device timing, but they are not necessarily tested on each device.
7. t_{HZ}, and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ) or begins driving (LZ).
8. $t_{QH} = t_{HP} - X$, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL},t_{CH}). X consists of t_{DQSQ}(max), the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
9. The CK/CK# input reference level (for timing reference to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK and CK# is V_{REF}.
10. Inputs are not recognized as valid until V_{REF} stabilizes.
11. CK and CK# slew rates are ≥ 1.0V/ns.

AC Output Load Circuit Diagram



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