Ordering Information		
Part Numbers	**Description**	**Device Vendor**
SG2567RDR212452ES	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Walton, Rev. G SX5104E3GP2B-3B
SG2567RDR212452HC	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Hynix, Rev. C HY5PS12421CFP-Y5-C
SG2567RDR212452IA	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Qimonda, Rev. A HYB18T512400AF-3S
SG2567RDR212452IB	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Qimonda, Rev. B HYB18T512400BF-3S
SG2567RDR212452NA	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Nanya, Rev. A NT5TU128M4AE-3C
SG2567RDR212452NB	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Nanya, Rev. B NT5TU128M4BE-3C
SG2567RDR212452SC	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Samsung, Rev. C K4T51043QC-ZCE6
SG2567RDR212452SE	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, Parity, 128Mx4 Based, PC2-5300, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Samsung, Rev. E K4T51043QE-ZCE6

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Revision History

- **July 31, 2007**
  Added SG2567RDR212452SE to the Ordering Information on page 1.

- **February 2, 2007**
  Added SG2567RDR212452ES, SG2567RDR212452HC, SG2567RDR212452IA & SG2567RDR212452NB to the Ordering Information on page 1.

- **June 2, 2006**
  Datasheet released.

2GByte (256Mx72) DDR2 SDRAM Module - 128Mx4 Based 240-pin DIMM, Registered, ECC, Parity

Features

- Standard : JEDEC
- Configuration : ECC
- Cycle Time : 3.0ns
- CAS# Latency (CL) : 4.0, 5.0
- Posted CAS#/Additive Latency (AL) : 0, 1.0, 2.0, 3.0 & 4.0
- Write Latency (WL) : Read (CAS#) Latency - 1
- Burst Length : 4, 8
- Burst Type : Sequential/Interleave
- No. of Internal Banks per SDRAM : 4
- Operating Voltage : 1.8V
- Refresh : 8K/64ms
- Device Physicals : FBGA
- Lead Finish : Gold
- Length x Height : 133.35mm x 30.00mm
- No. of sides : Double-sided
- Mating Connector (Examples)
  - Vertical : Molex - 87705-0021

DDR2 240-Pin DIMM Pin List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{REF}	31	DQ19	61	A4	91	V_{SS}	121	V_{SS}	151	V_{SS}	181	V_{DDQ}	211	DQS14
2	V_{SS}	32	V_{SS}	62	V_{DDQ}	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	V_{SS}
4	DQ1	34	DQ25	64	V_{DD}	94	V_{SS}	124	V_{SS}	154	V_{SS}	184	V_{DD}	214	DQ46
5	V_{SS}	35	V_{SS}	65	V_{SS}	95	DQ42	125	DQS9	155	DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	V_{SS}	96	DQ43	126	DQS9#	156	DQS12#	186	CK0#	216	V_{SS}
7	DQS0	37	DQS3	67	V_{DD}	97	V_{SS}	127	V_{SS}	157	V_{SS}	187	V_{DD}	217	DQ52
8	V_{SS}	38	V_{SS}	68	PAR_IN	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	V_{DD}	99	DQ49	129	DQ7	159	DQ31	189	V_{DD}	219	V_{SS}
10	DQ3	40	DQ27	70	A10/AP	100	V_{SS}	130	V_{SS}	160	V_{SS}	190	BA1	220	DU
11	V_{SS}	41	V_{SS}	71	BA0	101	SA2	131	DQ12	161	CB4	191	V_{DDQ}	221	DU
12	DQ8	42	CB0	72	V_{DDQ}	102	NC	132	DQ13	162	CB5	192	RAS#	222	V_{SS}
13	DQ9	43	CB1	73	WE#	103	V_{SS}	133	V_{SS}	163	V_{SS}	193	CS0#	223	DQS15
14	V_{SS}	44	V_{SS}	74	CAS#	104	DQS6#	134	DQS10	164	DQS17	194	V_{DDQ}	224	DQS15#
15	DQS1#	45	DQS8#	75	V_{DDQ}	105	DQS6	135	DQS10#	165	DQS17#	195	ODT0	225	V_{SS}
16	DQS1	46	DQS8	76	CS1#	106	V_{SS}	136	V_{SS}	166	V_{SS}	196	A13	226	DQ54
17	V_{SS}	47	V_{SS}	77	ODT1	107	DQ50	137	DU	167	CB6	197	V_{DD}	227	DQ55
18	RESET#	48	CB2	78	V_{DDQ}	108	DQ51	138	DU	168	CB7	198	V_{SS}	228	V_{SS}
19	NC	49	CB3	79	V_{SS}	109	V_{SS}	139	V_{SS}	169	V_{SS}	199	DQ36	229	DQ60
20	V_{SS}	50	V_{SS}	80	DQ32	110	DQ56	140	DQ14	170	V_{DDQ}	200	DQ37	230	DQ61

DDR2 240-pin DIMM Pin List (Contd.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
21	DQ10	51	V_{DDQ}	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	V_{SS}	231	V_{SS}
22	DQ11	52	CKE0	82	V_{SS}	112	V_{SS}	142	V_{SS}	172	V_{DD}	202	DQS13	232	DQS16
23	V_{SS}	53	V_{DD}	83	DQS4#	113	DQS7#	143	DQ20	173	A15 (NC)	203	DQS13#	233	DQS16#
24	DQ16	54	BA2 (NC)	84	DQS4	114	DQS7	144	DQ21	174	A14 (NC)	204	V_{SS}	234	V_{SS}
25	DQ17	55	ERR_OUT#	85	V_{SS}	115	V_{SS}	145	V_{SS}	175	V_{DDQ}	205	DQ38	235	DQ62
26	V_{SS}	56	V_{DDQ}	86	DQ34	116	DQ58	146	DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	DQS11#	177	A9	207	V_{SS}	237	V_{SS}
28	DQS2	58	A7	88	V_{SS}	118	V_{SS}	148	V_{SS}	178	V_{DD}	208	DQ44	238	V_{DDSPD}
29	V_{SS}	59	V_{DD}	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	V_{SS}	240	SA1

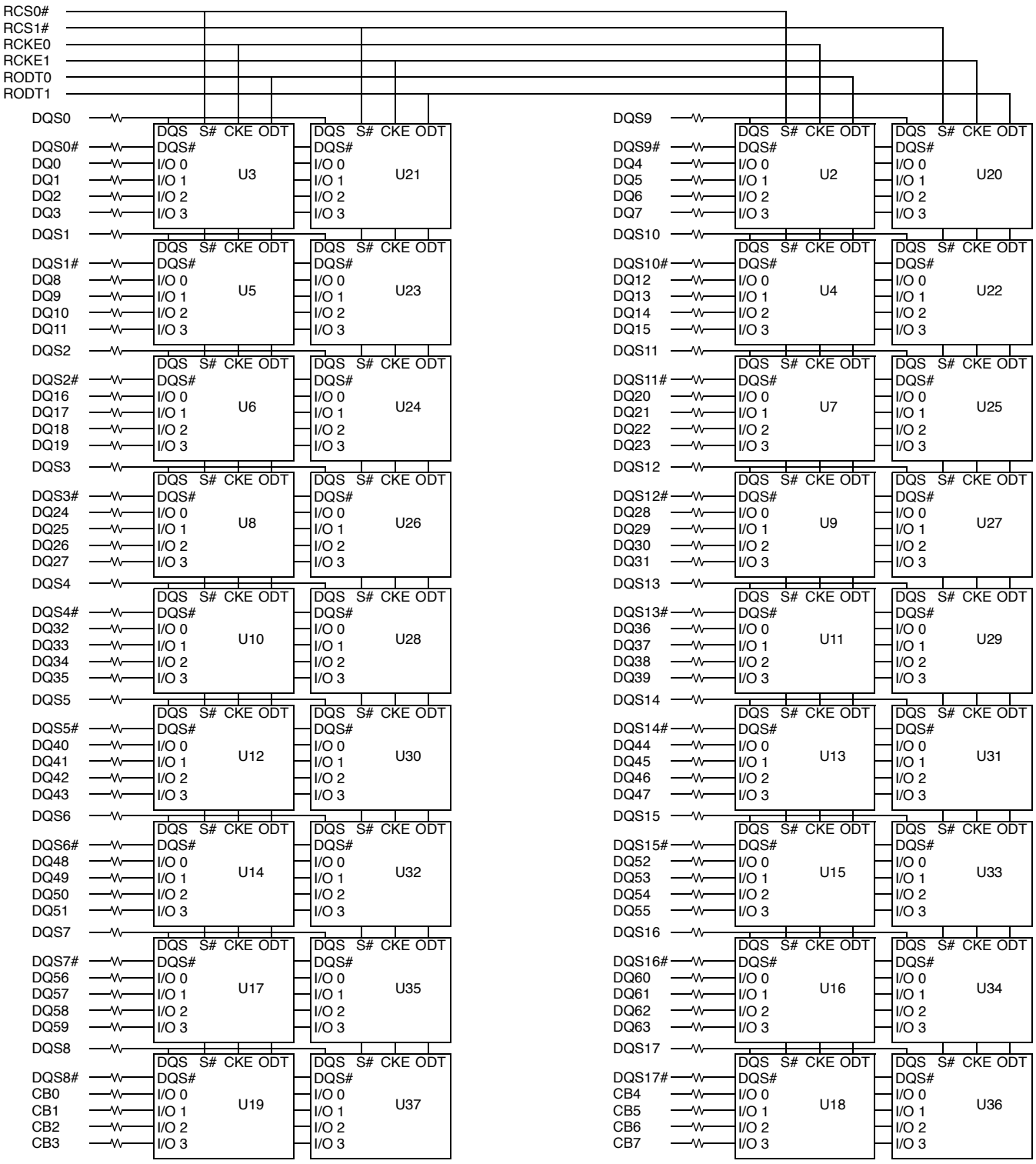
Pin Description Table

Symbol	Type	Polarity	Function
CK0	Input	Positive Edge	Positive line of the differential pair of system clock inputs. (All DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks. Output data is referenced at the crossings of the clocks.)
CK0#	Input	Negative Edge	Negative line of the differential pair of system clock inputs.
ODT0, ODT1	Input	Active High	On-Die Termination: ODT when high enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, and DM. The ODT input will be ignored if disabled in Extended Mode Register (EMRS).
CKE0, CKE1	Input	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#, CS1#	Input	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	Input	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0, BA1	Input	-	Bank Address define to which bank an Activate, Read, Write or Precharge command is being applied. Bank address also determines if the Mode Register or Extended Mode Register is to be accessed during a MRS or EMRS cycle.

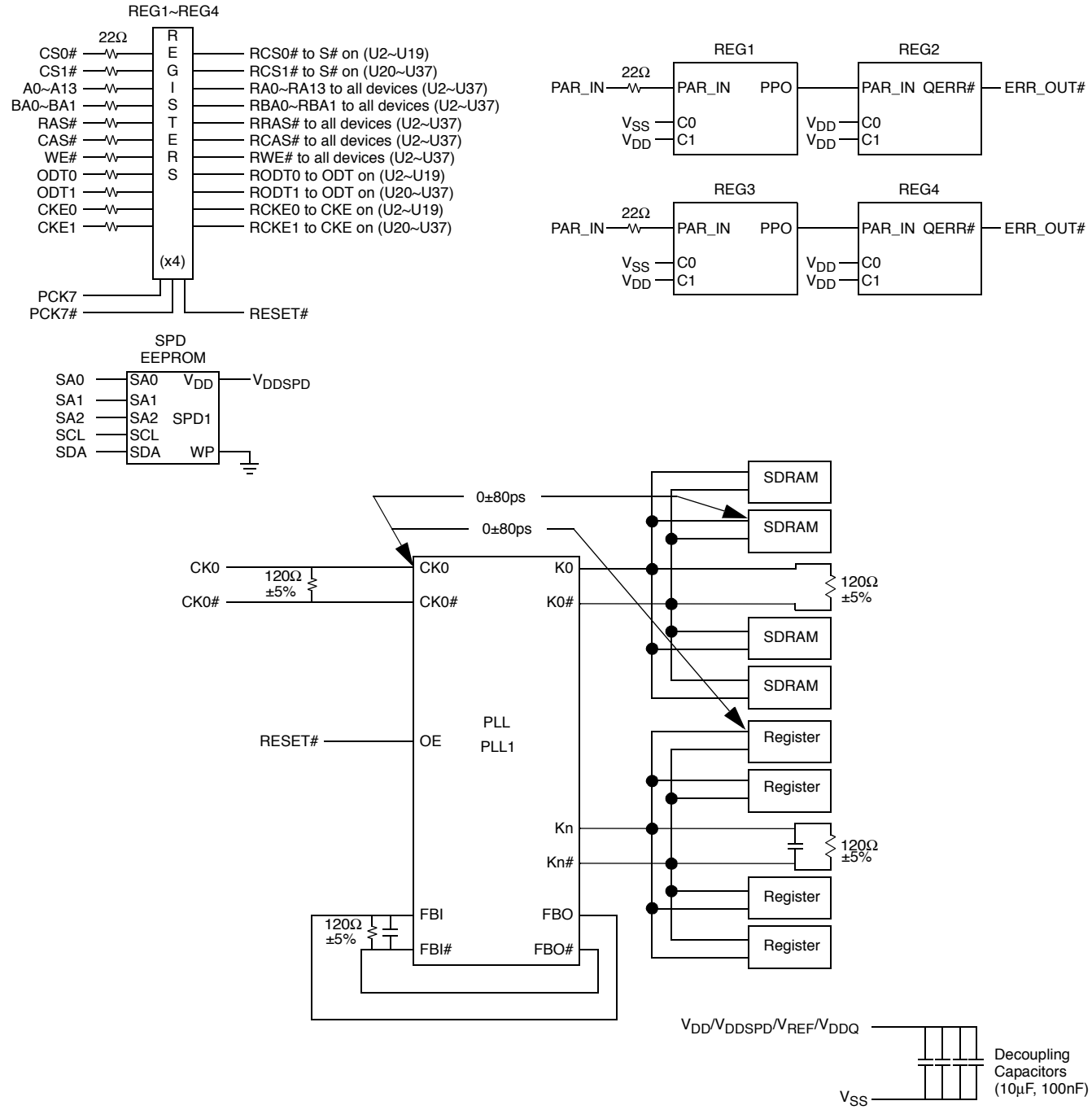
Pin Description Table (Contd.)

Symbol	Type	Polarity	Function
A0~A9, A10/AP, A11~A13	Input	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA9, CA11) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge. The address inputs also provide the op-code during Mode Register Set commands.
DQ0~DQ63 CB0~CB7	Input/ Output	-	Data and Check Bit Input/Output pins.
DQS0~DQS17	Input/ Output	Positive Edge	DDR2 SDRAM differential data strobe for input and output data.
DQS0#~DQS17#	Input/ Output	Negative Edge	DDR2 SDRAM differential data strobe for input and output data.
SA0~SA2	Input	-	Slave Address Select for EEPROM. These pins are used to configure the presence-detect device.
SDA	Input/ Output	-	Serial Bus Data Line for EEPROM. SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. A resistor must be connected from the SDA bus line to V_{DD} to act as pull up on the system board.
SCL	Input	-	Serial Bus Clock for EEPROM. SCL is used to synchronize the presence-detect data transfer to and from the module. A resistor may be connected from the SCL bus line to V_{DD} to act as pull up on the system board.
RESET#	Input	Active Low	Register and PLL control pin. When low, all register outputs will be driven low and the PLL clocks to the DRAM and register will be set to low levels (the PLL will remain synchronized with the input clock, if within spec range).
PAR_IN	Input	-	Parity bit for the Address and Control bus. (“1”: Odd, “0”: Even)
ERR_OUT#	Output	-	Parity error found in the Address and Control bus.
V_{DD}	Supply	-	SDRAM positive power supply. 1.8V±0.1V
V_{SS}	Supply	-	Power supply return (ground).
V_{REF}	Supply	-	SDRAM I/O reference supply.
V_{DDQ}	Supply	-	SDRAM I/O Driver positive power supply. 1.8V±0.1V
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports operation from 1.7V to 3.6V).
NC	-	-	No Connect.
DU	-	-	Do not use.

Block Diagram



Note: Unless otherwise noted, data resistor values are 22Ω ± 5%.

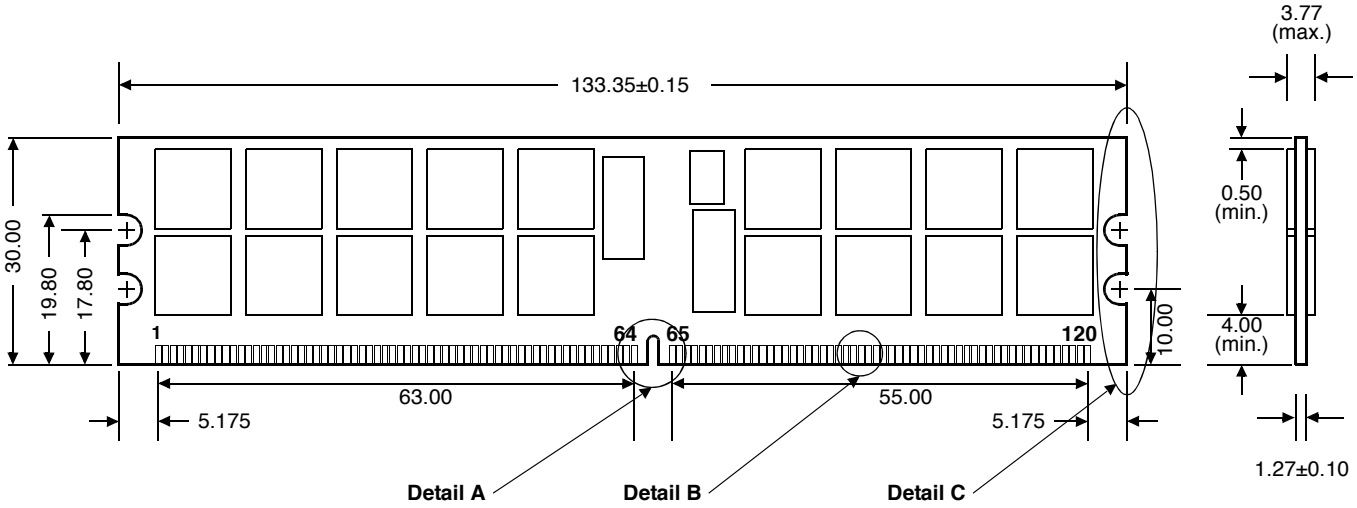


Notes:

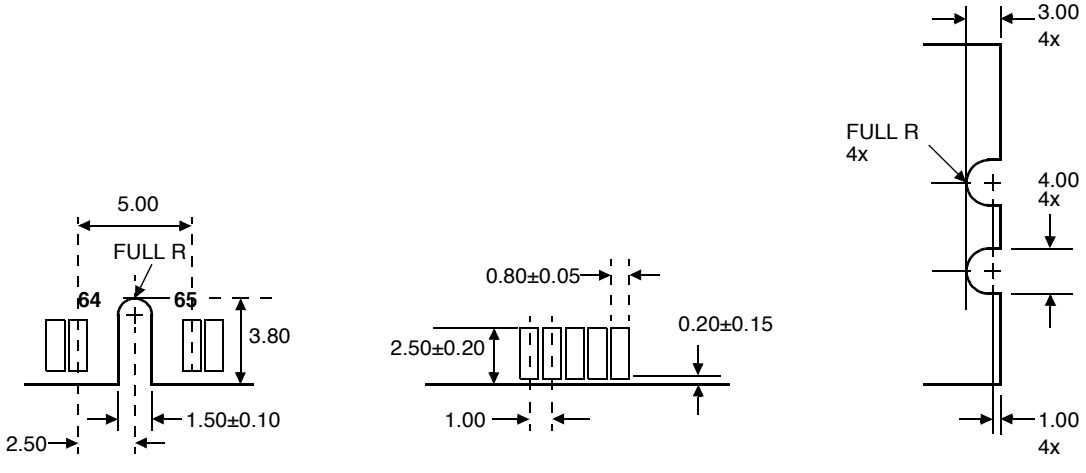
1. DM pin of all SDRAM devices is tied to V_{SS}.
2. PAR_IN has a pull-down resistor of 100KΩ.

Physical Dimensions

240-pin DIMM Module



Front View



Detail A **Detail B** **Detail C**

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Serial Presence Detect Table (SG2567RDR212452ES/HC/IA/IB/NA/NB/SC/SE)

Byte No.	Byte Description	Value Supported	Value in Hex
0	# of bytes written into serial memory at module manufacturer	128 Bytes	80h
1	Total # of bytes of SPD memory device	256 Bytes	08h
2	Fundamental memory type	SDRAM DDR2	08h
3	# of row address on this assembly	14	0Eh
4	# of column address on this assembly	11	0Bh
5	# of Ranks, Package and Height	2, Planar, 30.00mm	61h
6	Data width of this assembly	72	48h
7	Reserved	-	00h
8	Voltage interface standard of this assembly	SSTL_18	05h
9	SDRAM cycle time from clock @ CAS latency of 5.0	3.0ns	30h
10	SDRAM access time from clock @ CAS latency of 5.0	0.45ns	45h
11	DIMM configuration type	Addr./Comm. Parity, ECC	06h
12	Refresh rate & type	SR, 7.8	82h
13	Primary SDRAM width	4	04h
14	Error checking SDRAM width	4	04h
15	Reserved	-	00h
16	SDRAM device attributes : Burst lengths supported	4, 8	0Ch
17	SDRAM device attributes : # of banks on SDRAM device	4	04h
18	SDRAM device attributes : CAS latency	4.0, 5.0	30h
19	Reserved	3.77mm	01h
20	DIMM type information	RDIMM	01h
21	SDRAM module attributes	1 PLL, 4 Reg	07h
22	SDRAM device attributes : General	Weak Driver, 50Ω ODT	03h
23	SDRAM cycle time from clock @ CAS latency of 4.0	3.75ns	3Dh
24	SDRAM access time from clock @ CAS latency of 4.0	0.45ns	45h
25	SDRAM cycle time from clock @ CAS latency of 3.0	-	00h
26	SDRAM access time from clock @ CAS latency of 3.0	-	00h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Value in Hex
27	Minimum row precharge time (=tRP)	15ns	3Ch
28	Minimum row active to row active delay (=tRRD)	7.5ns	1Eh
29	Minimum RAS to CAS delay (=tRCD)	15ns	3Ch
30	Minimum activate precharge time (=tRAS)	45ns	2Dh
31	Module row density	1GB	01h
32	Command and Address signal input setup time	0.20ns	20h
33	Command and Address signal input hold time	0.27ns	27h
34	Data signal input setup time	0.10ns	10h
35	Data signal input hold time	0.17ns	17h
36	Write recovery time (=tWR)	15ns	3Ch
37	Internal write to read command delay (=tWTR)	7.5ns	1Eh
38	Internal read to precharge delay (=tRTP)	7.5ns	1Eh
39	Memory Analysis Probe Characteristics	-	00h
40	Extension of tRC and tRFC	None	00h
41	Device Minimum activate/auto-refresh time (=tRC)	60ns	3Ch
42	Device Minimum auto-refresh to active/auto-refresh time (=tRFC)	105ns	69h
43	Maximum device cycle time (=tCK max)	8ns	80h
44	Device DQS-DQ skew for DQS and associated DQ signals (=tDQSQ max)	0.24ns	18h
45	Device read data hold skew factor (=tQHS)	0.34ns	22h
46	PLL relock time	15μs	0Fh
47~61	Reserved	-	00h
62	SPD data revision code	1.2	12h
63	Checksum for bytes 0~62		54h
64	Manufacturer JEDEC ID code	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	SMART's ID	94h
66~71	.....Manufacturer JEDEC ID code	Not Used	00h
72	Manufacturing location	See Note 1	01h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Value in Hex
73~90	Manufacturer part #	SG25672RDR212452UU	P. No
91	Manufacturer revision code	Rev. 0	00h
92	.....Manufacturer revision code	None	00h
93	Manufacturing data (Year)	Date	Date
94	Manufacturing data (Week)	Date	Date
95~98	Assembly serial #	Serial Number	S. No
99~125	Manufacturer specific data	SMART Modular Technologies	
126~255	Unused storage locations	-	00h

Note:

1. Manufacturing Location:
   00h - Undefined,
   01h - Fremont, USA,
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia,
   05h - Bangalore, India,
   06h - Sao Paulo, Brazil,
   07h - Aguadilla, Puerto Rico,
   08h - Mayaguez, Puerto Rico,
   09h - Santo Domingo, Dominican Republic,
   0Ah - Dongguan, China,

Mode Register Table Definition

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, t_{WR} and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0 and BA1, while controlling the state of address pins A0~A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0~A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4~A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time t_{WR} is defined by A9~A11.

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Mode Register
0[1]	MR		0[1]	0[1]	0	PD	WR			DLL	TM	CAS Latency			BT	Burst Length			

M8	DLL Reset
0	No
1	Yes

M7	Mode
0	Normal
1	Test

M3	Burst Type
0	Sequential
1	Interleave

Burst Length

M2	M1	M0	BL
0	1	0	4
0	1	1	8

M12	Active power down exit time
0	Fast exit (t_{XARD})
1	Slow exit (t_{XARDS})

Write recovery for autoprecharge

M11	M10	M9	WR (cycles)[2]
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

DDR2-400 DDR2-533 DDR2-667 DDR2-800

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2.0 (optional)
0	1	1	3.0 (optional)
1	0	0	4.0
1	0	1	5.0
1	1	0	6.0 (optional)
1	1	1	Reserved

M17	M16	MRS mode
0	0	MRS
0	1	EMRS (1)
1	0	EMRS (2): Reserved
1	1	EMRS (3): Reserved

Notes:
1. BA2 and A14~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. WR min is determinedby t_{CK} max and WR max is determined by t_{CK} min. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer. The mode register must be programmed to this value.

Extended Mode Register Table Definition

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (R_{TT}), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT enable/disable. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Notes:
1. BA2 and A14~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. When the adjust mode of the OCD Calibration Program is issued, AL from previously set value must be applied.
3. After setting the OCD Calibration Program to default, OCD mode needs to be exited by setting A9-A7 to 000.
4. Outputs disabled - DQs, DQSs, DQS#s, RDQSs, RDQS#s. This feature is used in conjunction with DIMM I_{DD} measurements when I_{DDQ} is not desired to be included.
5. If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

Extended Mode Register Table

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	Extended Mode Register
0[1]	EMR		0[1]	0[1]	0	Q_{off}	RDQS	DQS#	OCD Program			R_{TT}	Additive latency			R_{TT}	D.I.C	DLL	

E17	E16	MRS mode
0	0	MRS
0	1	EMRS (1)
1	0	EMRS (2)
1	1	EMRS (3): Reserved

E6	E2	R_{TT} (Nominal)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm

E0	DLL Enable
0	Enable
1	Disable

E9	E8	E7	OCD Calibration Program
0	0	0	OCD calibration mode exit; maintain setting
0	0	1	Drive (1)
0	1	0	Drive (0)
0	1	1	Adjust mode[2] (See page 16)
1	1	1	OCD calibration default[3] (See page 16)

E5	E4	E3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

E12	Q_{off} (Optional)[4] (See page 16)
0	Output buffer enabled
1	Output buffer disabled

E1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

E10	DQS#
0	Enable
1	Disable

E11	RDQS
0	Disable
1	Enable[5] (See page 16)

E11 (RDQS Enable)	E10 (DQS# Enable)	Strobe Function Matrix			
		RDQS/DM	RDQS#	DQS	DQS#
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	DQS#
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	RDQS#	DQS	DQS#
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

Commands

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

Truth Table - Commands

Function	CKE		CS#	RAS#	CAS#	WE#	BA0~BAn[9]	An[8]~A11	A10	A9~A0	Notes
	Previous cycle	Current cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Refresh	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1, 7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge All Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	Column	L	Column	1, 2, 3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1, 2, 3
Read	H	H	L	H	L	H	BA	Column	L	Column	1, 2, 3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1, 2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					

Notes:

1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL=4 cannot be terminated or interrupted.
4. The Power Down Mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. “X” means “H or L (but a defined logic level)”.
7. Self Refresh Exit is asynchronous.
8. An = A12 for 256Mb, A13 for 512Mb & 1 Gb, A14 for 2Gb.
9. BAn = BA1 for up to 512Mb , BA2 for 1 Gb & 2Gb.

DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Notes
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 2.3	V	
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.3	V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.3	V	
Voltage on V_{DDSPD} relative to V_{SS}	V_{DDSPD}	1.7 ~ 3.6	V	
Operating Temperature (Ambient)	T_{OPR}	0 to +65	°C	
Operating Temperature (Case)	T_{CASE}	0 to +85	°C	1, 2
Storage Temperature	T_{STG}	-55 to +100	°C	

Notes:

1. It is possible to operate the DRAM above Case Temperature up to 95ºC.
2. Above 85°C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9μs.

Recommended DC Operating Conditions (T_A = 0 to +65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	
I/O Reference Voltage	V_{REF}	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1, 2
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	3
SPD Voltage	V_{DDSPD}	1.7	-	3.6	V	
Input High Voltage	$V_{IH(DC)}$	V_{REF} + 0.125	-	V_{DDQ} + 0.3	V	
Input Low Voltage	$V_{IL(DC)}$	-0.3	-	V_{REF} - 0.125	V	
Input Voltage Level, CK/CK#	$V_{IN(DC)}$	-0.3	-	V_{DDQ} + 0.3	V	
Input Differential Voltage, CK/CK#	$V_{ID(DC)}$	0.25	-	V_{DDQ} + 0.6	V	
Ground	V_{SS}	0	0	0	V	

Notes:

1. V_{REF} is expected to track variation in V_{DDQ}.
2. Peak to peak noise (non-common mode) on V_{REF} may not exceed ±1% of the DC value. Peak to peak AC noise on V_{REF} may not exceed ±2% of V_{REF} (DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not used on the module. It is the voltage used on the system board to terminate all the signals. However, this supply should track the variations in DC level of V_{REF}.

Capacitance
(V_{DD} = 1.8V±0.1V, T_{Case} = +25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (CKn, CKn#)	C_{CK}	2.0	3.0	pF
Input Capacitance delta (CKn, CKn#)	C_{DCK}	-	-	pF
Input Capacitance (all other input-only pins)	C_{I}	2.5	3.5	pF
Input Capacitance delta (all other input-only pins)	C_{DI}	-	-	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#, CB)	C_{I0}	5.0	7.0	pF
Input/Output Capacitance delta (DQ, DM, DQS, DQS#, CB)	C_{DI0}	-	1.0	pF

AC Operating Conditions
(V_{DD} = 1.8V±0.1V, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Input High Logic Voltage	$V_{IH(AC)}$	V_{REF} + 0.250	-	V	1, 2
Input Low Logic Voltage	$V_{IL(AC)}$	-	V_{REF} - 0.250	V	1, 2
Input differential voltage, CK and CK# inputs	$V_{ID(AC)}$	0.5	V_{DDQ} + 0.6	V	1, 2, 3
Input crossing point voltage, CK and CK# inputs	$V_{IX(AC)}$	0.5*V_{DDQ} - 0.175	0.5*V_{DDQ} + 0.175	V	1, 2, 3
AC differential crossing point voltage	$V_{OX(AC)}$	0.5*V_{DDQ} - 0.125	0.5*V_{DDQ} + 0.125	V	3

Notes:
1. Input slew rate is 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The value of V_{IX}/V_{OX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

ODT DC Electrical Characteristics

Parameter	Symbol	Min	Nom	Max	Unit	Notes
R_{TT} effective impedence value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT1(EFF)}$	60	75	90	Ω	1
R_{TT} effective impedence value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT2(EFF)}$	120	150	180	Ω	1
R_{TT} effective impedence value for 50Ω setting EMR (A6, A2) = 1, 1	$R_{TT3(EFF)}$	40	50	60	Ω	1
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	-6		+6	%	2

Notes:

1. $R_{TT1(EFF)}$ and $R_{TT2(EFF)}$ are determined by applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to pin under test separately, then measure current $I(V_{IH(AC)})$ and $I(V_{IL(AC)})$ respectively. $R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$
2. Measured voltage (VM) at tested pin with no load.

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1\right) \times 100\,\%$$

Output DC Current Drive

Parameter	Symbol	Min	Max	Unit	Notes
Output Minimum Source DC Current	I_{OH}	-13.4	-	mA	1, 3, 4
Output Minimum Sink DC Current	I_{OL}	13.4	-	mA	2, 3, 4

Notes:

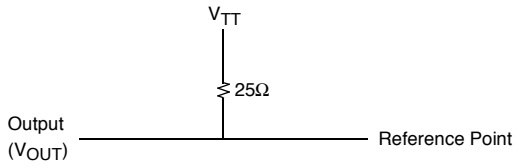
1. For I_{OH} (DC); V_{DDQ} = 1.7V, V_{OUT} = 1420mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV.
2. For I_{OL} (DC); V_{DDQ} = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of I_{OH} (DC) and I_{OL} (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21Ω load line to define a convenient driver current for measurement.

OCD Default Output Characteristics
(V_{DD} = 1.8V±0.1V, V_{SS} = 0V, T_A = 0 to +65°C)

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Output Impedance		12.6	18	23.4	Ω	1, 2
Pull-up and Pull-down mismatch		0		4	Ω	1, 2, 3
Output Slew Rate	S_{OUT}	1.5		5	V/ns	1, 4, 5, 7
Output Step Size for Calibration		0		1.5	Ω	6

Notes:
1. Absolute specifications: 0°C ≤ T_{case} ≤ +85°C; V_{DDQ} = +1.8V±0.1V, V_{DD} = +1.8V±0.1V.
2. Impedance measurement condition for output source DC current: V_{DDQ} = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - V_{DDQ})/I_{OH} must be less than 23.4Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV. Impedance measurement condition for output sink DC current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single ended signals. For differential signals output slew rate is measured between DQS - DQS# = -500mV and DQS# - DQS = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from V_{IL} (DC) max to V_{IH} (DC) min is equal to or greater than the slew rate as measured from V_{IL} (AC) max to V_{IH} (AC) min. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18Ω at nominal conditions across all process and represent only the DRAM uncertainty.
7. Timing skew due to DRAM output slew rate mis-match between DQS/DQS# and associated DQs is included in t_{DQSQ} and t_{QHS} specification.

Output Slew Rate Load Diagram



IDD Specification Parameters and Test Conditions
(V_{DD} = 1.8V±0.1V, V_{SS} = 0V, T_A = 0 to +65°C)

Symbol	Parameter		3.0ns CL 5.0	Unit
IDD0	**Operating one bank active–precharge current;** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		5140	mA
IDD1	**Operating one bank active–read–precharge current;** I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		5410	mA
IDD2P	**Precharge power–down current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		2260	mA
IDD2Q	**Precharge quiet standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		2800	mA
IDD2N	**Precharge standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		3160	mA
IDD3P	**Active power–down current;** All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	3880	mA
		Slow PDN Exit MRS(12) = 1	3610	mA
IDD3N	**Active standby current;** All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		4420	mA
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		6580	mA
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		6760	mA
IDD5B	**Burst refresh current;** $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		8020	mA
IDD6	**Self refresh current;** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		216	mA
IDD7	**Operating bank interleave read current;** All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R		8560	mA

IDD Specification Parameters and Test Conditions (Contd.)

Notes:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#. IDD values must be met with all combinations of ERMS bits 10 and 11.
5. Definitions for IDD

LOW	=	$V_{in} \leq V_{IL(AC)}$(max)
HIGH	=	$V_{in} \geq V_{IH(AC)}$(min)
STABLE	=	inputs stable at a HIGH or LOW level
FLOATING	=	inputs at $V_{REF} = V_{DDQ}/2$
SWITCHING	=	inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks of strobes.

IDD Testing Parameters

	DDR2–667	
Parameter	**5-5-5**	**Units**
CL(IDD)	5	t_{CK}
$t_{RCD(IDD)}$	15	ns
$t_{RC(IDD)}$	60	ns
$t_{RRD(IDD)}$	7.5	ns
$t_{CK(IDD)}$	3	ns
$t_{RASmin(IDD)}$	45	ns
$t_{RASmax(IDD)}$	70000	ns
$t_{RP(IDD)}$	15	ns
$t_{RFC(IDD)}$	105	ns

Device AC Operating Conditions

Parameter		Symbol	3.0ns @ CL 5.0 DDR2-667		Unit	Notes
			Min	Max		
Clock cycle time	CL=5.0	t_{CK}	3000	8000	ps	12, 20
	CL=4.0		3750	8000	ps	12, 20
Clock high-level width		t_{CH}	0.45	0.55	t_{CK}	14
Clock low-level width		t_{CL}	0.45	0.55	t_{CK}	14
Clock half period		t_{HP}	Min (t_{CL}, t_{CH})	-	ps	15
DQ output access time from CK/CK#		t_{AC}	-450	+450	ps	
Data-out high-impedence window from CK/CK#		t_{HZ}	-	t_{AC}(max)	ps	4, 5
Data-out low-impedence window from CK/CK#		t_{LZ}	t_{AC}(min)	t_{AC}(max)	ps	4, 6
DQ & DM input setup time relative to DQS		t_{DS}	100	-	ps	3, 11, 17
DQ & DM input hold time relative to DQS		t_{DH}	175	-	ps	3, 11, 17
DQ & DM input pulse width (for each input)		t_{DIPW}	0.35	-	t_{CK}	
Data hold skew factor		t_{QHS}	-	340	ps	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	t_{HP} - t_{QHS}	-	ps	11,13
DQS input high pulse width		t_{DQSH}	0.35	-	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35	-	t_{CK}	
DQS output access time from CK/CK#		t_{DQSCK}	-400	+400	ps	
DQS falling edge to CK rising - setup time		t_{DSS}	0.2	-	t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.2	-	t_{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	240	ps	11,13
DQS read preamble		t_{RPRE}	0.9	1.1	t_{CK}	18
DQS read postamble		t_{RPST}	0.4	0.6	t_{CK}	
DQS write preamble setup time		t_{WPRES}	0	-	ps	8, 9
DQS write preamble		t_{WPRE}	0.35	-	t_{CK}	
DQS write postamble		t_{WPST}	0.4	0.6	t_{CK}	7
Write command to first DQS latching transition		t_{DQSS}	WL - 0.25	WL + 0.25	t_{CK}	
Address & control input pulse width for each input		t_{IPW}	0.6	-	t_{CK}	
Address and control input setup time		t_{IS}	200	-	ps	2, 17
Address and control input hold time		t_{IH}	275	-	ps	2, 17
CAS# to CAS# command delay		t_{CCD}	2	-	t_{CK}	
OCD Drive mode delay		t_{OIT}	0	12	ns	
CKE low to CK, CK# uncertainity		t_{DELAY}	3.475	3.475	ns	24

Device AC Operating Conditions (Contd.)

Parameter	Symbol	3.0ns @ CL 5.0 DDR2-667		Unit	Notes
		Min	Max		
ACTIVE to ACTIVE (same bank) command	t_{RC}	60	-	ns	
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5	-	ns	23
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	ns	
ACTIVE to PRECHARGE command	t_{RAS}	45	70000	ns	16
Internal READ to precharge command delay	t_{RTP}	7.5	-	ns	19, 23
Write recovery time	t_{WR}	15	-	ns	23
Auto precharge write recovery + Precharge time	t_{DAL}	$t_{WR} + t_{RP}$	-	t_{CK}	18
Internal WRITE to READ command delay	t_{WTR}	7.5	-	ns	23
PRECHARGE command period	t_{RP}	15	-	ns	
LOAD MODE command cycle time	t_{MRD}	2	-	t_{CK}	
REFRESH to REFRESH command interval	t_{RFC}	105	-	ns	10
Average periodic refresh Interval	t_{REFI}	-	7.8	μs	10
Exit self refresh to non-READ command	t_{XSNR}	t_{RFC}(min) + 10	-	ns	
Exit self refresh to READ command	t_{XSRD}	200	-	t_{CK}	
ODT turn-on delay	t_{AOND}	2	2	t_{CK}	
ODT turn-on	t_{AON}	t_{AC}(min)	t_{AC}(max) + 1000	ps	21
ODT turn-off delay	t_{AOFD}	2.5	2.5	t_{CK}	
ODT turn-off	t_{AOF}	t_{AC}(min)	t_{AC}(max) + 700	ps	22
ODT turn-on (power-down mode)	t_{AONPD}	t_{AC}(min) + 2000	2*t_{CK} + t_{AC}(max) + 1000	ps	
ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC}(min) + 2000	2.5*t_{CK} + t_{AC}(max) + 1000	ps	
ODT to power-down entry latency	t_{ANPD}	3		t_{CK}	
ODT power-down exit latency	t_{AXPD}	8		t_{CK}	
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	t_{CK}	
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	7 - AL	-	t_{CK}	
Exit precharge power down to any non-read command	t_{XP}	2	-	t_{CK}	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	-	t_{CK}	

Notes:

1. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level.
2. Command/Address minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of CK/CK#. t_{IS} timing is referenced to $V_{IH\ (AC)}$ for a rising signal and $V_{IL\ (AC)}$ for a fallng signal. t_{IH} timing is referenced to $V_{IH\ (DC)}$ for a rising signal and $V_{IL\ (DC)}$ for a fallng signal. Derating values for Command/Address input signal slew rates < 1.0V/ns are TBD.
3. Data minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of DQS/DQS# if differential strobe feature is enabled. t_{DS} timing is referenced to $V_{IH\ (AC)}$ for a rising signal and $V_{IL\ (AC)}$ for a fallng signal. t_{DH} timing is referenced to $V_{IH\ (DC)}$ for a rising signal and $V_{IL\ (DC)}$ for a fallng signal. Derating values for Data input signal slew rates < 1.0V/ns are TBD.
4. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (t_{HZ}) or begins driving (t_{LZ}).
5. This maximum value is derived from the reference test load. $t_{HZ\ (MAX)}$ will prevail over a $t_{DQSCK\ (MAX)} + t_{RPST\ (MAX)}$ condition.
6. $t_{LZ\ (MIN)}$ will prevail over a $t_{DQSCK\ (MIN)} + t_{RPRE\ (MAX)}$ condition.
7. The intent of the Don't Care state after completion of the postamble is the DQS driven signal should be high, low or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high [above $V_{IH\ DC\ (MIN)}$] then it must not transition low (below $V_{IH\ DC}$) prior to $t_{DQSH(min)}$.
8. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
9. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during his time depending on t_{DQSS}.
10. The refresh period is 64ms. This equates to an average refresh rate of 7.8125μs. However, an REFRESH comand must be asserted at least once every 70.3μs or $t_{RFC\ (MAX)}$; issuing more than eight REFRESH commands back to back at $t_{RFC\ (min)}$ is not allowed.
11. Each byte lane has a corresponding DQS.
12. CK and CK# input slew rate must be ≥ 1 V/ns (≥ 2 V/ns if measured differentially).
13. The data valid window is derived by achieving other specifications: $t_{HP,}$ (t_{CK}/2), t_{DQSQ}, and t_{QH} ($t_{QH} = t_{HP} - t_{QHS}$). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
14. MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
15. $t_{HP\ (MIN)}$ is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK# inputs.
16. READs and WRITEs with no auto precharge are allowed to be issued before $t_{RAS\ (MIN)}$ is satisfied since t_{RAS} lockout feature is supported in DDR2 SDRAM.
17. V_{IL}/V_{IH} DDR2 overshoot/undershoot. Refer to 256MB, 512MB, or 1GB DDR2 SDRAM component data sheet for more detailed information.
18. $t_{DAL} = (n_{WR}) + (t_{RP}/t_{CK})$: For each of the terms above, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period; n_{WR} refers to the t_{WR} parameter stored in the MR[11,10,9].
19. This is a minimum requirement. Minimum READ to internal PRECHARGE timing is AL + BL/2 providing the t_{RTP} and $t_{RAS\ (MIN)}$ have been satisfied. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until $t_{RAS\ (MIN)}$ has been satisfied.
20. Operating frequency is only allowed to change during self refresh mode or precharge power-down mode. Anytime the operating frequency is changed, not including jitter, the DLL is required to be reset followed by 200 clock cycles.
21. ODT turn-on time $t_{AON\ (MIN)}$ is when the device leaves high impedence and ODT resistance begins to turn-on. ODT turn-on time $t_{AON\ (MAX)}$ is when the resistance is fully on. Both are measured from t_{AOND}.
22. ODT turn-off time $t_{AOF\ (MIN)}$ is when the device starts to turn-off ODT resistance. ODT turn-off time $t_{AOF\ (MAX)}$ is when the bus is in high impedence. Both are measured from t_{AOFD}.
23. This parameter has a two clock minimum requirement at any t_{CK}.
24. t_{DELAY} is calculated from $t_{IS} + t_{CK} + t_{IH}$ so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system reset condition.

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