

**Ordering Information**

Part Numbers	Description	Device Vendor
SG2567RDR212435IB	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, 128Mx4 Based, PC2-3200, DDR2-400-333, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Qimonda, Rev. B HYB18T512400BF-5
SG2567RDR212435NB	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, 128Mx4 Based, PC2-3200, DDR2-400-333, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Nanya, Rev. B NT5TU128M4BE-3C
SG2567RDR212435SE	256Mx72 (2GB), DDR2, 240-pin DIMM, Registered, ECC, 128Mx4 Based, PC2-3200, DDR2-400-333, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	Samsung, Rev. E K4T51043QE-ZCE6

(All specifications of this module are subject to change without notice.)



## Revision History

- **September 25, 2007**  
Datasheet released.



**2GByte (256Mx72) DDR2 SDRAM Module - 128Mx4 Based  
240-pin DIMM, Registered, ECC**

**Features**

- Standard : JEDEC
- Configuration : ECC
- Cycle Time : 5.0ns
- CAS# Latency : 3.0, 4.0
- Posted CAS#/Additive Latency (AL) : 0, 1.0, 2.0, 3.0 & 4.0
- Write Latency (WL) : Read (CAS#) Latency - 1
- Burst Length : 4, 8
- Burst Type : Sequential/Interleave
- No. of Internal Banks per SDRAM : 4
- Operating Voltage : 1.8V
- Refresh : 8K/64ms
- Device Physicals : FBGA
- Lead Finish : Gold
- Length x Height : 133.35mm x 30.00mm
- No. of sides : Double-sided
- Mating Connector (Examples)  
Vertical : Molex - 87705-0021

**DDR2 240-Pin DIMM Pin List**

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>REF</sub>	31	DQ19	61	A4	91	V <sub>SS</sub>	121	V <sub>SS</sub>	151	V <sub>SS</sub>	181	V <sub>DDQ</sub>	211	DQS14
2	V <sub>SS</sub>	32	V <sub>SS</sub>	62	V <sub>DDQ</sub>	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	DQS14#
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	V <sub>SS</sub>
4	DQ1	34	DQ25	64	V <sub>DD</sub>	94	V <sub>SS</sub>	124	V <sub>SS</sub>	154	V <sub>SS</sub>	184	V <sub>DD</sub>	214	DQ46
5	V <sub>SS</sub>	35	V <sub>SS</sub>	65	V <sub>SS</sub>	95	DQ42	125	DQS9	155	DQS12	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	V <sub>SS</sub>	96	DQ43	126	DQS9#	156	DQS12#	186	CK0#	216	V <sub>SS</sub>
7	DQS0	37	DQS3	67	V <sub>DD</sub>	97	V <sub>SS</sub>	127	V <sub>SS</sub>	157	V <sub>SS</sub>	187	V <sub>DD</sub>	217	DQ52
8	V <sub>SS</sub>	38	V <sub>SS</sub>	68	DU	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	V <sub>DD</sub>	99	DQ49	129	DQ7	159	DQ31	189	V <sub>DD</sub>	219	V <sub>SS</sub>
10	DQ3	40	DQ27	70	A10/AP	100	V <sub>SS</sub>	130	V <sub>SS</sub>	160	V <sub>SS</sub>	190	BA1	220	DU
11	V <sub>SS</sub>	41	V <sub>SS</sub>	71	BA0	101	SA2	131	DQ12	161	CB4	191	V <sub>DDQ</sub>	221	DU
12	DQ8	42	CB0	72	V <sub>DDQ</sub>	102	NC	132	DQ13	162	CB5	192	RAS#	222	V <sub>SS</sub>
13	DQ9	43	CB1	73	WE#	103	V <sub>SS</sub>	133	V <sub>SS</sub>	163	V <sub>SS</sub>	193	CS0#	223	DQS15
14	V <sub>SS</sub>	44	V <sub>SS</sub>	74	CAS#	104	DQS6#	134	DQS10	164	DQS17	194	V <sub>DDQ</sub>	224	DQS15#
15	DQS1#	45	DQS8#	75	V <sub>DDQ</sub>	105	DQS6	135	DQS10#	165	DQS17#	195	ODT0	225	V <sub>SS</sub>
16	DQS1	46	DQS8	76	CS1#	106	V <sub>SS</sub>	136	V <sub>SS</sub>	166	V <sub>SS</sub>	196	A13	226	DQ54
17	V <sub>SS</sub>	47	V <sub>SS</sub>	77	ODT1	107	DQ50	137	DU	167	CB6	197	V <sub>DD</sub>	227	DQ55
18	RESET#	48	CB2	78	V <sub>DDQ</sub>	108	DQ51	138	DU	168	CB7	198	V <sub>SS</sub>	228	V <sub>SS</sub>
19	NC	49	CB3	79	V <sub>SS</sub>	109	V <sub>SS</sub>	139	V <sub>SS</sub>	169	V <sub>SS</sub>	199	DQ36	229	DQ60
20	V <sub>SS</sub>	50	V <sub>SS</sub>	80	DQ32	110	DQ56	140	DQ14	170	V <sub>DDQ</sub>	200	DQ37	230	DQ61

**DDR2 240-pin DIMM Pin List (Contd.)**

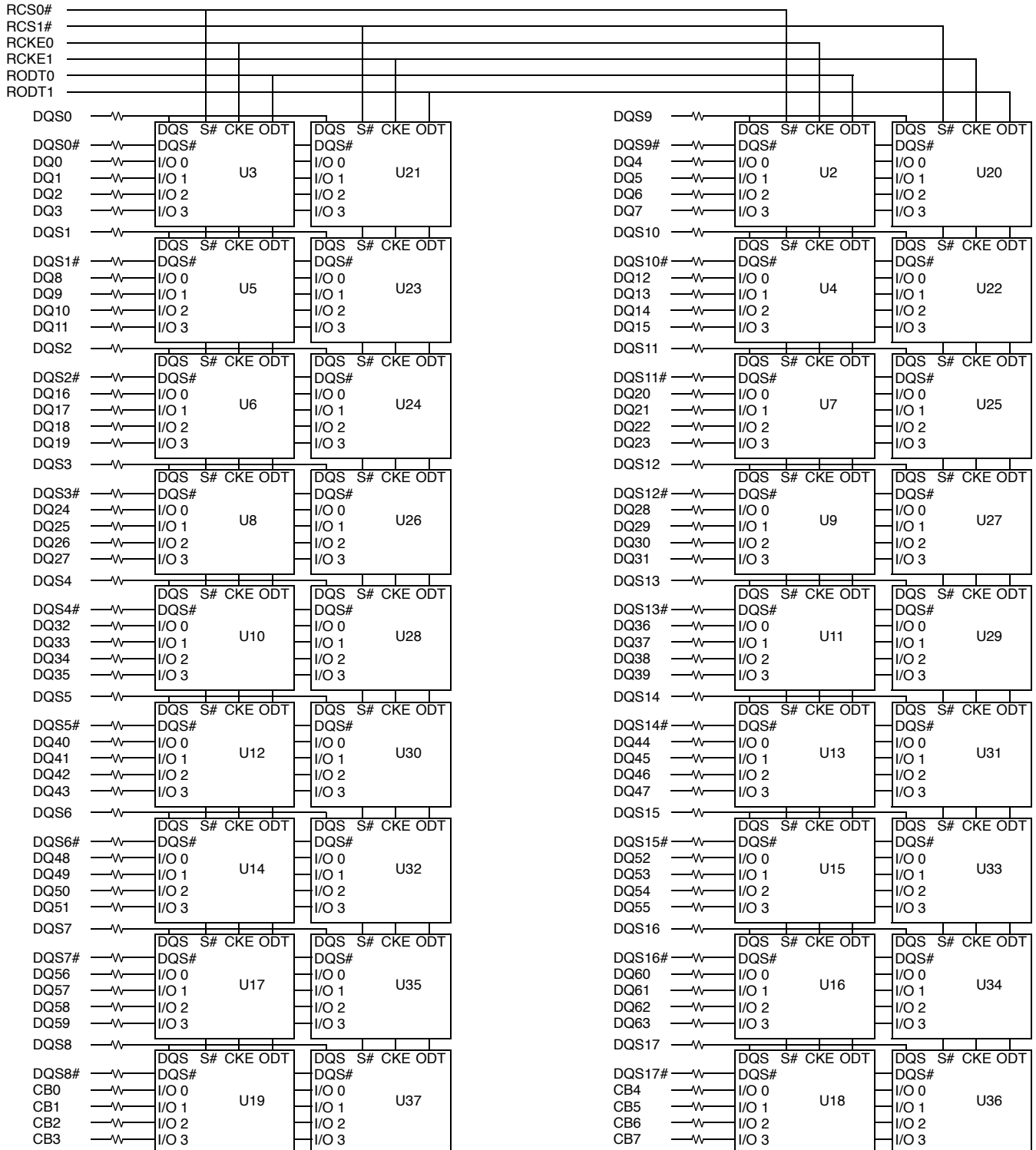
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
21	DQ10	51	V <sub>DDQ</sub>	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	V <sub>SS</sub>	231	V <sub>SS</sub>
22	DQ11	52	CKE0	82	V <sub>SS</sub>	112	V <sub>SS</sub>	142	V <sub>SS</sub>	172	V <sub>DD</sub>	202	DQS13	232	DQS16
23	V <sub>SS</sub>	53	V <sub>DD</sub>	83	DQS4#	113	DQS7#	143	DQ20	173	A15 (NC)	203	DQS13#	233	DQS16#
24	DQ16	54	BA2	84	DQS4	114	DQS7	144	DQ21	174	A14 (NC)	204	V <sub>SS</sub>	234	V <sub>SS</sub>
25	DQ17	55	DU	85	V <sub>SS</sub>	115	V <sub>SS</sub>	145	V <sub>SS</sub>	175	V <sub>DDQ</sub>	205	DQ38	235	DQ62
26	V <sub>SS</sub>	56	V <sub>DDQ</sub>	86	DQ34	116	DQ58	146	DQS11	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	DQS11#	177	A9	207	V <sub>SS</sub>	237	V <sub>SS</sub>
28	DQS2	58	A7	88	V <sub>SS</sub>	118	V <sub>SS</sub>	148	V <sub>SS</sub>	178	V <sub>DD</sub>	208	DQ44	238	V <sub>DDSPD</sub>
29	V <sub>SS</sub>	59	V <sub>DD</sub>	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	V <sub>SS</sub>	240	SA1

**Pin Description Table**

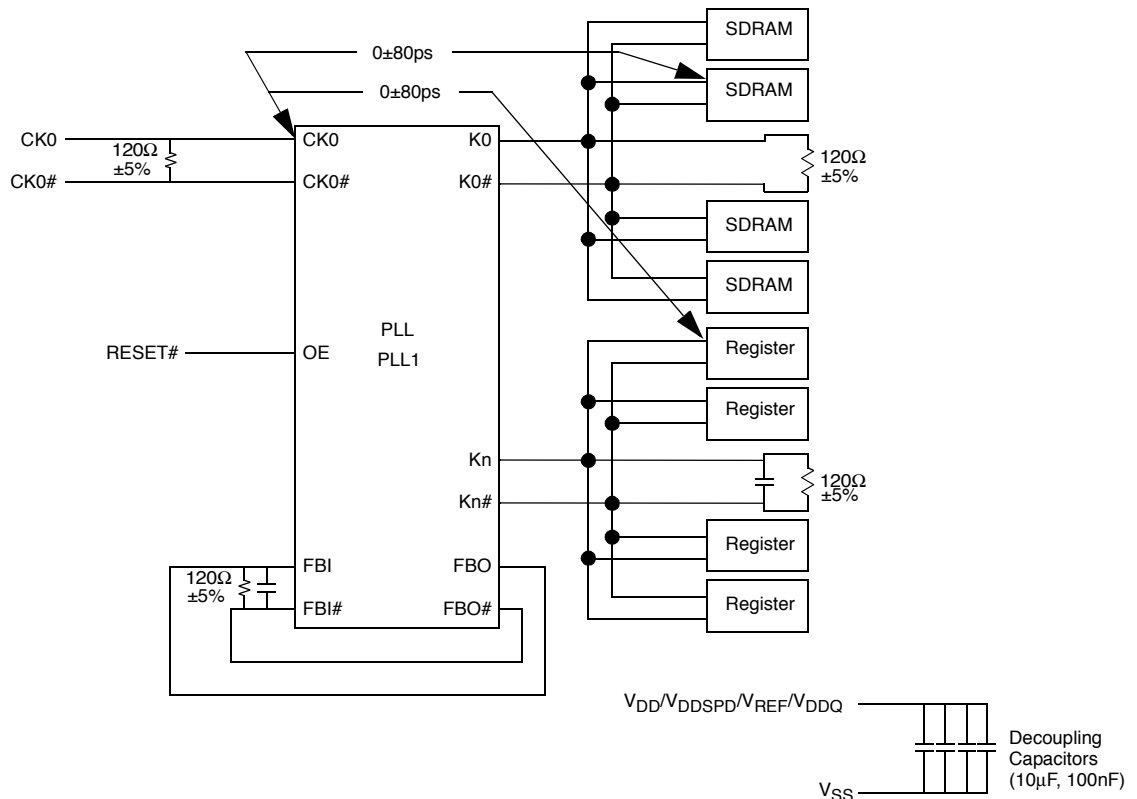
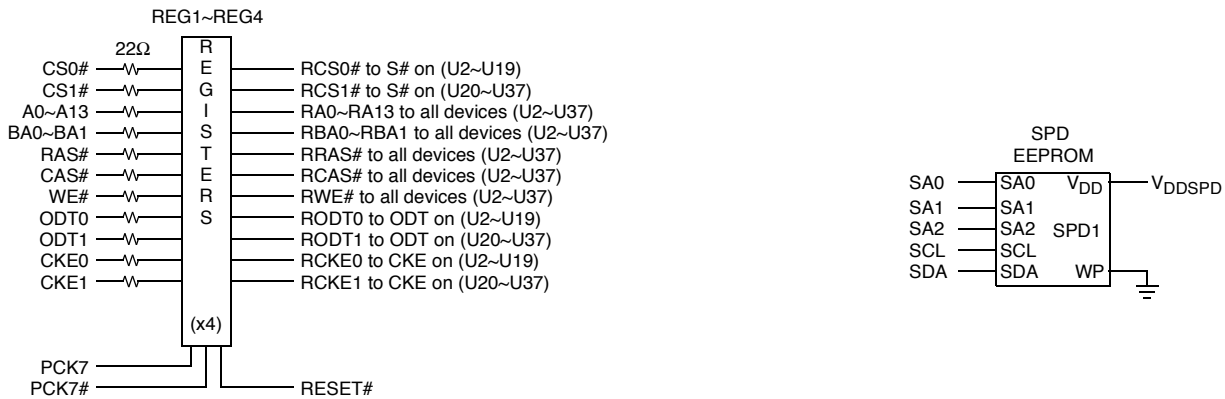
Symbol	Type	Polarity	Function
CK0	SSTL_18	Positive Edge	Positive line of the differential pair of system clock inputs. (All DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks. Output data is referenced at the crossings of the clocks.)
CK0#	SSTL_18	Negative Edge	Negative line of the differential pair of system clock inputs.
ODT0, ODT1	SSTL_18	Active High	On-Die Termination: ODT when high enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, and DM. The ODT input will be ignored if disabled in Extended Mode Register (EMRS).
CKE0, CKE1	SSTL_18	Active High	Activates the DDR2 SDRAM CLK signal when high and deactivates the CLK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#, CS1#	SSTL_18	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	SSTL_18	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0~BA1	SSTL_18	-	Bank Address define to which bank an Activate, Read, Write or Precharge command is being applied. Bank address also determines if the Mode Register or Extended Mode Register is to be accessed during a MRS or EMRS cycle.

**Pin Description Table (Contd.)**

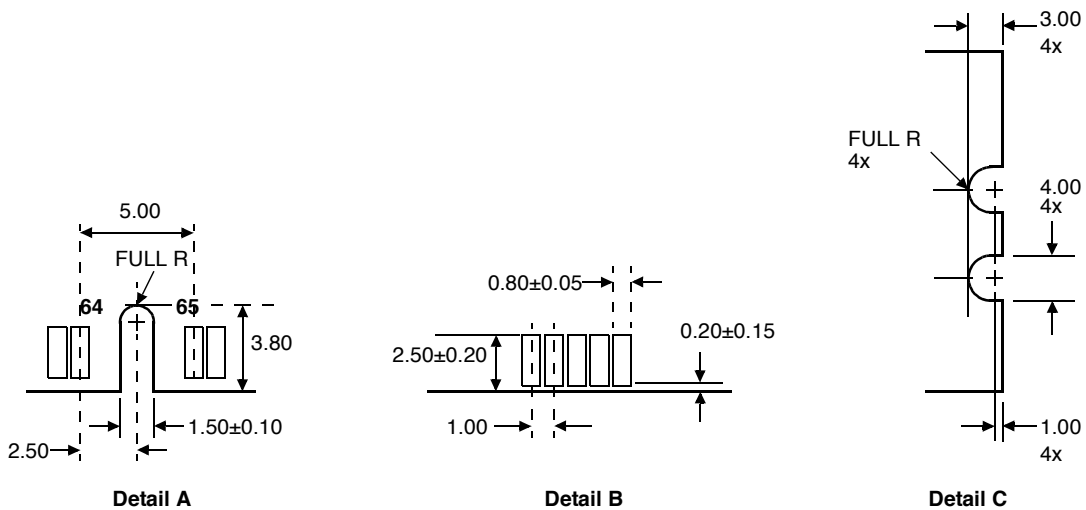
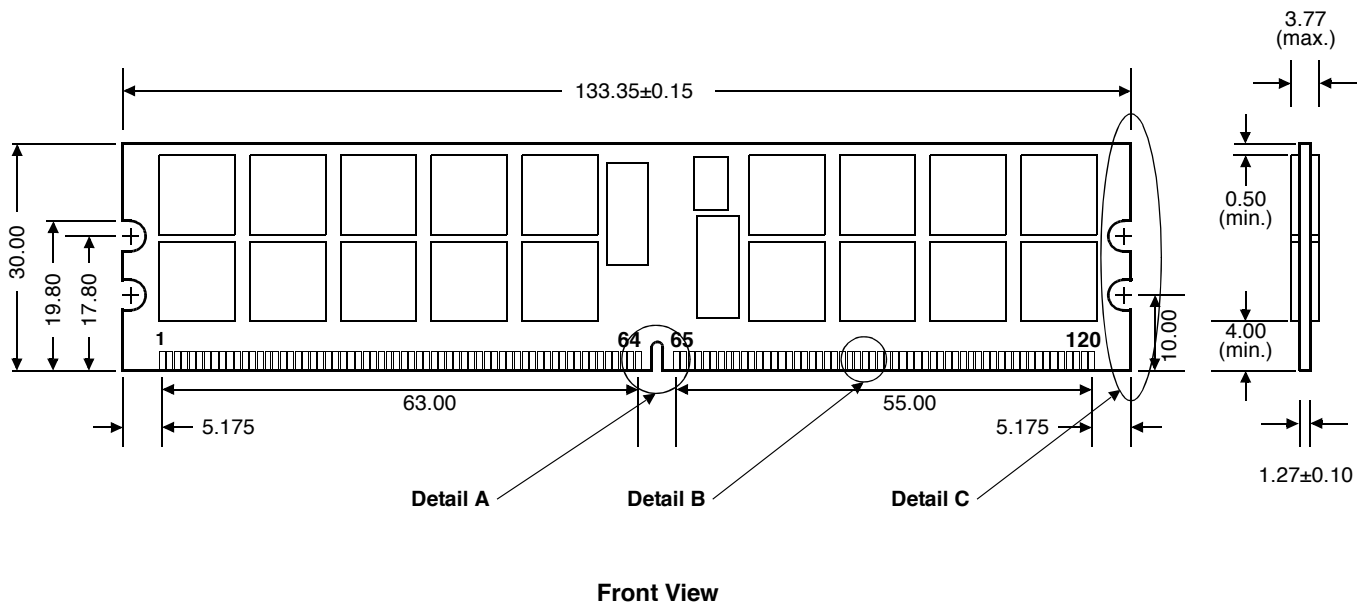
Symbol	Type	Polarity	Function
A0~A9, A10/AP, A11~A13	SSTL_18	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA9, CA11) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be pre-charged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to pre-charge. The address inputs also provide the op-code during Mode Register Set commands.
DQ0~DQ63 CB0~CB7	SSTL_18	-	Data and Check Bit Input/Output pins.
DQS0~DQS17	SSTL_18	Positive Edge	SDRAM differential data strobe for input and output data.
DQS0#~DQS17#	SSTL_18	Negative Edge	SDRAM differential data strobe for input and output data.
SA0~SA2	LVTTTL	-	Slave Address Select for EEPROM. These pins are used to configure the presence-detect device.
SDA	LVTTTL	-	Serial Bus Data Line for EEPROM. SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. A resistor must be connected from the SDA bus line to V <sub>DD</sub> to act as pull up on the system board.
SCL	LVTTTL	-	Serial Bus Clock for EEPROM. SCL is used to synchronize the presence-detect data transfer to and from the module. A resistor may be connected from the SCL bus line to V <sub>DD</sub> to act as pull up on the system board.
RESET#	LV-CMOS	Active Low	Register and PLL control pin. When low, all register outputs will be driven low and the PLL clocks to the DRAM and register will be set to low levels (the PLL will remain synchronized with the input clock, if within spec range).
V <sub>DD</sub>	Supply	-	SDRAM positive power supply. 1.8V±0.1V
V <sub>SS</sub>	Supply	-	Power supply return (ground).
V <sub>REF</sub>	Supply	-	SDRAM I/O reference supply.
V <sub>DDQ</sub>	Supply	-	SDRAM I/O Driver positive power supply. 1.8V±0.1V
V <sub>DDSPD</sub>	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports operation from 1.7V to 3.6V).
NC	-	-	No Connect.
DU	-	-	Do not use.

**Block Diagram**


Note: Unless otherwise noted, data resistor values are  $22\Omega \pm 5\%$ .


**Notes:**

1. Data bits may be swapped within a device. However, DQ/DQS relationship is maintained as shown.
2. Only one PLL output is shown above. Any additional PLL outputs will be wired in a similar manner.
3. DM pin of all SDRAM devices is tied to V<sub>SS</sub>.

**Physical Dimensions**
240-pin DIMM Module


(All dimensions are in millimeters with  $\pm 0.15$ mm tolerance unless specified otherwise.)



**Serial Presence Detect Table (SG2567RDR212435IB/NB/SE)**

Byte No.	Byte Description	Value Supported	Value in Hex
0	# of bytes written into serial memory at module manufacturer	128 Bytes	80h
1	Total # of bytes of SPD memory device	256 Bytes	08h
2	Fundamental memory type	SDRAM DDR2	08h
3	# of row address on this assembly	14	0Eh
4	# of column address on this assembly	11	0Bh
5	# of Ranks, Package and Height	2, Planar, 30.00mm	61h
6	Data width of this assembly	72	48h
7	Reserved	-	00h
8	Voltage interface standard of this assembly	SSTL_18	05h
9	SDRAM cycle time from clock @ CAS latency of 4.0	5.0ns	50h
10	SDRAM access time from clock @ CAS latency of 4.0	0.60ns	60h
11	DIMM configuration type	ECC	02h
12	Refresh rate & type	SR, 7.8	82h
13	Primary SDRAM width	4	04h
14	Error checking SDRAM width	4	04h
15	Reserved	-	00h
16	SDRAM device attributes : Burst lengths supported	4, 8	0Ch
17	SDRAM device attributes : # of banks on SDRAM device	4	04h
18	SDRAM device attributes : CAS latency	3.0, 4.0	18h
19	DIMM mechanical characteristics	3.77mm	01h
20	DIMM type information	RDIMM	01h
21	SDRAM module attributes	1 PLL, 4 Reg	07h
22	SDRAM device attributes : General	Weak Driver	01h
23	SDRAM cycle time from clock @ CAS latency of 3.0	5.0ns	50h
24	SDRAM access time from clock @ CAS latency of 3.0	0.60ns	60h
23	SDRAM cycle time from clock @ CAS latency of 2.0	-	00h
24	SDRAM access time from clock @ CAS latency of 2.0	-	00h

**Serial Presence Detect Table (Contd.)**

Byte No.	Byte Description	Value Supported	Value in Hex
27	Minimum row precharge time (=tRP)	15ns	3Ch
28	Minimum row active to row active delay (=tRRD)	7.5ns	1Eh
29	Minimum RAS to CAS delay (=tRCD)	15ns	3Ch
30	Minimum activate precharge time (=tRAS)	40ns	28h
31	Module row density	1GB	01h
32	Command and Address signal input setup time	0.35ns	35h
33	Command and Address signal input hold time	0.47ns	47h
34	Data signal input setup time	0.15ns	15h
35	Data signal input hold time	0.27ns	27h
36	Write recovery time (=tWR)	15ns	3Ch
37	Internal write to read command delay (=tWTR)	10.0ns	28h
38	Internal read to precharge delay (=tRTP)	7.5ns	1Eh
39	Memory Analysis Probe Characteristics	-	00h
40	Extension of tRC and tRFC	-	00h
41	Device Minimum activate/auto-refresh time (=tRC)	55ns	37h
42	Device Minimum auto-refresh to active/auto-refresh time (=tRFC)	105ns	7Fh
43	Maximum device cycle time (=tCK max)	8ns	80h
44	Device DQS-DQ skew for DQS and associated DQ signals (=tDQSQ max)	0.35ns	23h
45	Device read data hold skew factor (=tQHS)	0.45ns	2Dh
46	PLL relock time	15 $\mu$ s	0Fh
47~61	Reserved	-	00h
62	SPD data revision code	1.2	12h
63	Checksum for bytes 0~62		FFh
64	Manufacturer JEDEC ID code	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	SMART's ID	94h
66~71	.....Manufacturer JEDEC ID code	Not Used	00h
72	Manufacturing location	See Note 1	01h

**Serial Presence Detect Table (Contd.)**

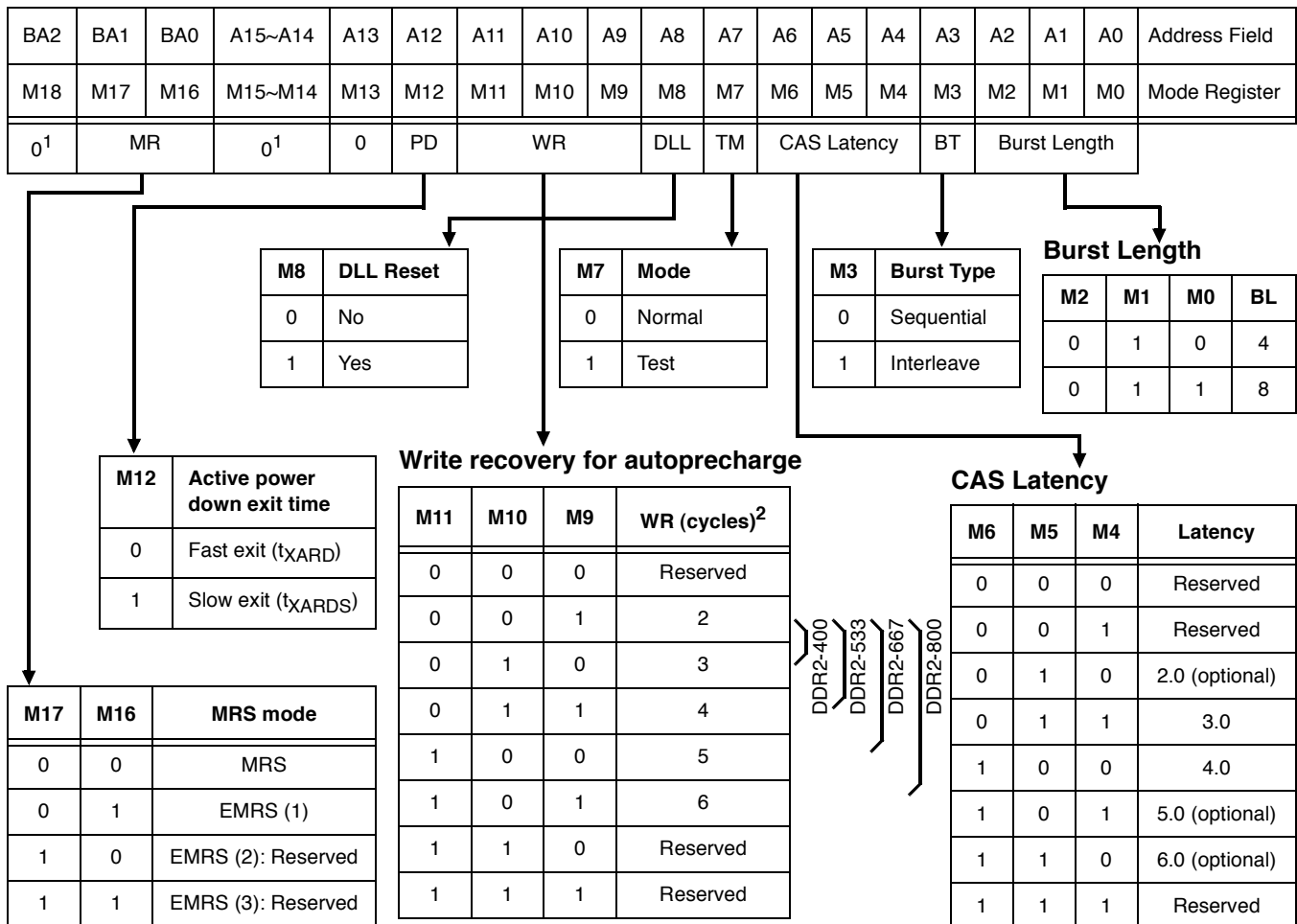
Byte No.	Byte Description	Value Supported	Value in Hex
73~90	Manufacturer part #	SG2567RDR212435UU	P. No
91	Manufacturer revision code	Rev. 0	00h
92	.....Manufacturer revision code	None	00h
93	Manufacturing data (Year)	Date	Date
94	Manufacturing data (Week)	Date	Date
95~98	Assembly serial #	Serial Number	S. No
99~125	Manufacturer specific data	SMART Modular Technologies	
126~127	Unused storage locations	-	00h
128~255	Unused storage locations	-	00h

**Note:**

- Manufacturing Location:
  - 00h - Undefined,
  - 01h - Fremont, USA,
  - 02h - Aguada, Puerto Rico,
  - 03h - East Kilbride, Scotland,
  - 04h - Penang, Malaysia,
  - 05h - Bangalore, India,
  - 06h - Sao Paulo, Brazil,
  - 07h - Aguadilla, Puerto Rico,
  - 08h - Mayaguez, Puerto Rico,
  - 09h - Santo Domingo, Dominican Republic,
  - 0Ah - Dongguan, China,

**Mode Register Table Definition**

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset,  $t_{WR}$  and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0 and BA1, while controlling the state of address pins A0~A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time ( $t_{MRD}$ ) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0~A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4~A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time  $t_{WR}$  is defined by A9~A11.


**Notes:**

- BA2 and A14~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
- WR min is determined by  $t_{CK}$  max and WR max is determined by  $t_{CK}$  min. WR in clock cycles is calculated by dividing  $t_{WR}$  (in ns) by  $t_{CK}$  (in ns) and rounding up to the next integer. The mode register must be programmed to this value.

### Extended Mode Register Table Definition

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT ( $R_{TT}$ ), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT enable/disable. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

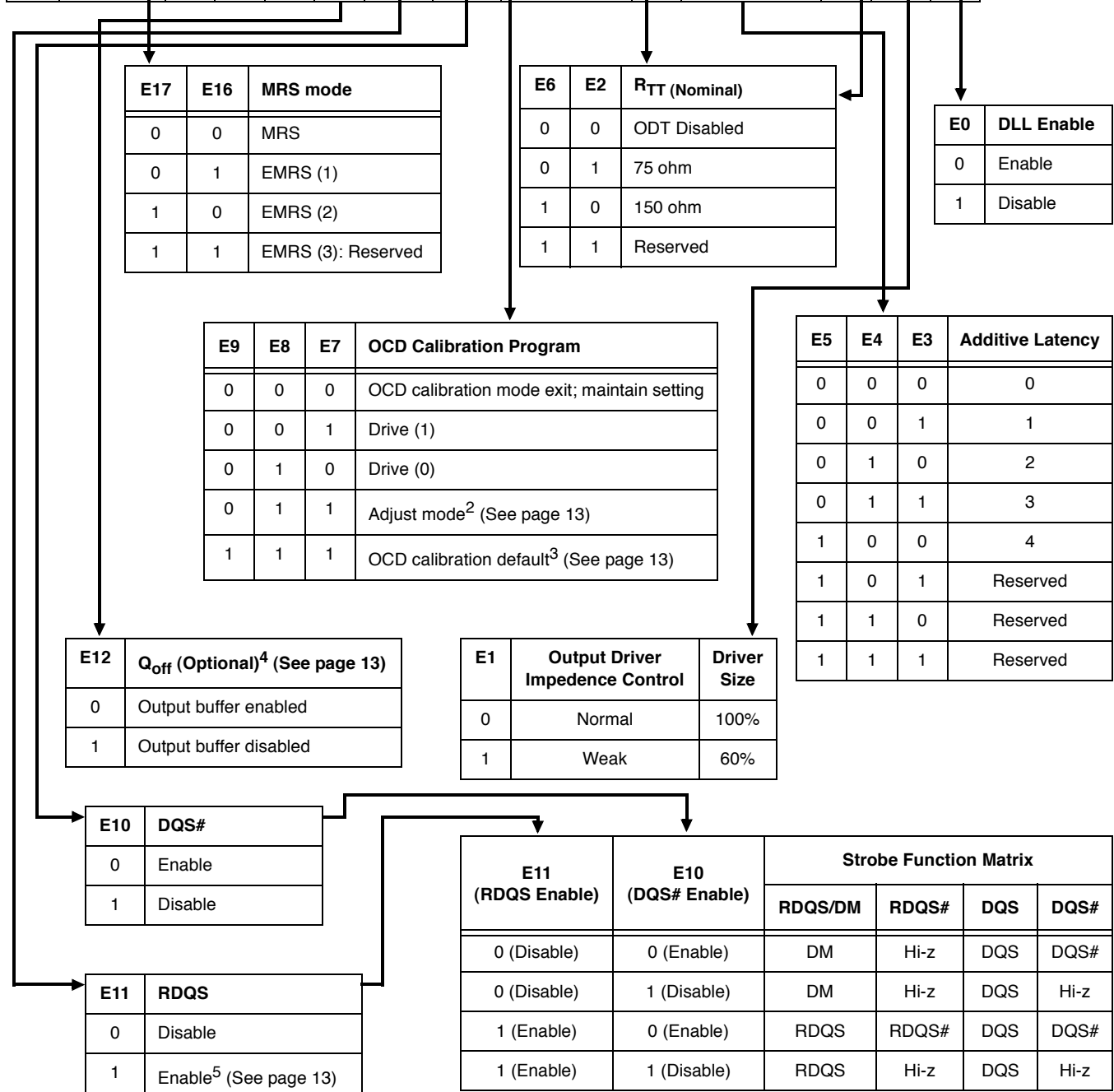
The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time  $t_{MRD}$  before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

#### Notes:

1. BA2 and A14~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. When the adjust mode of the OCD Calibration Program is issued, AL from previously set value must be applied.
3. After setting the OCD Calibration Program to default, OCD mode needs to be exited by setting A9-A7 to 000.
4. Outputs disabled - DQs, DQSs, DQS#s, RDQSs, RDQS#s. This feature is used in conjunction with DIMM  $I_{DDQ}$  measurements when  $I_{DDQ}$  is not desired to be included.
5. If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.

**Extended Mode Register Table**

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	Extended Mode Register
0 <sup>1</sup>	EMR		0 <sup>1</sup>	0 <sup>1</sup>	0	Q <sub>off</sub>	RDQS	DQS#	OCD Program			R <sub>TT</sub>	Additive latency			R <sub>TT</sub>	D.I.C	DLL	



**Commands**

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

Truth Table - Commands

Function	CKE		CS#	RAS#	CAS#	WE#	BA0~ BA <sub>n</sub> <sup>9</sup>	An <sup>8</sup> ~A11	A10	A9~A0	Notes
	Previous cycle	Current cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Refresh	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1, 7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge All Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	Column	L	Column	1, 2, 3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1, 2, 3
Read	H	H	L	H	L	H	BA	Column	L	Column	1, 2, 3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1, 2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					

**Notes:**

- All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock.
- Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
- Burst reads or writes at BL=4 cannot be terminated or interrupted.
- The Power Down Mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- "X" means "H or L (but a defined logic level)".
- Self Refresh Exit is asynchronous.
- An = A12 for 256Mb, A13 for 512Mb & 1 Gb, A14 for 2Gb.
- BA<sub>n</sub> = BA1 for up to 512Mb, BA2 for 1 Gb & 2Gb.

## DC Characteristics

### Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Notes
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	-1.0 ~ 2.3	V	
Voltage on $V_{DDQ}$ relative to $V_{SS}$	$V_{DDQ}$	-0.5 ~ 2.3	V	
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 ~ 2.3	V	
Voltage on $V_{DDSPD}$ relative to $V_{SS}$	$V_{DDSPD}$	1.7 ~ 3.6	V	
Operating Temperature (Ambient)	$T_{OPR}$	0 to +65	°C	
Operating Temperature (Case)	$T_{CASE}$	0 to +85	°C	1, 2
Storage Temperature	$T_{STG}$	-55 to +100	°C	

#### Notes:

- It is possible to operate the DRAM above Case Temperature up to 95°C.
- Above 85°C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9\mu s$ .

### Recommended DC Operating Conditions ( $T_A = 0$ to +65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V	
I/O Supply Voltage	$V_{DDQ}$	1.7	1.8	1.9	V	
I/O Reference Voltage	$V_{REF}$	$0.49 \cdot V_{DDQ}$	$0.50 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	mV	1, 2
I/O Termination Voltage	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V	3
SPD Voltage	$V_{DDSPD}$	1.7	-	3.6	V	
Input High Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$	-	$V_{DDQ} + 0.3$	V	
Input Low Voltage	$V_{IL(DC)}$	-0.3	-	$V_{REF} - 0.125$	V	
Input Voltage Level, CK/CK#	$V_{IN(DC)}$	-0.3	-	$V_{DDQ} + 0.3$	V	
Input Differential Voltage, CK/CK#	$V_{ID(DC)}$	0.25	-	$V_{DDQ} + 0.6$	V	
Ground	$V_{SS}$	0	0	0	V	

#### Notes:

- $V_{REF}$  is expected to track variation in  $V_{DDQ}$ .
- Peak to peak noise (non-common mode) on  $V_{REF}$  may not exceed  $\pm 1\%$  of the DC value. Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\%$  of  $V_{REF}$  (DC). This measurement is to be taken at the nearest  $V_{REF}$  bypass capacitor.
- $V_{TT}$  is not used on the module. It is the voltage used on the system board to terminate all the signals. However, this supply should track the variations in DC level of  $V_{REF}$ .



**Capacitance**
**( $V_{DD} = 1.8V \pm 0.1V$ ,  $T_{Case} = +25^{\circ}C$ )**

Parameter	Symbol	Min	Max	Unit
Input Capacitance (CKn, CKn#)	$C_{CK}$	2.0	3.0	pF
Input Capacitance delta (CKn, CKn#)	$C_{DCK}$	-	-	pF
Input Capacitance (all other input-only pins)	$C_I$	5.0	7.0	pF
Input Capacitance delta (all other input-only pins)	$C_{DI}$	-	-	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#, CB)	$C_{IO}$	5.0	8.0	pF
Input/Output Capacitance delta (DQ, DM, DQS, DQS#, CB)	$C_{DIO}$	-	1.0	pF

**AC Operating Conditions**
**( $V_{DD} = 1.8V \pm 0.1V$ ,  $V_{SS} = 0V$ )**

Parameter	Symbol	Min	Max	Unit	Notes
Input High Logic Voltage	$V_{IH(AC)}$	$V_{REF} + 0.250$	-	V	1, 2
Input Low Logic Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.250$	V	1, 2
Input differential voltage, CK and CK# inputs	$V_{ID(AC)}$	0.5	$V_{DDQ} + 0.6$	V	1, 2, 3
Input crossing point voltage, CK and CK# inputs	$V_{IX(AC)}$	$0.5 * V_{DDQ} - 0.175$	$0.5 * V_{DDQ} + 0.175$	V	1, 2, 3
AC differential crossing point voltage	$V_{OX(AC)}$	$0.5 * V_{DDQ} - 0.125$	$0.5 * V_{DDQ} + 0.125$	V	3

**Notes:**

1. Input slew rate is 1V/ns.
2. Inputs are not recognized as valid until  $V_{REF}$  stabilizes.
3.  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The value of  $V_{IX}/V_{OX}$  is expected to equal  $0.5 * V_{DDQ}$  of the transmitting device and must track variations in the DC level of the same.

**ODT DC Electrical Characteristics**

Parameter	Symbol	Min	Nom	Max	Unit	Notes
R <sub>TT</sub> effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	R <sub>TT1(EFF)</sub>	60	75	90	Ω	1
R <sub>TT</sub> effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	R <sub>TT2(EFF)</sub>	120	150	180	Ω	1
Deviation of VM with respect to V <sub>DDQ</sub> /2	ΔVM	-6		+6	%	2

**Notes:**

- R<sub>TT1(EFF)</sub> and R<sub>TT2(EFF)</sub> are determined by applying V<sub>IH(AC)</sub> and V<sub>IL(AC)</sub> to pin under test separately, then

$$\text{measure current } I(V_{IH(AC)}) \text{ and } I(V_{IL(AC)}) \text{ respectively. } R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

- Measured voltage (VM) at tested pin with no load.

$$\Delta VM = \left( \frac{2 \times VM}{V_{DDQ}} - 1 \right) \times 100 \%$$

**Output DC Current Drive**

Parameter	Symbol	Min	Max	Unit	Notes
Output Minimum Source DC Current	I <sub>OH</sub>	-13.4	-	mA	1, 3, 4
Output Minimum Sink DC Current	I <sub>OL</sub>	13.4	-	mA	2, 3, 4

**Notes:**

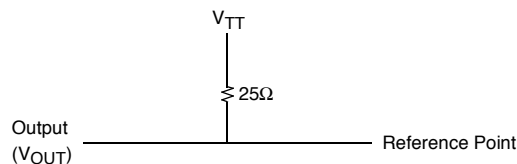
- For I<sub>OH</sub> (DC); V<sub>DDQ</sub> = 1.7V, V<sub>OUT</sub> = 1420mV. (V<sub>OUT</sub> - V<sub>DDQ</sub>)/I<sub>OH</sub> must be less than 21Ω for values of V<sub>OUT</sub> between V<sub>DDQ</sub> and V<sub>DDQ</sub> - 280mV.
- For I<sub>OL</sub> (DC); V<sub>DDQ</sub> = 1.7V, V<sub>OUT</sub> = 280mV. V<sub>OUT</sub>/I<sub>OL</sub> must be less than 21Ω for values of V<sub>OUT</sub> between 0V and 280mV.
- The DC value of V<sub>REF</sub> applied to the receiving device is set to V<sub>TT</sub>.
- The values of I<sub>OH</sub> (DC) and I<sub>OL</sub> (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V<sub>IH</sub> min plus a noise margin and V<sub>IL</sub> max minus a noise margin are delivered to an SSTL\_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21Ω load line to define a convenient driver current for measurement.

**OCD Default Output Characteristics**  
 ( $V_{DD} = 1.8V \pm 0.1V$ ,  $V_{SS} = 0V$ ,  $T_A = 0$  to  $+65^\circ C$ )

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Output Impedance		12.6	18	23.4	$\Omega$	1, 2
Pull-up and Pull-down mismatch		0		4	$\Omega$	1, 2, 3
Output Slew Rate	$S_{OUT}$	1.5		5	V/ns	1, 4, 5, 7
Output Step Size for Calibration		0		1.5	$\Omega$	6

**Notes:**

1. Absolute specifications:  $0^\circ C \leq T_{case} \leq +85^\circ C$ ;  $V_{DDQ} = +1.8V \pm 0.1V$ ,  $V_{DD} = +1.8V \pm 0.1V$ .
2. Impedance measurement condition for output source DC current:  $V_{DDQ} = 1.7V$ ;  $V_{OUT} = 1420mV$ ;  $(V_{OUT} - V_{DDQ})/I_{OH}$  must be less than  $23.4\Omega$  for values of  $V_{OUT}$  between  $V_{DDQ}$  and  $V_{DDQ} - 280mV$ . Impedance measurement condition for output sink DC current:  $V_{DDQ} = 1.7V$ ;  $V_{OUT} = 280mV$ ;  $V_{OUT}/I_{OL}$  must be less than  $23.4\Omega$  for values of  $V_{OUT}$  between  $0V$  and  $280mV$ .
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between  $V_{TT} - 250mV$  and  $V_{TT} + 250mV$  for single ended signals. For differential signals output slew rate is measured between  $DQS - DQS\# = -500mV$  and  $DQS\# - DQS = +500mV$ . Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from  $V_{IL}$  (DC) max to  $V_{IH}$  (DC) min is equal to or greater than the slew rate as measured from  $V_{IL}$  (AC) max to  $V_{IH}$  (AC) min. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near  $18\Omega$  at nominal conditions across all process and represent only the DRAM uncertainty.
7. Timing skew due to DRAM output slew rate mis-match between  $DQS/DQS\#$  and associated  $DQs$  is included in  $t_{DQSQ}$  and  $t_{QHS}$  specification.

**Output Slew Rate Load Diagram**


**IDD Specification Parameters and Test Conditions**  
**(V<sub>DD</sub> = 1.8V±0.1V, V<sub>SS</sub> = 0V, T<sub>A</sub> = 0 to +65°C)**

Symbol	Parameter	5.0ns CL 3.0	Unit
IDD0	<b>Operating one bank active–precharge current;</b> t <sub>CK</sub> = t <sub>CK(IDD)</sub> , t <sub>RC</sub> = t <sub>RC(IDD)</sub> , t <sub>RAS</sub> = t <sub>RASmin(IDD)</sub> ; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	4060	mA
IDD1	<b>Operating one bank active–read–precharge current;</b> I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK(IDD)</sub> , t <sub>RC</sub> = t <sub>RC(IDD)</sub> , t <sub>RAS</sub> = t <sub>RASmin(IDD)</sub> , t <sub>RCD</sub> = t <sub>RCD(IDD)</sub> ; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	4330	mA
IDD2P	<b>Precharge power–down current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK(IDD)</sub> ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	2188	mA
IDD2Q	<b>Precharge quiet standby current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK(IDD)</sub> ; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	2980	mA
IDD2N	<b>Precharge standby current;</b> All banks idle; t <sub>CK</sub> = t <sub>CK(IDD)</sub> ; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	3160	mA
IDD3P	<b>Active power–down current;</b> All banks open; t <sub>CK</sub> = t <sub>CK(IDD)</sub> ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	3340 mA
		Slow PDN Exit MRS(12) = 1	3016 mA
IDD3N	<b>Active standby current;</b> All banks open; t <sub>CK</sub> = t <sub>CK(IDD)</sub> , t <sub>RAS</sub> = t <sub>RASmax(IDD)</sub> , t <sub>RP</sub> = t <sub>RP(IDD)</sub> ; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	3700	mA
IDD4W	<b>Operating burst write current;</b> All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK(IDD)</sub> , t <sub>RAS</sub> = t <sub>RASmax(IDD)</sub> , t <sub>RP</sub> = t <sub>RP(IDD)</sub> ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	4240	mA
IDD4R	<b>Operating burst read current;</b> All banks open, Continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = 0; t <sub>CK</sub> = t <sub>CK(IDD)</sub> , t <sub>RAS</sub> = t <sub>RASmax(IDD)</sub> , t <sub>RP</sub> = t <sub>RP(IDD)</sub> ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	4420	mA
IDD5B	<b>Burst refresh current;</b> t <sub>CK</sub> = t <sub>CK(IDD)</sub> ; Refresh command at every t <sub>RFC(IDD)</sub> interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	4690	mA
IDD6	<b>Self refresh current;</b> CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	288	mA
IDD7	<b>Operating bank interleave read current;</b> All bank interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(IDD), AL = t <sub>RCD(IDD)</sub> –1*t <sub>CK(IDD)</sub> ; t <sub>CK</sub> = t <sub>CK(IDD)</sub> , t <sub>RC</sub> = t <sub>RC(IDD)</sub> , t <sub>RRD</sub> = t <sub>RRD(IDD)</sub> , t <sub>RCD</sub> = 1*t <sub>CK(IDD)</sub> ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R	6040	mA

**IDD Specification Parameters and Test Conditions (Contd.)**
**Notes:**

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#. IDD values must be met with all combinations of ERMS bits 10 and 11.
5. Definitions for IDD
  - LOW =  $V_{in} \leq V_{IL(AC)}(\max)$
  - HIGH =  $V_{in} \geq V_{IH(AC)}(\min)$
  - STABLE = inputs stable at a HIGH or LOW level
  - FLOATING = inputs at  $V_{REF} = V_{DDQ}/2$
  - SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks of strobes.

**IDD Testing Parameters**

Parameter	DDR2-400	Units
	3-3-3	
CL(IDD)	3	t <sub>CK</sub>
t <sub>RCD</sub> (IDD)	15	ns
t <sub>RC</sub> (IDD)	55	ns
t <sub>RRD</sub> (IDD)	7.5	ns
t <sub>CK</sub> (IDD)	5	ns
t <sub>RASmin</sub> (IDD)	40	ns
t <sub>RASmax</sub> (IDD)	70000	ns
t <sub>RP</sub> (IDD)	15	ns
t <sub>RFC</sub> (IDD)	105	ns

### Device AC Operating Conditions

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400		Unit	Notes	
		Min	Max			
Clock cycle time	CL=4.0	t <sub>CK</sub>	5000	8000	ps	12, 20
	CL=3.0		5000	8000	ps	12, 20
Clock high-level width	t <sub>CH</sub>	0.45	0.55	t <sub>CK</sub>	14	
Clock low-level width	t <sub>CL</sub>	0.45	0.55	t <sub>CK</sub>	14	
Clock half period	t <sub>HP</sub>	Min (t <sub>CL</sub> , t <sub>CH</sub> )	-	ps	15	
DQ output access time from CK/CK#	t <sub>AC</sub>	-600	+600	ps		
Data-out high-impedence window from CK/CK#	t <sub>HZ</sub>	-	t <sub>AC</sub> (max)	ps	4, 5	
Data-out low-impedence window from CK/CK#	t <sub>LZ</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	ps	4, 6	
DQ & DM input setup time relative to DQS	t <sub>DS</sub>	150	-	ps	3, 11, 17	
DQ & DM input hold time relative to DQS	t <sub>DH</sub>	275	-	ps	3, 11, 17	
DQ & DM input pulse width (for each input)	t <sub>DIPW</sub>	0.35	-	t <sub>CK</sub>		
Data hold skew factor	t <sub>QHS</sub>	-	450	ps		
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t <sub>QH</sub>	t <sub>HP</sub> - t <sub>QHS</sub>	-	ps	11,13	
DQS input high pulse width	t <sub>DQSH</sub>	0.35	-	t <sub>CK</sub>		
DQS input low pulse width	t <sub>DQSL</sub>	0.35	-	t <sub>CK</sub>		
DQS output access time from CK/CK#	t <sub>DQSSCK</sub>	-500	+500	ps		
DQS falling edge to CK rising - setup time	t <sub>DSS</sub>	0.2	-	t <sub>CK</sub>		
DQS falling edge from CK rising - hold time	t <sub>DSH</sub>	0.2	-	t <sub>CK</sub>		
DQS-DQ skew, DQS to last DQ valid, per group, per access	t <sub>DQSQ</sub>	-	350	ps	11,13	
DQS read preamble	t <sub>RPRE</sub>	0.9	1.1	t <sub>CK</sub>	18	
DQS read postamble	t <sub>RPST</sub>	0.4	0.6	t <sub>CK</sub>		
DQS write preamble setup time	t <sub>WPRES</sub>	0	-	ps	8, 9	
DQS write preamble	t <sub>WPRE</sub>	0.25	-	t <sub>CK</sub>		
DQS write postamble	t <sub>WPST</sub>	0.4	0.6	t <sub>CK</sub>	7	
Write command to first DQS latching transition	t <sub>DQSS</sub>	WL - 0.25	WL + 0.25	t <sub>CK</sub>		
Address & control input pulse width for each input	t <sub>IPW</sub>	0.6	-	t <sub>CK</sub>		
Address and control input setup time	t <sub>IS</sub>	350	-	ps	2, 17	
Address and control input hold time	t <sub>IH</sub>	475	-	ps	2, 17	
CAS# to CAS# command delay	t <sub>CCD</sub>	2	-	t <sub>CK</sub>		
OCD Drive mode delay	t <sub>OIT</sub>	0	12	ns		
CKE low to CK,CK# uncertainty	t <sub>DELAY</sub>	5.825	5.825	ns	24	

**Device AC Operating Conditions (Contd.)**

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400		Unit	Notes
		Min	Max		
ACTIVE to ACTIVE (same bank) command	t <sub>RC</sub>	55	-	ns	
ACTIVE bank a to ACTIVE bank b command	t <sub>RRD</sub>	7.5	-	ns	23
ACTIVE to READ or WRITE delay	t <sub>RCD</sub>	15	-	ns	
ACTIVE to PRECHARGE command	t <sub>RAS</sub>	40	70000	ns	16
Internal READ to precharge command delay	t <sub>RTP</sub>	7.5	-	ns	19, 23
Write recovery time	t <sub>WR</sub>	15	-	ns	23
Auto precharge write recovery + Precharge time	t <sub>DAL</sub>	t <sub>WR</sub> + t <sub>RP</sub>	-	t <sub>CK</sub>	18
Internal WRITE to READ command delay	t <sub>WTR</sub>	10	-	ns	23
PRECHARGE command period	t <sub>RP</sub>	15	-	ns	
LOAD MODE command cycle time	t <sub>MRD</sub>	2	-	t <sub>CK</sub>	
REFRESH to REFRESH command interval	t <sub>RFC</sub>	105	-	ns	10
Average periodic refresh Interval	t <sub>REFI</sub>	-	7.8	μs	10
Exit self refresh to non-READ command	t <sub>XSNR</sub>	t <sub>RFC</sub> (min) + 10	-	ns	
Exit self refresh to READ command	t <sub>XSRD</sub>	200	-	t <sub>CK</sub>	
ODT turn-on delay	t <sub>AOND</sub>	2	2	t <sub>CK</sub>	
ODT turn-on	t <sub>AON</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 1000	ps	21
ODT turn-off delay	t <sub>AOFD</sub>	2.5	2.5	t <sub>CK</sub>	
ODT turn-off	t <sub>AOF</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	ps	22
ODT turn-on (power-down mode)	t <sub>AONPD</sub>	t <sub>AC</sub> (min) + 2000	2*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	ps	
ODT turn-off (power-down mode)	t <sub>AOFPD</sub>	t <sub>AC</sub> (min) + 2000	2.5*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	ps	
ODT to power-down entry latency	t <sub>ANPD</sub>	3		t <sub>CK</sub>	
ODT power-down exit latency	t <sub>AXPD</sub>	8		t <sub>CK</sub>	
Exit active power-down to READ command, MR[bit12=0]	t <sub>XARD</sub>	2	-	t <sub>CK</sub>	
Exit active power-down to READ command, MR[bit12=1]	t <sub>XARDS</sub>	6 - AL	-	t <sub>CK</sub>	
Exit precharge power down to any non-read command	t <sub>XP</sub>	2	-	t <sub>CK</sub>	
CKE minimum pulse width (high and low pulse width)	t <sub>CKE</sub>	3	-	t <sub>CK</sub>	

**Notes:**

1. The AC and DC input level specifications are as defined in the SSTL\_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level.
2. Command/Address minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of CK/CK#.  $t_{1S}$  timing is referenced to  $V_{IH(AC)}$  for a rising signal and  $V_{IL(AC)}$  for a falling signal.  $t_{1H}$  timing is referenced to  $V_{IH(DC)}$  for a rising signal and  $V_{IL(DC)}$  for a falling signal. Derating values for Command/Address input signal slew rates < 1.0V/ns are TBD.
3. Data minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of DQS/DQS# if differential strobe feature is enabled.  $t_{DS}$  timing is referenced to  $V_{IH(AC)}$  for a rising signal and  $V_{IL(AC)}$  for a falling signal.  $t_{DH}$  timing is referenced to  $V_{IH(DC)}$  for a rising signal and  $V_{IL(DC)}$  for a falling signal. Derating values for Data input signal slew rates < 1.0V/ns are TBD.
4.  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving ( $t_{HZ}$ ) or begins driving ( $t_{LZ}$ ).
5. This maximum value is derived from the reference test load.  $t_{HZ(MAX)}$  will prevail over a  $t_{DQSCK(MAX)} + t_{RPST(MAX)}$  condition.
6.  $t_{LZ(MIN)}$  will prevail over a  $t_{DQSCK(MIN)} + t_{RPST(MAX)}$  condition.
7. The intent of the Don't Care state after completion of the postamble is the DQS driven signal should be high, low or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high [above  $V_{IH(DC(MIN))}$ ] then it must not transition low (below  $V_{IH(DC)}$ ) prior to  $t_{DQSH(min)}$ .
8. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
9. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during his time depending on  $t_{DQSS}$ .
10. The refresh period is 64ms. This equates to an average refresh rate of 7.8125 $\mu$ s. However, an REFRESH command must be asserted at least once every 70.3 $\mu$ s or  $t_{RFC(MAX)}$ ; issuing more than eight REFRESH commands back to back at  $t_{RFC(min)}$  is not allowed.
11. Each byte lane has a corresponding DQS.
12. CK and CK# input slew rate must be  $\geq 1$  V/ns ( $\geq 2$  V/ns if measured differentially).
13. The data valid window is derived by achieving other specifications:  $t_{HP}$ , ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
14. MIN ( $t_{CL}$ ,  $t_{CH}$ ) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for  $t_{CL}$  and  $t_{CH}$ ).
15.  $t_{HP(MIN)}$  is the lesser of  $t_{CL}$  minimum and  $t_{CH}$  minimum actually applied to the device CK and CK# inputs.
16. READs and WRITEs with no auto precharge are allowed to be issued before  $t_{RAS(MIN)}$  is satisfied since  $t_{RAS}$  lockout feature is supported in DDR2 SDRAM.
17.  $V_{IL}/V_{IH}$  DDR2 overshoot/undershoot. Refer to 256MB, 512MB, or 1GB DDR2 SDRAM component data sheet for more detailed information.
18.  $t_{DAL} = (n_{WR}) + (t_{RP}/t_{CK})$ : For each of the terms above, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period;  $n_{WR}$  refers to the  $t_{WR}$  parameter stored in the MR[11,10,9].
19. This is a minimum requirement. Minimum READ to internal PRECHARGE timing is AL + BL/2 providing the  $t_{RTP}$  and  $t_{RAS(MIN)}$  have been satisfied. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until  $t_{RAS(MIN)}$  has been satisfied.
20. Operating frequency is only allowed to change during self refresh mode or precharge power-down mode. Anytime the operating frequency is changed, not including jitter, the DLL is required to be reset followed by 200 clock cycles.
21. ODT turn-on time  $t_{AON(MIN)}$  is when the device leaves high impedance and ODT resistance begins to turn-on. ODT turn-on time  $t_{AON(MAX)}$  is when the resistance is fully on. Both are measured from  $t_{AOND}$ .
22. ODT turn-off time  $t_{AOF(MIN)}$  is when the device starts to turn-off ODT resistance. ODT turn-off time  $t_{AOF(MAX)}$  is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .
23. This parameter has a two clock minimum requirement at any  $t_{CK}$ .
24.  $t_{DELAY}$  is calculated from  $t_{1S} + t_{CK} + t_{1H}$  so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system reset condition.



**Part Number Decode**

<u>S</u>	<u>G</u>	<u>256</u>	<u>7</u>	<u>RDR2</u>	<u>12</u>	<u>4</u>	<u>3</u>	<u>5</u>	<u>U</u>	<u>U</u>
1	2	3	4	5	6	7	8	9	10	11

- 1 SMART Modular Technologies**
- 2 Module Process Technology**  
G: Green Module (RoHS Compliant)
- 3 Module Address Depth**  
256: 256M
- 4 Module Data Bus Width**  
7: x72
- 5 Module Configuration**  
RDR2: DDR2 Registered DIMM
- 6 Device Depth**  
12: 128M
- 7 Device Width**  
4: x4
- 8 CAS Latency**  
3: CL 3.0
- 9 Module Speed**  
5: DDR2-400
- 10 Device Vendor**  
I: Qimonda  
N: Nanya  
S: Samsung
- 11 Device Revision**  
B: Revision B  
E: Revision E

Note : "U" in the part number should be replaced by user specified option.

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