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### 1.0 Features

- Three PLLs with deep reference, feedback, and post dividers to provide precision clock frequencies
- Multiple outputs provide several clocking options
- Outputs may be tristated for board testing
- S0, S1, and S2 inputs modify output frequencies for design flexibility
- 3.3V operation
- Accepts 5 to 30MHz crystals (see Frequency Table for specific reference frequencies required)
- Custom frequency patterns, pinouts, and packages are available. Contact your local AMI Sales Representative for more information.

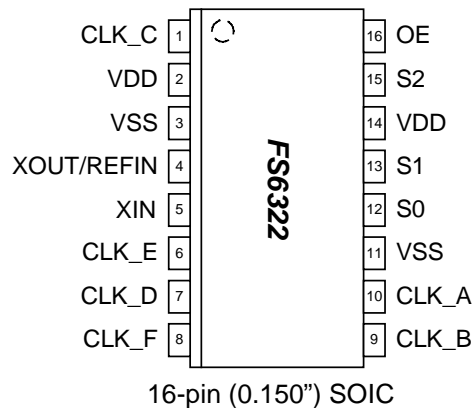
### 2.0 Description

The FS6322 is a ROM-based CMOS clock generator IC designed to minimize cost and component count in a variety of electronic systems.

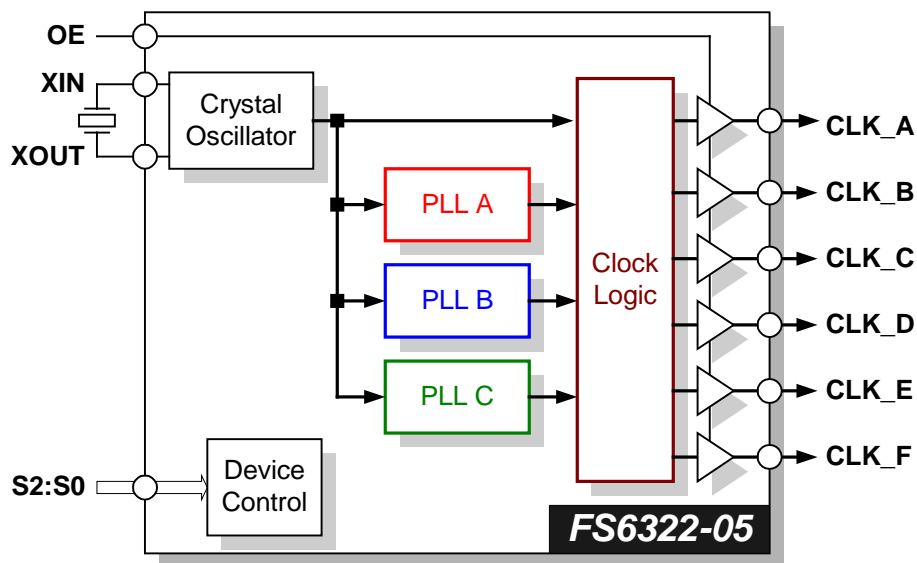
Three low-jitter phase-locked loops (PLLs) drive up to five low-skew clock outputs to provide a high degree of flexibility. The device is packaged in a 16-pin SOIC to minimize board space.

High-resolution divider capability permits generation of desired frequencies.

**Figure 1: Pin Configuration**



**Figure 2: Block Diagram**



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### Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI<sup>U</sup> = Input with Internal Pull-Up; DI<sub>D</sub> = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	DO	CLK_C	C clock output
2	P	VDD	Power supply (3.3V nominal – see version specific information)
3	P	VSS	Ground
4	AI	XOUT / REFIN	Crystal oscillator drive / external reference input
5	AO	XIN	Crystal oscillator feedback
6	DO	CLK_E	E clock output
7	DO	CLK_D	D clock output
8	DO	CLK_F	F clock output
9	DO	CLK_B	A clock output
10	DO	CLK_A	B clock output
11	P	VSS	Ground
12	DI <sup>U</sup>	S0	Frequency select control input
13	DI <sup>U</sup>	S1	Frequency select control input
14	P	VDD	Power supply (5V to 3.3V)
15	DI <sup>U</sup>	S2	Frequency select control input
16	DI <sup>U</sup>	OE	Output enable input: logic-high enables outputs; logic-low tristates outputs (high impedance)

### Table 2: Frequency Table – FS6322-05 (3.3volt) (all frequencies in MHz)

S2	S1	S0	FREF	CLK_A (pin 10)	CLK_B (pin 9)	CLK_C (pin 1)	CLK_D (pin 7)	CLK_E (pin 6)	CLK_F (pin 8)
0	0	0	16.0000	25.00000	10.00000	1.84320	0.00000	0.00000	0.00000
0	0	1	11.0592	24.57600	11.28960	1.84320	33.33336	25.00002	20.00002
0	1	0	13.5000	36.86400	18.43200	16.93440	27.00000	33.86880	54.00000
0	1	1	13.5000	33.86880	16.93440	16.93440	27.00000	33.86880	54.00000
1	0	0	13.5000	33.86880	73.72800	49.15200	27.00000	27.00000	54.00000
1	0	1	13.5000	33.86880	67.73760	45.15840	27.00000	27.00000	54.00000
1	1	0	13.5000	33.86880	49.15200	32.76800	27.00000	27.00000	54.00000
1	1	1	13.5000	33.86880	36.86400	24.57600	27.00000	27.00000	54.00000

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### 3.0 Electrical Specifications

**Table 3: Absolute Maximum Ratings**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc ( $V_{SS} = \text{ground}$ )	$V_{DD}$	$V_{SS}-0.5$	7	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{IK}$	-50	50	mA
Output Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{OK}$	-50	50	mA
Storage Temperature Range (non-condensing)	$T_S$	-65	150	°C
Ambient Temperature Range, Under Bias	$T_A$	-55	125	°C
Junction Temperature	$T_J$		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV



**CAUTION: ELECTROSTATIC SENSITIVE DEVICE**

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

**Table 4: Operating Conditions**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	$V_{DD}$	$3.3V \pm 10\%$	3	3.3	3.6	V
Ambient Operating Temperature Range	$T_A$		0		70	°C
Crystal Resonator Frequency	$f_{XIN}$		5		30	MHz
Output Load Capacitance	$C_L$				20	pF

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**Table 5: DC Electrical Specifications**

Unless otherwise stated,  $V_{DD} = 3.3V \pm 10\%$ , no load on any output, and ambient temperature range  $T_A = 0^\circ C$  to  $70^\circ C$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
<b>Overall</b>						
Supply Current, Dynamic, with Loaded Outputs	$I_{DD}$	$f_{XTAL} = 27MHz$ ; $C_L = 0pF$ , $V_{DD} = 3.3V$ FS6322-05: S[2:0]=[100]		20		mA
<b>Digital Inputs (OE, S2, S0)</b>						
High-Level Input Voltage	$V_{IH}$		2.4		$V_{DD}+0.3$	V
Low-Level Input Voltage	$V_{IL}$		$V_{SS}-0.3$		0.8	V
High-Level Input Current	$I_{IH}$	$V_{IN} = V_{DD}$	-1		1	$\mu A$
Low-Level Input Current (pull-up)	$I_{IL}$	$V_{IN} = 0V$		-8		$\mu A$
<b>Digital Inputs (S1)</b>						
High-Level Input Voltage	$V_{IH}$		2.4		$V_{DD}+0.3$	V
Low-Level Input Voltage	$V_{IL}$		$V_{SS}-0.3$		0.8	V
High-Level Input Current	$I_{IH}$	$V_{IN} = V_{DD}$	-1		1	$\mu A$
Low-Level Input Current (pull-up)	$I_{IL}$	$V_{IN} = 0V$		-16		$\mu A$
<b>Crystal Oscillator</b>						
Crystal Loading Capacitance	$C_{L(xtal)}$	As seen by a crystal connected to XIN and XOUT		16		pF
Crystal Drive Level		$R_{XTAL}=20\Omega$		200		$\mu W$
<b>Clock Outputs (CLKA, CLKB)</b>						
Output Current High	$I_{OH}$	$V_O = 2.4V$	-4			mA
Output Current Low	$I_{OL}$	$V_O = 0.4V$	4			mA
Short Circuit Source Current *	$I_{OSH}$	$V_O = 0V$ ; shorted for 30s, max.		-35		mA
Short Circuit Sink Current *	$I_{OSL}$	$V_O = 3.3V$ ; shorted for 30s, max.		40		mA
Output Impedance *	$Z_{OH}$	$V_O = 0.5V_{DD}$ ; output driving high		45		$\Omega$
	$Z_{OL}$	$V_O = 0.5V_{DD}$ ; output driving low		45		

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**Table 6: AC Timing Specifications**

Unless otherwise stated,  $V_{DD} = 3.3V \pm 10\%$ , no load on any output, and ambient temperature range  $T_A = 0^\circ C$  to  $70^\circ C$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are  $\pm 3\sigma$  from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	CLOCK (MHz)	MIN.	TYP.	MAX.	UNITS
<b>Clock Output (CLK_X)</b>							
Duty Cycle *		Crystal oscillator derived outputs Measured @1.4V; $C_L = 20pF$		43	51	57	%
Duty Cycle *		PLL derived outputs Measured @1.4V; $C_L = 20pF$		45	51	55	%
Rise Time *	$t_r$	$V_O = 0.4V$ to $2.4V$ ; $C_L = 20pF$			2.2		ns
Fall Time *	$t_f$	$V_O = 2.4V$ to $0.4V$ ; $C_L = 20pF$			1.8		ns
Jitter, Period (RMS) *	$t_{j(1\sigma)}$	From rising edge to next rising edge at $V_{DD}/2$ , $C_L = 20pF$			50		ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at $V_{DD}/2$ , $C_L = 20pF$			400		ps
Jitter, Cumulative (RMS)*	$t_{j(LT)}$	PLL-derived outputs From 0-500 $\mu s$ at $V_{DD}/2$ , $C_L = 20pF$ compared to ideal clock source			100		ps
Phase Noise *		PLL derived outputs @ 100KHz offset from fundamental			-80		dbC/Hz

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### 4.0 Package Information

**Table 7: 16-pin SOIC (0.150") Package Dimensions**

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
$\theta$	0°	8°	0°	8°

**Table 8: 16-pin SOIC (0.150") Package Characteristics**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air 16-pin 0.150" SOIC	$\theta_{JA}$	Air flow = 0 m/s	95	°C/W
Lead Inductance, Self	$L_{11}$	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	$L_{12}$	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	$C_{11}$	Any lead to $V_{SS}$	0.5	pF

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### 5.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
<b>11825-808</b>	FS6322-05	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
<b>11825-818</b>	FS6322-05	16-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tubes

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