High Frequency LCD Panel EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Provides up to 20 dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- 40 MHz to 166 MHz input frequency range
- Optimized for SVGA, XGA and high resolution SXGA and UXGA LCD panels
- Internal loop filter minimizes external components and board space
- 2 selectable spreading options
- SSON# control pin for spread spectrum enable and disable options
- 2 selectable modulation rates
- Low cycle-to-cycle jitter
- 3.3V operating range 16 mA output drives
- 16 mA output drives
- TTL or CMOS compatible outputs
- Low power CMOS design
- Supports most mobile graphic accelerator specifications
- Available in 8 pin SOIC and TSSOP

Product Description

The P2160 is a selectable spread spectrum frequency modulator designed compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called "spread spectrum clock generation" reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The P2160 uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

The P2160 modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called "spread spectrum clock generation".

Applications

The P2160 is targeted towards digital flat panel applications for Notebook PCs, Palm-size PCs, Office Automation Equipments, and LCD Monitors, Digital Still Cameras and GPS Devices.
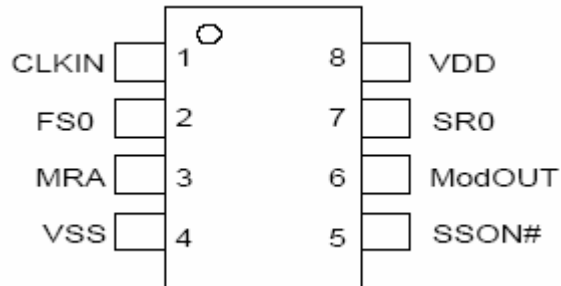
Block Diagram

P2160 Block Diagram
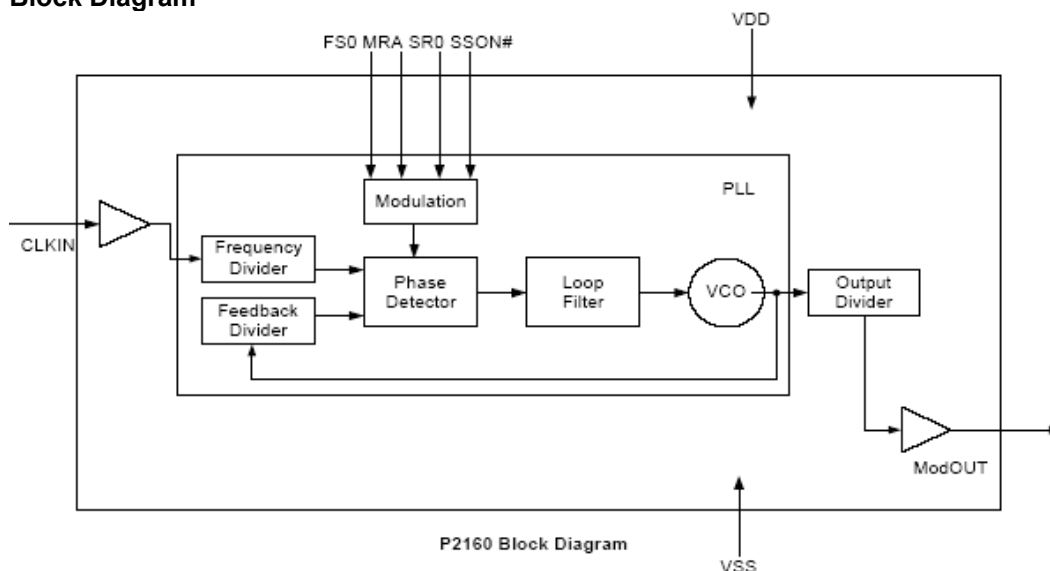
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Pin Configuration

Pin Description

| Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal. Select appropriate frequency range for the intended input frequency (see Table 'Modulation Selection')
2	FSO	I	Digital logic input used to select Frequency Range (see Table 1). This pin has an internal pull-up resistor.
3	MRA	I	Digital logic input used to select Modulation Rate (see Table 1). This pin has an internal pull-up resistor.
4	VSS	P	Ground Connection. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active Low). Spread Spectrum function enable when low. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread Spectrum Clock Output.
7	SRO	I	Digital logic input used to select Spreading Range (see Table 1). This pin has an internal pull-up resistor.
8	VDD	P	Connect to +3.3V

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Table-1 Modulation Selection

FS0	MRA	SR0	Frequency Range	Spread Range	Modulation Rate
0	0	0	40-80MHz	+/- 0.5%	(Fin/40) * 34.72 KHz
0	0	1	40-80MHz	+/- 1.0%	(Fin/40) * 34.72 KHz
0	1	0	40-80MHz	+/- 0.5%	(Fin/40) * 20.83 KHz
0	1	1	40-80MHz	+/- 1.0%	(Fin/40) * 20.83 KHz
1	0	0	80-166MHz	+/- 0.5%	(Fin/80) * 34.72 KHz
1	0	1	80-166MHz	+/- 1.00%	(Fin/80) * 34.72 KHz
1	1	0	80-166MHz	+/- 0.5%	(Fin/80) * 20.83 KHz
1	1	1	80-166MHz	+/- 1.00%	(Fin/80) * 20.83 KHz

Spread Spectrum Selection

Table 1 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: the center frequency is the frequency of the external reference input on CLKIN, Pin 1).

Example: P2160 is designed for high-resolution flat panel applications and is able to support UXGA (1600 X 1200) flat panel that operates on 162 MHz (Fin) clock speed. A spreading selection of FS0=1, SR0=1 and modulation rate selection MRA=1, enables input frequency range from 80 ~ 166 MHz and provides a percentage deviation of +/-1.00% (see Table 1) of the input frequency (Fin). This results in frequency on ModOUT being swept from 160.38 MHz to 163.62 MHz at a modulation rate of 42.18 KHz (162 MHz/80 MHz X 20.83KHz). This particular example (see below figure) given here is a common EMI reduction method for notebook and LCD monitor manufacturers and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

**Application Schematic for Mobile LCD Graphics Controllers**

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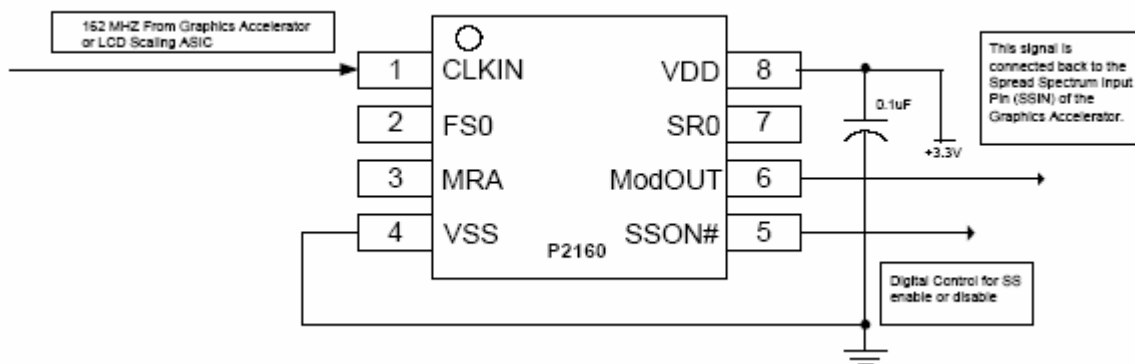
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EMC Software Simulation

By using Alliance Semiconductor's proprietary EMC simulation software – EMI-lator®, radiated system level EMI analysis can be made easier to allow a quantitative assessment on Alliance's EMI reduction products. The simulation engine of this EMC software has already been characterized to correlate with the electrical characteristics of Alliance EMI reduction IC's. The figure below is an example of the simulation result. Please visit our web site at www.alsc.com for information on how to obtain a free copy and demonstration of EMI-lator®.

Simulation Result from EMI-lator®

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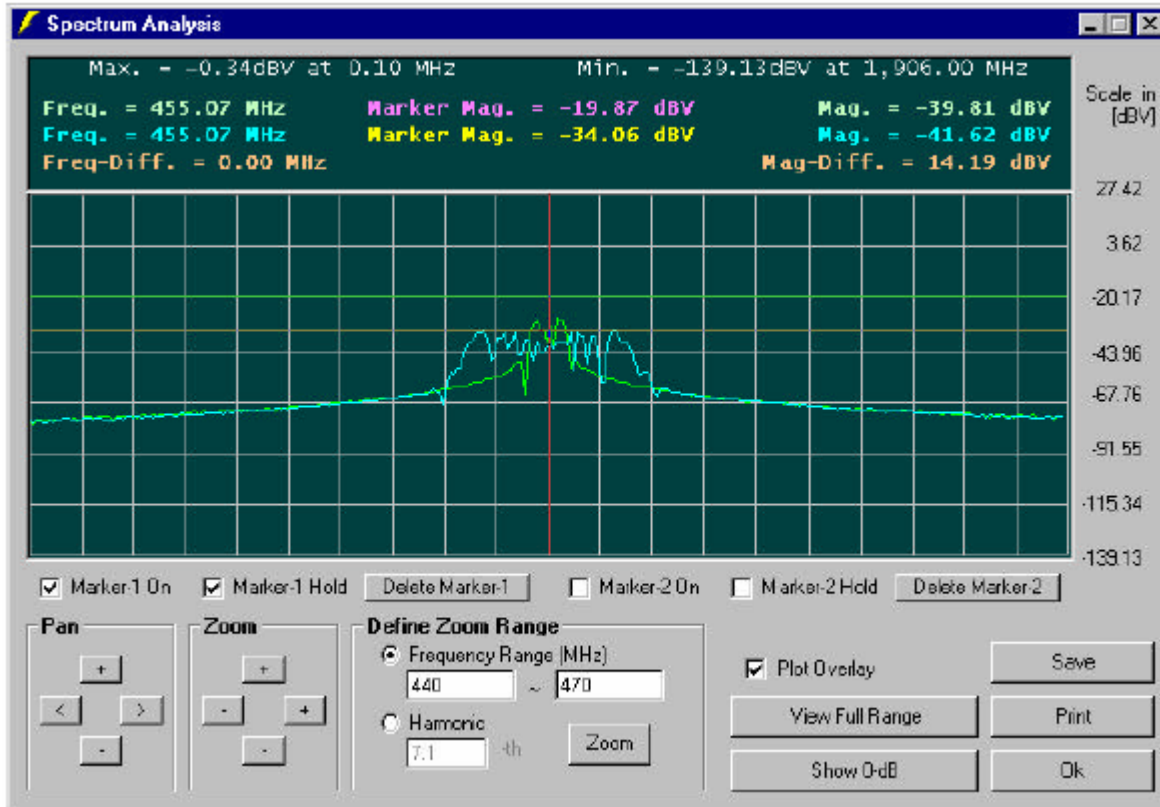
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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to + 7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to +70	°C

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	GND – 0.3	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	V_{DD} + 0.3	V
I_{IL}	Input Low Current (pull-up resistor on inputs FS0, SR0 and MRA)	-	-	-35	μA
I_{IH}	Input High Current (pull-down resistor on input SSON#)	-	-	35	μA
V_{OL}	Output Low Voltage (V_{DD}=3.3V, I_{OL} = 20 mA)	-	-	0.4	V
V_{OH}	Output High Voltage (V_{DD}=3.3V, I_{OH} = 20 mA)	2.5	-	-	V
I_{DD}	Static Supply Current, measured @ FS0=0 @ FS0=1	-	3.27 0.67	-	mA
I_{CC}	Dynamic Supply Current FS0=0 (see f_{IN}) (3.3V and 15 pF loading) FS0=1 (see f_{IN})	7.92 10.9	10 16	12.9 22.1	mA
V_{DD}	Operating Voltage	2.7	3.3	3.8	V
t_{ON}	Power Up Time (First locked clock cycle after power up)		0.18		ms
Z_{OUT}	Clock Output Impedance		50		Ω

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency when FS0=0 FS0=1	40 80	65 120	80 166	MHz MHz
t_{LH}*	Output rise time (Measured at 0.8V to 2.0V)	0.7	0.9	1.1	ns
t_{HL}*	Output fall time (Measured at 0.8V to 2.0V)	0.6	0.8	1.0	ns
t_{JC}	Jitter (cycle to cycle)	-	-	360	ps
t_D	Output duty cycle	45	50	55	%
*t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

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Package Information

Mechanical Package Outline 8-Pin SOIC
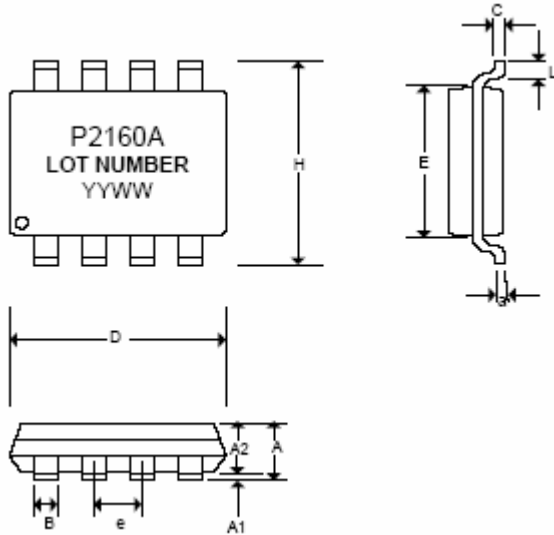
Symbol	Dimensions in inches			Dimensions in millimeters		
	Min	Nor	Max	Min	Nor	Max
A	0.057	0.064	0.071	1.45	1.63	1.80
A1	0.004	0.007	0.010	0.10	0.18	0.25
A2	0.053	0.061	0.069	1.35	1.55	1.75
B	0.012	0.016	0.020	0.31	0.41	0.51
C	0.004	0.006	0.01	0.10	0.15	0.25
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.164	3.75	3.95	4.15
e	0.050 BSC			1.27 BSC		
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.012	0.020	0.028	0.30	0.50	0.70
a	0°	5°	8°	0°	5°	8°

Note: Controlling dimensions are millimeters
SOIC – 0.074 grams unit weight

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Mechanical Package Outline 8-Pin TSSOP

	Dimensions in inches			Dimensions in millimeters		
Symbol	**Min**	**Nor**	**Max**	**Min**	**Nor**	**Max**
A			0.047			1.10
A1	0.002		0.006	0.05		0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007		0.012	0.19		0.30
C	0.004		0.008	0.09		0.20
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0°	5°	8°	0°	5°	8°

Note: Controlling dimensions are millimeters
TSSOP – 0.034 grams unit weight

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Ordering Codes

Part Number	Marking	Package Type	Qty per reel	Temperature (°C)
P2160A-08ST	P2160A	8-pin SOIC, tube		0 to 70
P2160A-08SR	P2160A	8-pin SOIC, tape & reel	2500	0 to 70
P2160A-08TT	P2160A	8-pin TSSOP, tube		0 to 70
P2160A-08TR	P2160A	8-pin TSSOP, tape & reel	2500	0 to 70

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