# 240pin Unbuffered DDR2 SDRAM MODULE

Based on 32Mx16 DDR2 SDRAM

## Features

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 32Mx64 DDR2 Unbuffered DIMM based on 32Mx16 DDR2 SDRAM
- Performance:

| | | PC2-5300 | Unit |
|---|---|---|---|
| Speed Sort | | -3C | |
| DIMM $\overline{CAS}$ Latency* | | 5 | |
| $f_{CK}$ | Clock Frequency | 333 | MHz |
| $t_{CK}$ | Clock Cycle | 3 | ns |
| $f_{DQ}$ | DQ Burst Frequency | 667 | MHz |

- Intended for 333MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD}$ = $V_{DDQ}$ = 1.8Volt ± 0.1
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge
- Write Latency = Read Latency - 1
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 3, 4, 5
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 13/10/2 Addressing (row/column/bank)
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- On Die Termination (ODT)
- Gold contacts
- SDRAMs in 84-ball FBGA Package
- RoHS Compliance

## Description

NT256T64UH4A1FY is 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a one-rank 64Mx64 high-speed memory array. Modules use four 32Mx16 DDR2 SDRAMs in FBGA packages. These DIMMs manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 333MHz clock speeds and achieves high-speed data transfer rates of up to 667MHz. Prior to any access operation, the device $\overline{CAS}$ latency and burst type/ length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

## Ordering Information

| Part Number | Speed | | | Organization | Leads | Power | Note |
|---|---|---|---|---|---|---|---|
| NT256T64UH4A1FY-3C | 333MHz (3ns @ CL = 5) | DDR2-667 | PC2-5300 | 32Mx64 | Gold | 1.8V | Green |

## Pin Description

| | | | |
|---|---|---|---|
| CK0, $\overline{CK0}$ | Differential Clock Inputs | DQ0-DQ63 | Data input/output |
| CKE0, CKE1 | Clock Enable | CB0-CB7 | ECC Check Bit Data Input/Output |
| $\overline{RAS}$ | Row Address Strobe | DQS0-DQS8 | Bidirectional data strobes |
| $\overline{CAS}$ | Column Address Strobe | DM0-DM8/DQS9-17 | Input Data Mask/High Data Strobes |
| $\overline{WE}$ | Write Enable | $\overline{DQS0}$-$\overline{DQS17}$ | Differential data strobes |
| $\overline{CS0}$, $\overline{CS1}$ | Chip Selects | VDD | Power (1.8V) |
| A0-A9, A11-A13 | Address Inputs | VREF | Ref. Voltage for SSTL_18 inputs |
| A10/AP | Column Address Input/Auto-precharge | VDDSPD | Serial EEPROM positive power supply |
| BA0, BA1 | SDRAM Bank Address Inputs | VSS | Ground |
| $\overline{RESET}$ | Reset pin | SCL | Serial Presence Detect Clock Input |
| ODT0, ODT1 | Active termination control lines | SDA | Serial Presence Detect Data input/output |
| NC | No Connect | SA0-2 | Serial Presence Detect Address Inputs |

## Pinout

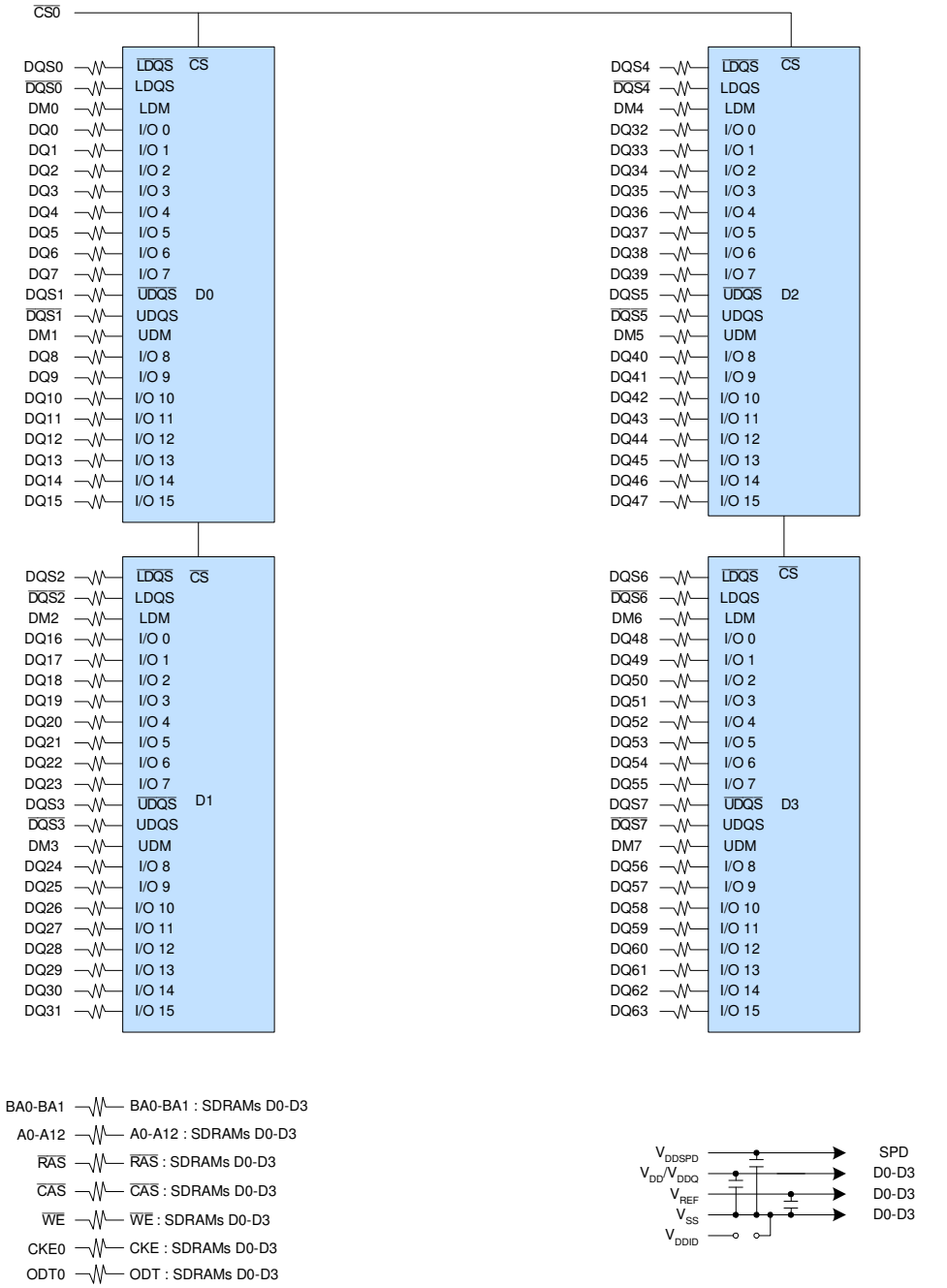
| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF | 42 | NC | 82 | VSS | 121 | VSS | 162 | NC | 202 | DM4 |
| 2 | VSS | 43 | NC | 83 | $\overline{DQS4}$ | 122 | DQ4 | 163 | VSS | 203 | NC |
| 3 | DQ0 | 44 | VSS | 84 | DQS4 | 123 | DQ5 | 164 | NC | 204 | VSS |
| 4 | DQ1 | 45 | NC | 85 | VSS | 124 | VSS | 165 | NC | 205 | DQ38 |
| 5 | VSS | 46 | NC | 86 | DQ34 | 125 | DM0, DQS9 | 166 | VSS | 206 | DQ39 |
| 6 | $\overline{DQS0}$ | 47 | VSS | 87 | DQ35 | 126 | $\overline{DQS9}$ | 167 | NC | 207 | VSS |
| 7 | DQS0 | 48 | NC | 88 | VSS | 127 | VSS | 168 | NC | 208 | DQ44 |
| 8 | VSS | 49 | NC | 89 | DQ40 | 128 | DQ6 | 169 | VSS | 209 | DQ45 |
| 9 | DQ2 | 50 | VSS | 90 | DQ41 | 129 | DQ7 | 170 | VDDQ | 210 | VSS |
| 10 | DQ3 | 51 | VDDQ | 91 | VSS | 130 | VSS | 171 | CKE1 | 211 | DM5 |
| 11 | VSS | 52 | CKE0 | 92 | $\overline{DQS5}$ | 131 | DQ12 | 172 | VDD | 212 | NC |
| 12 | DQ8 | 53 | VDD | 93 | DQS5 | 132 | DQ13 | 173 | NC | 213 | VSS |
| 13 | DQ9 | 54 | NC | 94 | VSS | 133 | VSS | 174 | NC | 214 | DQ46 |
| 14 | VSS | 55 | NC | 95 | DQ42 | 134 | DM1, DQS10 | 175 | VDDQ | 215 | DQ47 |
| 15 | $\overline{DQS1}$ | 56 | VDDQ | 96 | DQ43 | 135 | $\overline{DQS10}$ | 176 | A12 | 216 | VSS |
| 16 | DQS1 | 57 | A11 | 97 | VSS | 136 | VSS | 177 | A9 | 217 | DQ52 |
| 17 | VSS | 58 | A7 | 98 | DQ48 | 137 | CK1 | 178 | VDD | 218 | DQ53 |
| 18 | NC | 59 | VDD | 99 | DQ49 | 138 | $\overline{CK1}$ | 179 | A8 | 219 | VSS |
| 19 | NC | 60 | A5 | 100 | VSS | 139 | VSS | 180 | A6 | 220 | CK2 |
| 20 | VSS | 61 | A4 | 101 | SA2 | 140 | DQ14 | 181 | VDDQ | 221 | $\overline{CK2}$ |
| 21 | DQ10 | 62 | VDDQ | 102 | NC | 141 | DQ15 | 182 | A3 | 222 | VSS |
| 22 | DQ11 | 63 | A2 | 103 | VSS | 142 | VSS | 183 | A1 | 223 | DM6 |
| 23 | VSS | 64 | VDD | 104 | $\overline{DQS6}$ | 143 | DQ20 | 184 | VDD | 224 | NC |
| 24 | DQ16 | KEY | | 105 | DQS6 | 144 | DQ21 | KEY | | 225 | VSS |
| 25 | DQ17 | 65 | VSS | 106 | VSS | 145 | VSS | 185 | CK0 | 226 | DQ54 |
| 26 | VSS | 66 | VSS | 107 | DQ50 | 146 | DM2 | 186 | $\overline{CK0}$ | 227 | DQ55 |
| 27 | $\overline{DQS2}$ | 67 | VDD | 108 | DQ51 | 147 | NC | 187 | VDD | 228 | VSS |
| 28 | DQS2 | 68 | NC | 109 | VSS | 148 | VSS | 188 | A0 | 229 | DQ60 |
| 29 | VSS | 69 | VDD | 110 | DQ56 | 149 | DQ22 | 189 | VDD | 230 | DQ61 |
| 30 | DQ18 | 70 | A10/AP | 111 | DQ57 | 150 | DQ23 | 190 | BA1 | 231 | VSS |
| 31 | DQ19 | 71 | BA0 | 112 | VSS | 151 | VSS | 191 | VDDQ | 232 | DM7 |
| 32 | VSS | 72 | VDDQ | 113 | $\overline{DQS7}$ | 152 | DQ28 | 192 | $\overline{RAS}$ | 233 | NC |
| 33 | DQ24 | 73 | $\overline{WE}$ | 114 | DQS7 | 153 | DQ29 | 193 | $\overline{CS0}$ | 234 | VSS |
| 34 | DQ25 | 74 | $\overline{CAS}$ | 115 | VSS | 154 | VSS | 194 | VDDQ | 235 | DQ62 |
| 35 | Vss | 75 | VDDQ | 116 | DQ58 | 155 | DM3 | 195 | ODT0 | 236 | DQ63 |
| 36 | $\overline{DQS3}$ | 76 | $\overline{CS1}$ | 117 | DQ59 | 156 | NC | 196 | A13 | 237 | VSS |
| 37 | DQS3 | 77 | ODT1 | 118 | VSS | 157 | VSS | 197 | VDD | 238 | VDDSPD |
| 38 | Vss | 78 | VDDQ | 119 | SDA | 158 | DQ30 | 198 | VSS | 239 | SA0 |
| 39 | DQ26 | 79 | Vss | 120 | SCL | 159 | DQ31 | 199 | DQ36 | 240 | SA1 |
| 40 | DQ27 | 80 | DQ32 | | | 160 | VSS | 200 | DQ37 | | |
| 41 | Vss | 81 | DQ33 | | | 161 | NC | 201 | VSS | | |

## Input/Output Functional Description

| Symbol | Type | Polarity | Function |
|---|---|---|---|
| CK0, CK1, CK2 | (SSTL) | Positive Edge | The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks. |
| $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$ | (SSTL) | Negative Edge | The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. |
| CKE0, CKE1 | (SSTL) | Active High | Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode. |
| $\overline{CS0}$, $\overline{CS1}$ | (SSTL) | Active Low | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | (SSTL) | Active Low | When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM. |
| $V_{REF}$ | Supply | | Reference voltage for SSTL-18 inputs |
| $V_{DDQ}$ | Supply | | Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity |
| ODT0, ODT1 | Input | Active High | On-Die Termination control signals |
| BA0, BA1 | (SSTL) | - | Selects which SDRAM bank is to be active. |
| A0 - A9<br>A10/AP<br>A11 - A13 | (SSTL) | - | During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge.<br>During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled.<br>During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge. |
| DQ0 – DQ63<br>CB0 – CB7 | (SSTL) | Active High | Data and Check Bit Input/Output pins. Check bits are only applicable on the x72 DIMM configurations. |
| $V_{DD}$, $V_{SS}$ | Supply | | Power and ground for the DDR SDRAM input buffers and core logic |
| DQS0 – DQS8<br>$\overline{DQS0}$ – $\overline{DQS8}$ | (SSTL) | Negative and Positive Edge | Data strobe for input and output data |
| DM0 – DM8 | Input | Active High | The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules. |
| SA0 – SA2 | | - | Address inputs. Connected to either $V_{DD}$ or $V_{SS}$ on the system board to configure the Serial Presence Detect EEPROM address. |
| SDA | | - | This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to $V_{DD}$ to act as a pull-up. |
| SCL | | - | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to $V_{DD}$ to act as a pull-up. |
| $V_{DDSPD}$ | Supply | | Serial EEPROM positive power supply. |

## Functional Block Diagram

(256MB, 1 Rank, 32Mx16 DDR SDRAMs)

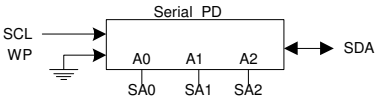









Notes :
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
4. BAx, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
5. Address and control resistors are 22 Ohms +/- 5%



## Serial Presence Detect -- Part 1 of 2

*32Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 32Mx16, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD*

| Byte | Description | SPD Entry Value | Serial PD Data Entry (Hexadecimal) | Note |
|---|---|---|---|---|
| | | DDR2-667 (-3C) | DDR2-667 (-3C) | |
| 0 | Number of Serial PD Bytes Written during Production | 128 | 80 | |
| 1 | Total Number of Bytes in Serial PD device | 256 | 08 | |
| 2 | Fundamental Memory Type | DDR2-SDRAM | 08 | |
| 3 | Number of Row Addresses on Assembly | 13 | 0D | |
| 4 | Number of Column Addresses on Assembly | 10 | 0A | |
| 5 | Number of DIMM Bank | 1 rank, Height=30mm | 60 | |
| 6 | Data Width of Assembly | X64 | 40 | |
| 7 | Reserved | Undefined | 00 | |
| 8 | Voltage Interface Level of this Assembly | SSTL_1.8 | 05 | |
| 9 | DDR2 SDRAM Device Cycle Time at CL=5 | 3ns | 30 | |
| 10 | DDR2 SDRAM Device Access Time from Clock at CL=5 | ±0.45ns | 45 | |
| 11 | DIMM Configuration Type | Non - ECC | 00 | |
| 12 | Refresh Rate/Type | 7.8us/self | 82 | |
| 13 | Primary DDR SDRAM Width | X16 | 10 | |
| 14 | Error Checking DDR SDRAM Device Width | N/A | 00 | |
| 15 | Reserved | Undefined | 00 | |
| 16 | DDR2 SDRAM Device Attributes: Burst Length Supported | 4,8 | 0C | |
| 17 | DDR2 SDRAM Device Attributes: Number of Device Banks | 4 | 04 | |
| 18 | DDR2 SDRAM Device Attributes: CAS Latencies Supported | 3/4/5 | 38 | |
| 19 | DIMM Mechanical Characteristics | < 4.1mm | 01 | |
| 20 | DDR2 SDRAM DIMM Type Information | Unbuffered DIMM | 02 | |
| 21 | DDR2 SDRAM Module Attributes: | Normal DIMM | 00 | |
| 22 | DDR2 SDRAM Device Attributes: General | Support 50Ω ODT | 03 | |
| 23 | Minimum Clock Cycle at CL=4 | 3.75ns | 3D | |
| 24 | Maximum Data Access Time from Clock at CL=4 | ±0.5ns | 50 | |
| 25 | Minimum Clock Cycle Time at CL=3 | 5ns | 50 | |
| 26 | Maximum Data Access Time from Clock at CL=3 | ±0.6ns | 60 | |
| 27 | Minimum Row Precharge Time ($t_{RP}$) | 15ns | 3C | |
| 28 | Minimum Row Active to Row Active delay ($t_{RRD}$) | 10ns | 28 | |
| 29 | Minimum RAS to CAS delay ($t_{RCD}$) | 15ns | 3C | |
| 30 | Minimum RAS Pulse Width ($t_{RAS}$) | 45ns | 2D | |
| 31 | Module Bank Density | 256MB | 40 | |
| 32 | Address and Command Setup Time Before Clock (tIS) | 0.2ns | 20 | |
| 33 | Address and Command Hold Time After Clock (tIH) | 0.275ns | 27 | |
| 34 | Data Input Setup Time Before Clock (tDS) | 0.10ns | 10 | |
| 35 | Data Input Hold Time After Clock (tDH) | 0.175ns | 17 | |
| 36 | Write Recovery Time (tWR) | 15ns | 3C | |
| 37 | Internal Write to Read Command delay (tWTR) | 7.5ns | 1E | |
| 38 | Internal Read to Precharge delay (tRTP) | 7.5ns | 1E | |
| 39 | Reserved | Undefined | 00 | |
| 40 | Extension of Byte 41 tRC and Byte 42 tRFC | The number below a decimal point of $t_{RC}$ and $t_{RFC}$ are 0, $t_{RFC}$ is less than 256ns | 00 | |

## Serial Presence Detect -- Part 2 of 2

*32Mx64 1 BANK UNBUFFERED DDR2 SDRAM DIMM based on 32Mx16, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD*

| Byte | Description | SPD Entry Value | Serial PD Data Entry (Hexadecimal) | Note |
|---|---|---|---|---|
| | | DDR2-667 (-3C) | DDR2-667 (-3C) | |
| 41 | Minimum Core Cycle Time (tRC) | 60ns | 3C | |
| 42 | Min. Auto Refresh Command Cycle Time (tRFC) | 105ns | 69 | |
| 43 | Maximum Clock Cycle Time (tCK) | 8ns | 80 | |
| 44 | Max. DQS-DQ Skew Factor (tQHS) | 0.24ns | 18 | |
| 45 | Read Data Hold Skew Factor (tQHS) | 0.34ns | 22 | |
| 46 | PLL Relock Time | N/A | 00 | |
| 47 | Tcasemax | 6˚C | 55 | |
| 48 | Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM) | 118˚C/W | 76 | |
| 49 | DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits) | 36˚C | 6B | |
| 50 | DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q) | 56˚C | 38 | |
| 51 | DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P) | 37˚C | 25 | |
| 52 | DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N) | 37˚C | 25 | |
| 53 | DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast) | 43˚C | 2B | |
| 54 | DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow) | 27˚C | 1B | |
| 55 | DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit) | 42˚C | 54 | |
| 56 | DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B) | 36˚C | 24 | |
| 57 | DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7) | 54˚C | 36 | |
| 58 | Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL) | 00 | 00 | |
| 59 | Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register) | 00 | 00 | |
| 60 | PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active) | 00 | 00 | |
| 61 | Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit(DT Register Active/Mode Bit) | 00 | 00 | |
| 62 | SPD Revision | 1.2 | 12 | |
| 63 | Checksum Data | Checksum Data | EE | |
| 64-71 | Manufacturer's JEDEC ID Code | NANYA | 7F7F7F0B00000000 | |
| 72 | Module Manufacturing Location | Manufacturing code | -- | |
| 73-91 | Module Part number | Module Part Number in ASCII | -- | 1 |
| 92-255 | Reserved | Undefined | -- | |

Note:
1. NT256T64UH4A1FY-3C ➔ 4E54323536543634554834413146592D334320

## Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{IN}$, $V_{OUT}$ | Voltage on I/O pins relative to Vss | -0.5 to 2.3 | V |
| $V_{DD}$ | Voltage on VDD supply relative to Vss | -1.0 to +2.3 | V |
| $V_{DDQ}$ | Voltage on VDDQ supply relative to Vss | -0.5 to +2.3 | V |
| $H_{STG}$ | Storage Humidity (without condensation) | 5 to 95 | % |
| $T_A$ | Operating Temperature (Ambient) | 0 to +70 | ℃ |
| $T_{STG}$ | Storage Temperature (Plastic) | -55 to +100 | ℃ |

**Note**: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC operating Conditions

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| $T_{CASE}$ | Operating Temperature (Ambient) | 0 to 95 | ℃ | 1,2,3 |
| $T_{STG}$ | Storage Temperature (Plastic) | -55 to 100 | ℃ | |
| $I_L$ | Short Circuit Output Current | -5 to 5 | μA | |
| $T_{OPR}$ | Module Operating Temperature Range (ambient) | 0 to 55 | ℃ | |
| $H_{OPR}$ | Operating Humidity (relative) | 10 to 90 | % | |

**Note:**
1. Case temperature is measured at top and center side of any DRAMs.
2. $t_{CASE}$ > 85℃ ➔ $t_{REFI}$ = 3.9 μs
3. All DRAM specification only support 0℃ < $t_{CASE}$ < 85℃

## DC Electrical Characteristics and Operating Conditions

($T_{CASE}$ = 0 ℃ ~ 85 ℃; $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V, See AC Characteristics)

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.7 | 1.9 | V | 1 |
| $V_{DDQ}$ | I/O Supply Voltage | 1.7 | 1.9 | V | 1 |
| $V_{SS}$, $V_{SSQ}$ | Supply Voltage, I/O Supply Voltage | 0 | 0 | V | |
| $V_{REF}$ | I/O Reference Voltage | 0.49$V_{DDQ}$ | 0.51$V_{DDQ}$ | V | 1, 2 |
| $V_{IH}$ (DC) | Input High (Logic1) Voltage | $V_{REF}$ + 0.125 | $V_{DDQ}$ + 0.3 | V | 1 |
| $V_{IL}$ (DC) | Input Low (Logic0) Voltage | -0.3 | $V_{REF}$ - 0.125 | V | 1 |

**Note:**
1. Inputs are not recognized as valid until $V_{REF}$ stabilizes.
2. $V_{REF}$ is expected to be equal to 0.5 $V_{DDQ}$ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on $V_{REF}$ may not exceed 2% of the DC value.

## On Die Termination (ODT) Current

| Symbol | Parameter | Min | Max | Units | EMRS(1) State |
|---|---|---|---|---|---|
| IODTO | Enabled ODT current per DQ<br>ODT is HIGH; Data Bus inputs are FLOATING | 5 | 7.5 | mA/DQ | A6=0, A2=1 |
| | | 2.5 | 3.75 | mA/DQ | A6=1, A2=0 |
| IODTT | Active ODT current per DQ<br>ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING | 10 | 15 | mA/DQ | A6=0, A2=1 |
| | | 5 | 7.5 | mA/DQ | A6=1, A2=0 |

## Operating, Standby, and Refresh Currents

$T_{CASE}$ = 0 ℃ ~ 80 ℃; $V_{DDQ}$ = $V_{DD}$= 1.8V ± 0.1V (256MB, 1 Rank, 32x16 DDR2 SDRAMs)

| Symbol | Parameter/Condition | PC2-5300 (-3C) | Unit | Notes |
|---|---|---|---|---|
| $I_{DD0}$ | Operating Current: one bank; active/precharge; $t_{RC}$ = $t_{RC\ (MIN)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | 380 | mA | 1 |
| $I_{DD1}$ | Operating Current: one bank; active/read/precharge; Burst = 2; $t_{RC}$ = $t_{RC\ (MIN)}$; CL=2.5; $t_{CK}$ = $t_{CK\ (MIN)}$; $I_{OUT}$ = 0mA; address and control inputs changing once per clock cycle | 440 | mA | 1 |
| $I_{DD2P}$ | Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$ | 20 | mA | 1 |
| $I_{DD2N}$ | Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle | 200 | mA | 1 |
| $I_{DD3PF}$ | Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; MRS(12) = 0 | 76 | mA | 1 |
| $I_{DD3PS}$ | Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; MRS(12) = 1 | 24 | mA | 1 |
| $I_{DD3N}$ | Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; $t_{RC}$ = $t_{RAS\ (MAX)}$; $t_{CK}$ = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle | 200 | mA | 1 |
| $I_{DD4R}$ | Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; $t_{CK}$ = $t_{CK\ (MIN)}$; $I_{OUT}$ = 0mA | 600 | mA | 1 |
| $I_{DD4W}$ | Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; $t_{CK}$ = $t_{CK\ (MIN)}$ | 680 | mA | 1 |
| $I_{DD5B}$ | Burst Auto-Refresh Current: $t_{RFC}$ = $t_{RFC\ (MIN)}$ | 640 | mA | 1 |
| $I_{DD5D}$ | Distributed Auto-Refresh Current: $t_{RFC}$ = $t_{REFI}$ | 24 | mA | 1 |
| $I_{DD6}$ | Self-Refresh Current: CKE ≤ 0.2V | 20 | mA | 1 |
| $I_{DD7}$ | Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC}$ = $t_{RC}$ (min); $I_{OUT}$ = 0mA. | 960 | mA | 1 |

**Note:**
1. Module IDD data was calculated from component IDD. It may differ from the actual measurement.

## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

($T_{CASE}$ = 0 ℃ ~ 85 ℃; $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

| Symbol | Parameter | | -3C | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| tAC | DQ output access time from CK/$\overline{CK}$ | | -0.45 | +0.45 | ns |
| tDQSCK | DQS output access time from CK/$\overline{CK}$ | | -0.4 | +0.4 | ns |
| tCH | CK high-level width | | 0.45 | 0.55 | tCK |
| tCL | CK low-level width | | 0.45 | 0.55 | tCK |
| tHP | Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time | | tCH or tCL | - | tCK |
| tCK | Clock cycle time | CL=3 | 3 | 8 | ns |
| tCK | | CL=4, 5 | 3 | 8 | ns |
| tDH | DQ and DM input hold time(differential data strobe) | | 0.175 | - | ns |
| tDS | DQ and DM input setup time(differential data strobe) | | 0.1 | - | ns |
| tIPW | Input pulse width | | 0.6 | - | tCK |
| tDIPW | DQ and DM input pulse width (each input) | | 0.35 | - | tCK |
| tHZ | Data-out high-impedance time from CK/$\overline{CK}$ | | - | tACmax | ns |
| tLZ(DQ) | Data-out low-impedance time from CK/$\overline{CK}$ | | 2tACmin | tACmax | ns |
| tLZ(DQS) | DQS low-impedance time from CK/$\overline{CK}$ | | tACmin | tACmax | ns |
| tDQSQ | DQS-DQ skew (DQS & associated DQ signals) | | 0.24 | - | ns |
| tQHS | Data hold Skew Factor | | 0.34 | - | ns |
| tQH | Data output hold time from DQS | | tHP - tQHS | - | ns |
| tDQSS | Write command to 1st DQS latching transition | | -0.25 | +0.25 | tCK |
| tDQSL,(H) | DQS input low (high) pulse width (write cycle) | | 0.35 | - | tCK |
| tDSS | DQS falling edge to CK setup time (write cycle) | | 0.2 | - | tCK |
| tDSH | DQS falling edge hold time from CK (write cycle) | | 0.2 | - | tCK |
| tMRD | Mode register set command cycle time | | 2 | - | tCK |
| tWPST | Write postamble | | 0.40 | 0.60 | tCK |
| tWPRE | Write preamble | | 0.35 | - | tCK |
| tIH | Address and control input hold time | | 0.275 | - | ns |
| tIS | Address and control input setup time | | 0.20 | - | ns |
| tRPRE | Read preamble | | 0.90 | 1.10 | tCK |
| tRPST | Read postamble | | 0.40 | 0.60 | tCK |
| tRRD | Active bank A to Active bank B command | | 7.5 | | ns |
| tDelay | Minimum time clocks remains ON after CKE asynchronously drops Low | | tIS + tCK + tIH | - | ns |
| tREFI | Average Periodic Refresh Interval (85ºC < $T_{CASE}$ ≤ 95ºC) | | - | 3.9 | µs |
| | Average Periodic Refresh Interval (0ºC ≤ $T_{CASE}$ ≤ 85ºC) | | - | 7.8 | µs |
| tOIT | OCD drive mode output delay | | 0 | 12 | ns |
| tRFC | Auto-Refresh to Active/Auto-Refresh command period | | 105 | - | ns |
| tCCD | $\overline{CAS}$ to $\overline{CAS}$ | | 2 | | tCK |

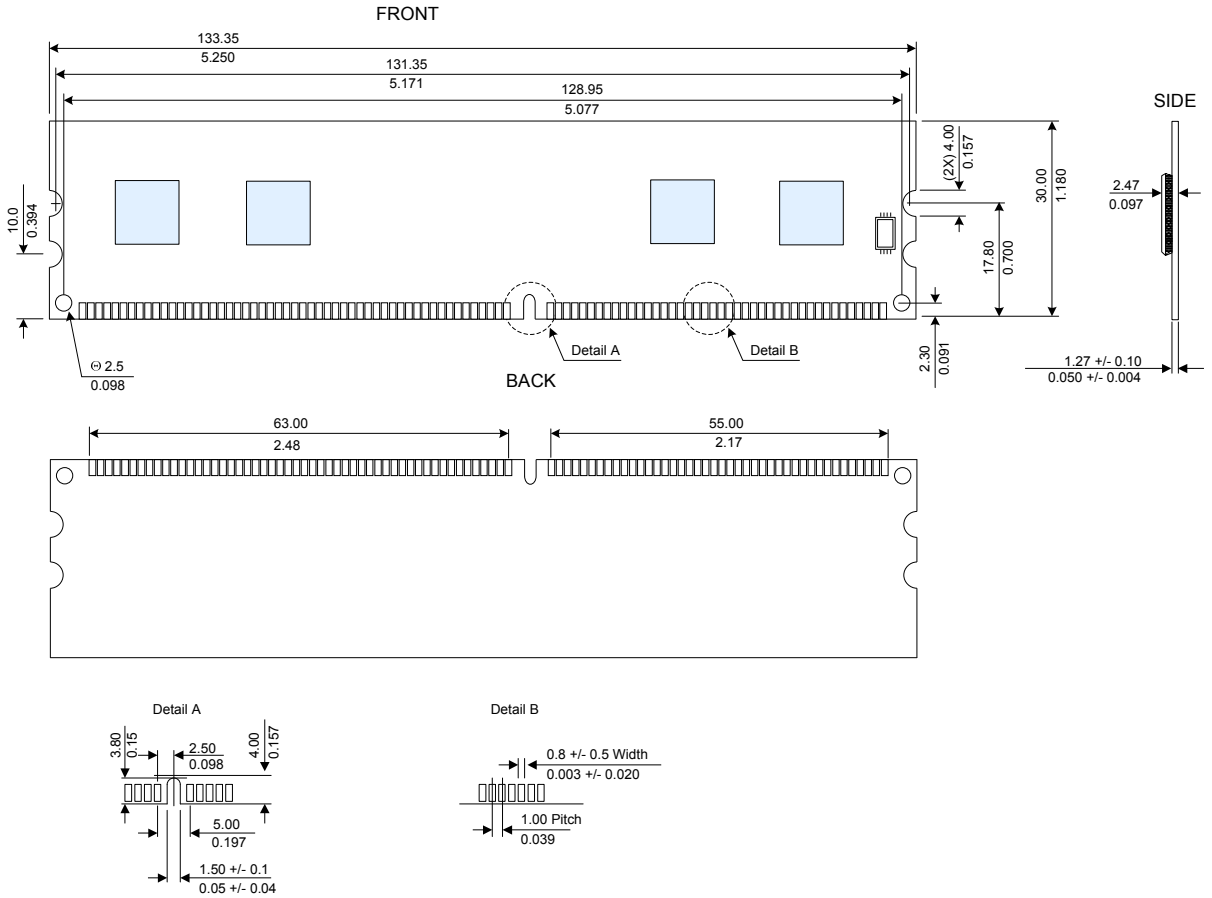
## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

($T_{CASE}$ = 0 ℃ ~ 85 ℃; $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

| Symbol | Parameter | -3C | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| tWR | Write recovery time without Auto-Precharge | 15 | - | ns |
| WR | Write recovery time with Auto-Precharge | tWR/tCK | | tCK |
| tDAL | Auto precharge write recovery + precharge time | WR+tRP | - | tCK |
| tWTR | Internal write to read command delay | 7.5 | - | ns |
| tRTP | Internal read to precharge command delay | 7.5 | - | ns |
| tXSNR | Exit self refresh to a Non-read command | tRFC+10 | - | ns |
| tXSRD | Exit self refresh to a Read command | 200 | - | tCK |
| tXP | Exit precharge power down to any Non- read command | 2 | - | tCK |
| tXARD | Exit active power down to read command | 2 | - | tCK |
| tXARDS | Exit active power down to read command | 7-AL | - | tCK |
| tCKE | CKE minimum pulse width | 3 | - | tCK |
| **ODT** | | | | |
| tAOND | ODT turn-on delay | 2 | 2 | tCK |
| tAON | ODT turn-on | tAC (min) | tAC (max) +0.7 | ns |
| tAONPD | ODT turn-on (Power down mode) | tAC (min) +2 | 2tCK + tAC(max) +1 | ns |
| tAOFD | ODT turn-off delay | 2.5 | 2.5 | tCK |
| tAOF | ODT turn-off | tAC(min) | tAC(max) +0.6 | ns |
| tAOFPD | ODT turn-off (Power down mode) | tAC (min)+2 | 2.5tCK + tAC(max) +1 | ns |
| tANPD | ODT to power down entry latency | 3 | - | tCK |
| tAXPD | ODT power down exit latency | 8 | - | tCK |
| **Speed Grade Definition** | | | | |
| tRAS | Row Active Time | 45 | 70,000 | ns |
| tRC | Row Cycle Time | 60 | - | ns |
| tRCD | RAS to CAS delay | 15 | - | ns |
| tRP | Row Precharge Time | 15 | - | ns |

## Package Dimensions

(1 Rank, 32Mx16 DDR SDRAMs)




Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

## Revision Log

| Rev | Date | Modification |
|---|---|---|
| 0.1 | 05/2005 | Preliminary Release |
| 1.0 | 06/2005 | Official Release |
| 1.1 | 11/2005 | Update SPD code |
| 1.2 | 03/2006 | Update Package Dimensions. |
| 1.3 | 08/2006 | Update Package Dimensions. |