# NT2GC64B88D0NS / NT4GC64B8HD0NS
# 2GB: 256M x 64 / 4GB: 512M x 64
# PC3-8500 / PC3-10600
# Unbuffered DDR3 SO-DIMM

Based on DDR3-1066/1333 256Mx8 SDRAM D-Die

## Features

•Performance:

| Speed Sort | PC3-8500 | PC3-10600 | Unit |
|---|---|---|---|
| | -BE | -CG | |
| DIMM CAS Latency | 7 | 9 | |
| fck – Clock Freqency | 533 | 667 | MHz |
| tck – Clock Cycle | 1.875 | 1.5 | ns |
| fDQ – DQ Burst Freqency | 1066 | 1333 | Mbps |

- 204-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- 2GB / 4GB: 256Mx64 / 512Mx64 Unbuffered DDR3 SO-DIMM based on 256Mx8 DDR3 SDRAM D-Die devices.
- Intended for 533MHz/667MHz applications
- Inputs and outputs are SSTL-15 compatible
- VDD = VDDQ = 1.5V ±0.075V
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Auto Self-Refresh option
- •Nominal and Dynamtic On-Die Termination support

Programmable Operation:
- DIMM $\overline{CAS}$ Latency: 5, 6,7,8,9
- Burst Type: Sequential or Interleave
- Burst Length: BC4, BL8
- Operation: Burst Read and Write

- Address and control signals are fully synchronous to positive clock edge
- Two different termination values (Rtt_Nom & Rtt_WR)
- 15/10/1 (row/column/rank) Addressing for 2GB
- 15/10/2 (row/column/rank) Addressing for 4GB
- Extended operating temperature rage
- Serial Presence Detect
- Gold contacts
- SDRAMs are in 78-ball BGA Package
- RoHS compliance and Halogen Free

## Description

NT2GC64B88D0NS / NT4GC64B8HD0NS are unbuffered 204-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as two ranks of 256Mx64 (2GB) and 512Mx64 (4GB) high-speed memory array. Modules use eight 256Mx8 (2GB) 78-ball BGA packaged devices and sixteen 256Mx8 (4GB) 78-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR3 SODIMMs provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 533MHz/667MHz clock speeds and achieves high-speed data transfer rates of 1066Mbps/1333Mbps. Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 (2GB)/A0-A14 (4GB) and I/O inputs BA0~BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

## Ordering Information

| Part Number | Speed | | | Organization | Power | Leads | Note |
|---|---|---|---|---|---|---|---|
| NT2GC64B88D0NS-BE | DDR3-1066 | PC3-8500 | 533MHz (1.875ns @ CL = 7) | 256Mx64 | 1.5V | Gold | |
| NT2GC64B88D0NS-CG | DDR3-1333 | PC3-10600 | 667MHz (1.500ns @ CL = 9) | | | | |
| NT4GC64B8HD0NS-BE | DDR3-1066 | PC3-8500 | 533MHz (1.875ns @ CL = 7) | 512Mx64 | | | |
| NT4GC64B8HD0NS-CG | DDR3-1333 | PC3-10600 | 667MHz (1.500ns @ CL = 9) | | | | |

## Pin Description

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| CK0, CK1 | Clock Inputs, positive line | DQ0-DQ63 | Data input/output |
| $\overline{CK0}$, $\overline{CK1}$ | Clock Inputs, negative line | DQS0-DQS7 | Data strobes |
| CKE0, CKE1 | Clock Enable | $\overline{DQS0}$-$\overline{DQS7}$ | Data strobes complement |
| $\overline{RAS}$ | Row Address Strobe | DM0-DM7 | Data Masks |
| $\overline{CAS}$ | Column Address Strobe | $\overline{EVENT}$ | Temperature event pin |
| $\overline{WE}$ | Write Enable | $\overline{RESET}$ | Reset pin |
| $\overline{S0}$, $\overline{S1}$ | Chip Selects | $V_{REFDQ}$ , $V_{REFCA}$ | Input/Output Reference |
| A0-A9, A11, A13-A15 | Address Inputs | $V_{DDSPD}$ | SPD and Temp sensor power |
| A10/AP | Address Input/Auto-Precharge | SA0, SA1 | Serial Presence Detect Address Inputs |
| A12/$\overline{BC}$ | Address Input/Burst Chop | Vtt | Termination voltage |
| BA0-BA2 | SDRAM Bank Address Inputs | $V_{SS}$ | Ground |
| ODT0, ODT1 | Active termination control lines | $V_{DD}$ | Core and I/O power |
| SCL | Serial Presence Detect Clock Input | NC | No Connect |
| SDA | Serial Presence Detect Data input/output | | |

Note: A14 is for 4GB modules only.

## DDR3 SDRAM Pin Assignment

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REFDQ}$ | 2 | $V_{SS}$ | 53 | DQ19 | 54 | $V_{SS}$ | 105 | $V_{DD}$ | 106 | $V_{DD}$ | 155 | $V_{SS}$ | 156 | $V_{SS}$ |
| 3 | $V_{SS}$ | 4 | DQ4 | 55 | $V_{SS}$ | 56 | DQ28 | 107 | A10/AP | 108 | BA1 | 157 | DQ42 | 158 | DQ46 |
| 5 | DQ0 | 6 | DQ5 | 57 | DQ24 | 58 | DQ29 | 109 | BA0 | 110 | $\overline{RAS}$ | 159 | DQ43 | 160 | DQ47 |
| 7 | DQ1 | 8 | $V_{SS}$ | 59 | DQ25 | 60 | $V_{SS}$ | 111 | $V_{DD}$ | 112 | $V_{DD}$ | 161 | $V_{SS}$ | 162 | $V_{SS}$ |
| 9 | $V_{SS}$ | 10 | $\overline{DQS0}$ | 61 | $V_{SS}$ | 62 | $\overline{DQS3}$ | 113 | $\overline{WE}$ | 114 | $\overline{S0}$ | 163 | DQ48 | 164 | DQ52 |
| 11 | DM0 | 12 | DQS0 | 63 | DM3 | 64 | DQS3 | 115 | $\overline{CAS}$ | 116 | ODT0 | 165 | DQ49 | 166 | DQ53 |
| 13 | $V_{SS}$ | 14 | $V_{SS}$ | 65 | $V_{SS}$ | 66 | $V_{SS}$ | 117 | $V_{DD}$ | 118 | $V_{DD}$ | 167 | $V_{SS}$ | 168 | $V_{SS}$ |
| 15 | DQ2 | 16 | DQ6 | 67 | DQ26 | 68 | DQ30 | 119 | A13/NC | 120 | ODT1 | 169 | $\overline{DQS6}$ | 170 | DM6 |
| 17 | DQ3 | 18 | DQ7 | 69 | DQ27 | 70 | DQ31 | 121 | $\overline{S1}$ | 122 | NC | 171 | DQS6 | 172 | $V_{SS}$ |
| 19 | $V_{SS}$ | 20 | $V_{SS}$ | 71 | $V_{SS}$ | 72 | $V_{SS}$ | 123 | $V_{DD}$ | 124 | $V_{DD}$ | 173 | $V_{SS}$ | 174 | DQ54 |
| 21 | DQ8 | 22 | DQ12 | 73 | CKE0 | 74 | CKE1 | 125 | NC | 126 | $V_{REFCA}$ | 175 | DQ50 | 176 | DQ55 |
| 23 | DQ9 | 24 | DQ13 | 75 | $V_{DD}$ | 76 | $V_{DD}$ | 127 | $V_{SS}$ | 128 | $V_{SS}$ | 177 | DQ51 | 178 | $V_{SS}$ |
| 25 | $V_{SS}$ | 26 | $V_{SS}$ | 77 | NC | 78 | A15/NC | 129 | DQ32 | 130 | DQ36 | 179 | $V_{SS}$ | 180 | DQ60 |
| 27 | $\overline{DQS1}$ | 28 | DM1 | 79 | BA2 | 80 | A14/NC | 131 | DQ33 | 132 | DQ37 | 181 | DQ56 | 182 | DQ61 |
| 29 | DQS1 | 30 | $\overline{RESET}$ | 81 | $V_{DD}$ | 82 | $V_{DD}$ | 133 | $V_{SS}$ | 134 | $V_{SS}$ | 183 | DQ57 | 184 | $V_{SS}$ |
| 31 | $V_{SS}$ | 32 | $V_{SS}$ | 83 | A12/$\overline{BC}$ | 84 | A11 | 135 | $\overline{DQS4}$ | 136 | DM4 | 185 | $V_{SS}$ | 186 | $\overline{DQS7}$ |
| 33 | DQ10 | 34 | DQ14 | 85 | A9 | 86 | A7 | 137 | DQS4 | 138 | $V_{SS}$ | 187 | DM7 | 188 | DQS7 |
| 35 | DQ11 | 36 | DQ15 | 87 | $V_{DD}$ | 88 | $V_{DD}$ | 139 | $V_{SS}$ | 140 | DQ38 | 189 | $V_{SS}$ | 190 | $V_{SS}$ |
| 37 | $V_{SS}$ | 38 | $V_{SS}$ | 89 | A8 | 90 | A6 | 141 | DQ34 | 142 | DQ39 | 191 | DQ58 | 192 | DQ62 |
| 39 | DQ16 | 40 | DQ20 | 91 | A5 | 92 | A4 | 143 | DQ35 | 144 | $V_{SS}$ | 193 | DQ59 | 194 | DQ63 |
| 41 | DQ17 | 42 | DQ21 | 93 | $V_{DD}$ | 94 | $V_{DD}$ | 145 | $V_{SS}$ | 146 | DQ44 | 195 | $V_{SS}$ | 196 | $V_{SS}$ |
| 43 | $V_{SS}$ | 44 | $V_{SS}$ | 95 | A3 | 96 | A2 | 147 | DQ40 | 148 | DQ45 | 197 | SA0 | 198 | $\overline{EVENT}$ |
| 45 | $\overline{DQS2}$ | 46 | DM2 | 97 | A1 | 98 | A0 | 149 | DQ41 | 150 | $V_{SS}$ | 199 | $V_{DDSPD}$ | 200 | SDA |
| 47 | DQS2 | 48 | $V_{SS}$ | 99 | $V_{DD}$ | 100 | $V_{DD}$ | 151 | $V_{SS}$ | 152 | $\overline{DQS5}$ | 201 | SA1 | 202 | SCL |
| 49 | $V_{SS}$ | 50 | DQ22 | 101 | CK0 | 102 | CK1 | 153 | DM5 | 154 | DQS5 | 203 | Vtt | 204 | Vtt |
| 51 | DQ18 | 52 | DQ23 | 103 | $\overline{CK0}$ | 104 | $\overline{CK1}$ | | | | | | | | |

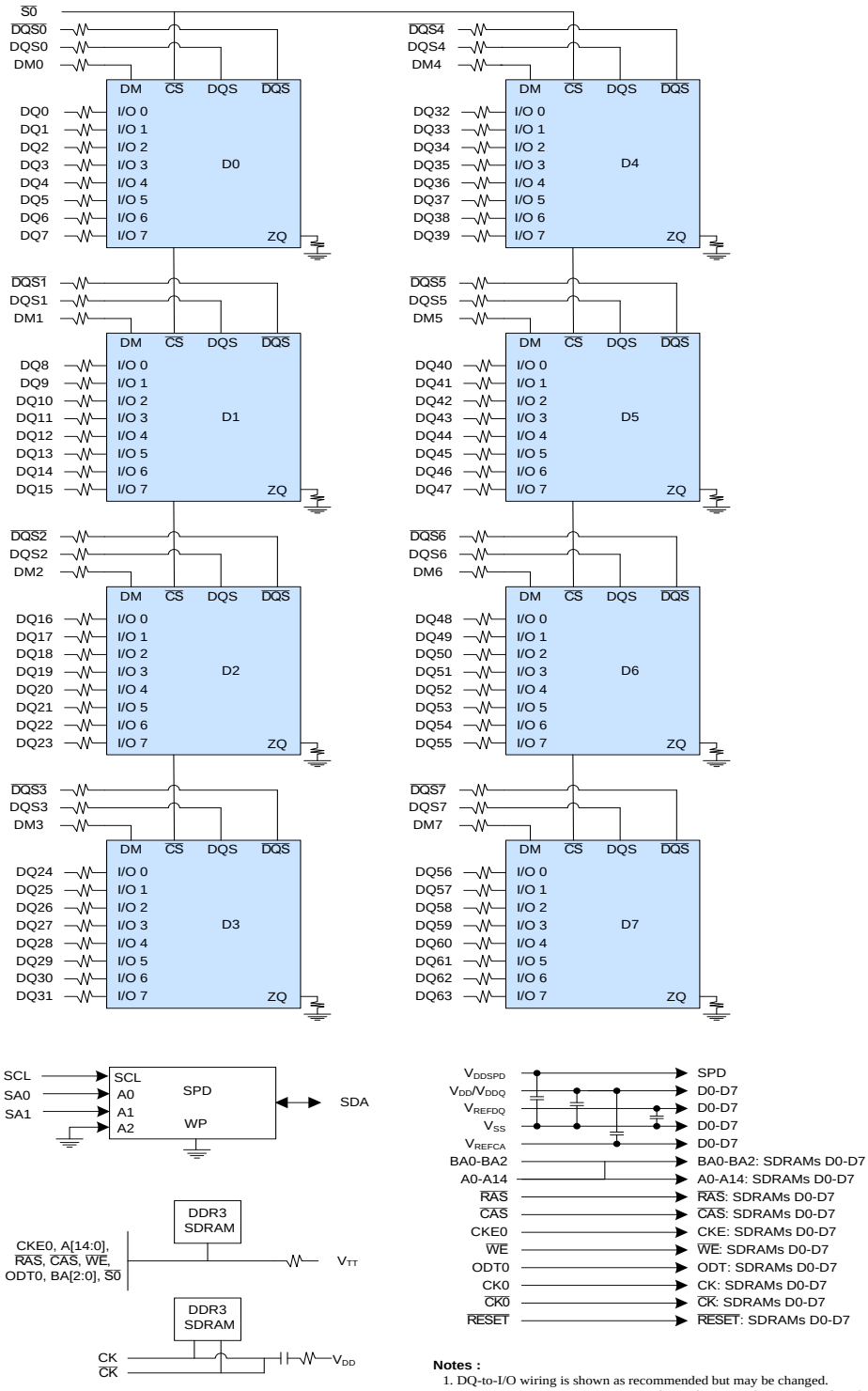
Note: A14 is for 4GB modules only.

## Input/Output Functional Description

| Symbol | Type | Polarity | Function |
|---|---|---|---|
| CK0, CK1<br>$\overline{CK0}$, $\overline{CK1}$ | Input | Cross point | The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock. |
| CKE0, CKE1 | Input | Active High | Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode. |
| $\overline{S0}$, $\overline{S1}$ | Input | Active Low | Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue, Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | Active Low | When sampled at the positive rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM. |
| ODT0, ODT1 | Input | Active High | Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register. |
| DM0 – DM7 | Input | Active High | The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. |
| DQS0 – DQS7<br>$\overline{DQS0}$ – $\overline{DQS7}$ | I/O | Cross point | The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the cross point of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to $V_{SS}$ and DDR3 SDRAM mode registers programmed appropriately. |
| BA0, BA1, BA2 | Input | - | Selects which DDR3 SDRAM internal bank of four or eight is activated. |
| A0 – A9<br>A10/AP<br>A11<br>A12/$\overline{BC}$<br>A13 – A15 | Input | - | During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. |
| DQ0 – DQ63 | Input | - | Data Input/Output pins. |
| $V_{DD}$, $V_{DDSPD}$, $V_{SS}$ | Supply | - | Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module. |
| $V_{REFDQ}$, $V_{REFCA}$ | Supply | - | Reference voltage for SSTL15 inputs |
| SDA | I/O | - | This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and temp sensor. A resistor must be connected from the SDA bus line to $V_{DDSPD}$ on the system planar to act as a pull up. |
| SCL | Input | - | This signal is used to clock data into and out of the SPD EEPROM and Temp sensor. |
| SA0 – SA2 | Input | - | Address pins used to select the Serial Presence Detect and Temp sensor base address. |
| $\overline{EVENT}$ | Output | - | The $\overline{EVENT}$ pin is reserved for use to flag critical module temperature. |
| $\overline{RESET}$ | Input | - | This signal resets the DDR3 SDRAM |
| ZQ | Supply | - | Reference pin for ZQ calibration |

## Functional Block Diagram

[2GB – 1 Rank, 256Mx8 DDR3 SDRAMs]

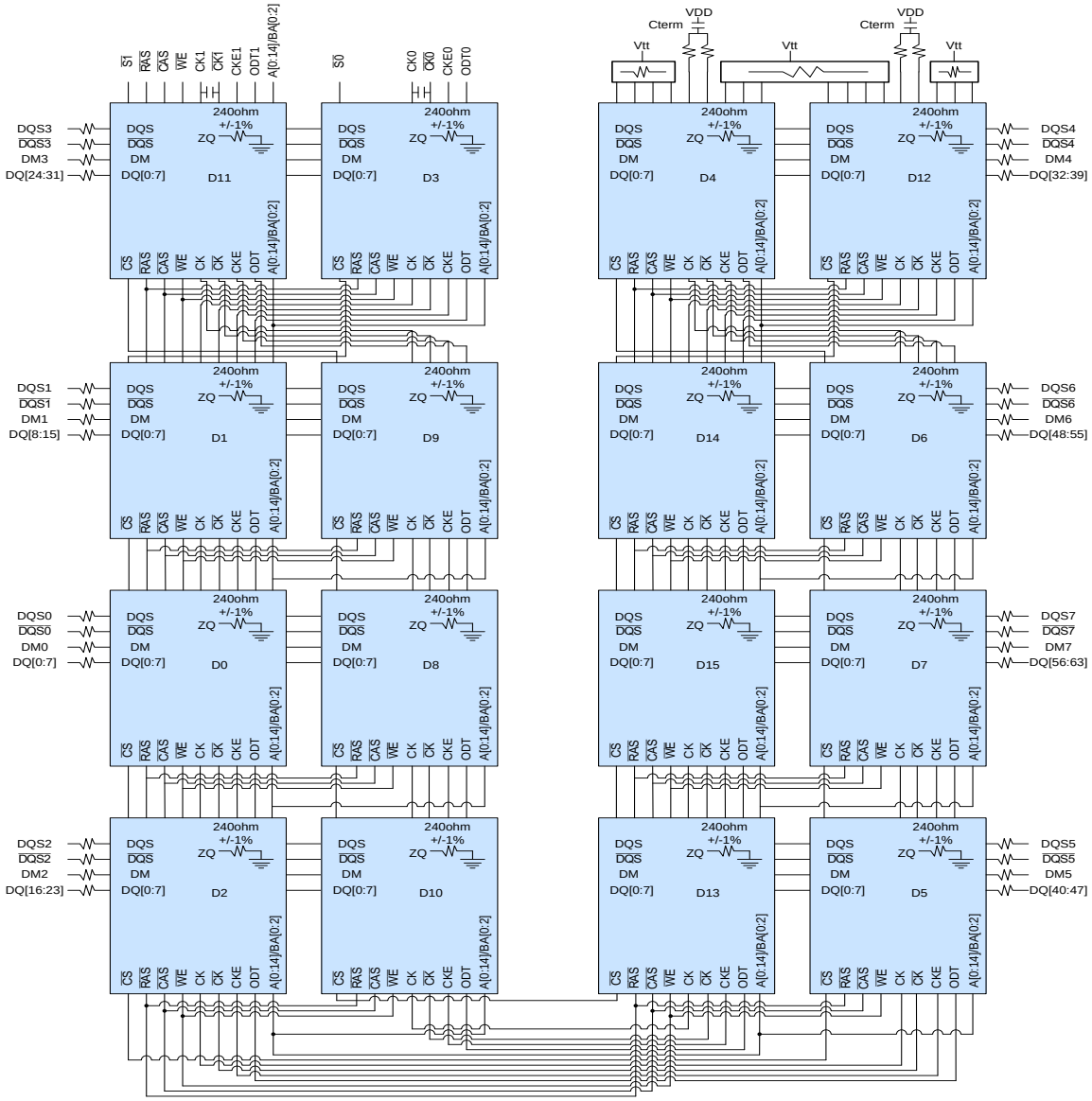



**Notes :**

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240Ω ±1%.
4. One SPD exists per module.

## Functional Block Diagram

[4GB – 2 Ranks, 256Mx8 DDR3 SDRAMs]




**Notes :**

1. DQ wiring may differ from that shown however, DQ, DM, DQS, and $\overline{DQS}$ relationships are maintained as shown.

## Environmental Requirements

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $T_{OPR}$ | Operating Temperature (ambient) | 0 to 85 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C |

**Note**: Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| $V_{DD}$ | Voltage on VDD pins relative to Vss | -0.4 V ~ 1.975 V | V | 1, 3 |
| $V_{DDQ}$ | Voltage on VDDQ pins relative to Vss | -0.4 V ~ 1.975 V | V | 1, 3 |
| $V_{IN}$, $V_{OUT}$ | Voltage on I/O pins relative to Vss | -0.4 V ~ 1.975 V | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1, 2 |

**Note**:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater

## Operating temperature Conditions

| Symbol | Parameter | Rating | Units | Note |
|---|---|---|---|---|
| $T_{OPER}$ | Normal Operating Temperature Range | 0 to 85 | °C | 1, 2 |
| | Extended Temperature Range | 85 to 95 | °C | 1, 3 |

**Note:**
1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

## DC Electrical Characteristics and Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |
| $V_{DDQ}$ | Output Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |

**Note:**
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

## Single-Ended AC and DC Input Levels for Command and Address

| Symbol | Parameter | DDR3-1066 (-BE) | | DDR3-1333 (-CG) | | Units | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| VIH.CA(DC) | DC Input Logic High | Vref + 0.100 | VDD | Vref + 0.100 | VDD | V | 1 |
| VIL.CA(DC) | DC Input Logic Low | VSS | Vref - 0.100 | VSS | Vref - 0.100 | V | 1 |
| VIH.CA(AC) | AC Input Logic High | Vref + 0.175 | Note 2 | Vref + 0.175 | Note 2 | V | 1, 2 |
| VIL.CA(AC) | AC Input Logic Low | Note 2 | Vref - 0.175 | Note 2 | Vref - 0.175 | V | 1, 2 |
| VIH.CA(AC150) | AC Input Logic High | Vref + 0.15 | Note 2 | Vref + 0.15 | Note 2 | V | 1, 2 |
| VIL.CA(AC150) | AC Input Logic Low | Note 2 | Vref - 0.15 | Note 2 | Vref - 0.15 | V | 1, 2 |
| $V_{RefCA(DC)}$ | Reference Voltage for ADD, CMD Inputs | 0.49 x VDD | 0.51 x VDD | 0.49 x VDD | 0.51 x VDD | V | 3, 4 |

**Note:**
1. For input only pins except RESET#. Vref = VrefCA(DC).
2. See “Overshoot and Undershoot Specifications” in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

## Single-Ended AC and DC Input Levels for DQ and DM

| Symbol | Parameter | DDR3-1066 (-BE) | | DDR3-1333 (-CG) | | Units | Note |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| VIH.DQ(DC) | DC Input Logic High | Vref + 0.100 | VDD | Vref + 0.100 | VDD | V | 1 |
| VIL.DQ(DC) | DC Input Logic Low | VSS | Vref - 0.100 | VSS | Vref - 0.100 | V | 1 |
| VIH.DQ(AC) | AC Input Logic High | Vref + 0.175 | Note 2 | Vref + 0.15 | Note 2 | V | 1, 2, 5 |
| VIL.DQ(AC) | AC Input Logic Low | Note 2 | Vref - 0.175 | Note 2 | Vref - 0.15 | V | 1, 2, 5 |
| $V_{RefDQ(DC)}$ | Reference Voltage for DQ, DM Inputs | 0.49 x VDD | 0.51 x VDD | 0.49 x VDD | 0.51 x VDD | V | 3, 4 |

**Note:**
1. For input only pins except RESET#. Vref = VrefDQ(DC).
2. See “Overshoot and Undershoot Specifications” in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. Single-ended swing requirement for DQS, DQS# is 350 mV (peak to peak). Differential swing requirement for DQS - DQS# is 700 mV (peak to peak).

## Operating, Standby, and Refresh Currents

$T_{CASE}$ = 0 °C ~ 85 °C; $V_{DDQ}$ = $V_{DD}$ = 1.5V ± 0.075V [2GB – 1 Rank, 256Mx8 DDR3 SDRAMs]

| Symbol | Parameter/Condition | PC3-8500 (-BE) | PC3-10600 (-CG) | Unit |
|---|---|---|---|---|
| IDD0 | Operating One Bank Active-Precharge Current | 528 | 572 | mA |
| IDD1 | Operating One Bank Active-Read-Precharge Current | 704 | 748 | mA |
| IDD2P0 | Precharge Power-Down Current Slow Exit | 106 | 106 | mA |
| IDD2P1 | Precharge Power-Down Current Fast Exit | 220 | 264 | mA |
| IDD2Q | Precharge Quiet Standby Current | 264 | 308 | mA |
| IDD2N | Precharge Standby Current | 290 | 334 | mA |
| IDD3P | Active Power-Down Current | 334 | 352 | mA |
| IDD3N | Active Standby Current | 396 | 440 | mA |
| IDD4R | Operating Burst Read Current | 1056 | 1188 | mA |
| IDD4W | Operating Burst Write Current | 1012 | 1144 | mA |
| IDD5B | Burst Refresh Current | 1452 | 1496 | mA |
| IDD6 | Self Refresh Current: Normal Temperature Range | 106 | 106 | mA |
| IDD7 | Operating Bank Interleave Read Current | 1848 | 1980 | mA |

## Operating, Standby, and Refresh Currents

$T_{CASE}$ = 0 °C ~ 85 °C; $V_{DDQ}$ = $V_{DD}$ = 1.5V ± 0.075V [4GB – 2 Ranks, 256Mx8 DDR3 SDRAMs]

| Symbol | Parameter/Condition | PC3-8500 (-BE) | PC3-10600 (-CG) | Unit |
|---|---|---|---|---|
| IDD0 | Operating One Bank Active-Precharge Current | 818 | 906 | mA |
| IDD1 | Operating One Bank Active-Read-Precharge Current | 994 | 1082 | mA |
| IDD2P0 | Precharge Power-Down Current Slow Exit | 211 | 211 | mA |
| IDD2P1 | Precharge Power-Down Current Fast Exit | 440 | 528 | mA |
| IDD2Q | Precharge Quiet Standby Current | 528 | 616 | mA |
| IDD2N | Precharge Standby Current | 581 | 669 | mA |
| IDD3P | Active Power-Down Current | 669 | 704 | mA |
| IDD3N | Active Standby Current | 686 | 774 | mA |
| IDD4R | Operating Burst Read Current | 1346 | 1522 | mA |
| IDD4W | Operating Burst Write Current | 1302 | 1478 | mA |
| IDD5B | Burst Refresh Current | 1742 | 1830 | mA |
| IDD6 | Self Refresh Current: Normal Temperature Range | 211 | 211 | mA |
| IDD7 | Operating Bank Interleave Read Current | 2138 | 2314 | mA |

## Speed Bins

### DDR3-1066MHz

| Speed Bin | | | DDR3-1066 | | Unit |
|---|---|---|---|---|---|
| CL-nRCD-nRP | | | 7-7-7 (-BE) | | |
| Parameter | | Symbol | Min | Max | |
| Internal read command to first data | | tAA | 13.125 | 20.000 | ns |
| ACT to internal read or write delay time | | tRCD | 13.125 | - | ns |
| PRE command period | | tRP | 13.125 | - | ns |
| ACT to ACT or REF command period | | tRC | 50.625 | - | ns |
| ACT to PRE command period | | tRAS | 37.500 | 9*tREFI | ns |
| CL=5 | CWL=5 | tCK(AVG) | 3.000 | 3.300 | ns |
| | CWL=6 | tCK(AVG) | Reserved | | ns |
| CL=6 | CWL=5 | tCK(AVG) | 2.500 | 3.300 | ns |
| | CWL=6 | tCK(AVG) | Reserved | | ns |
| CL=7 | CWL=5 | tCK(AVG) | Reserved | | ns |
| | CWL=6 | tCK(AVG) | 1.875 | <2.5 | ns |
| CL=8 | CWL=5 | tCK(AVG) | Reserved | | ns |
| | CWL=6 | tCK(AVG) | 1.875 | <2.5 | ns |
| Supported CL Settings | | | 5,6,7,8 | | nCK |
| Supported CWL Settings | | | 5,6 | | nCK |

## DDR3-1333MHz

| Speed Bin | | | DDR3-1333 | | Unit |
|---|---|---|---|---|---|
| CL-nRCD-nRP | | | 9-9-9 (-CG) | | Unit |
| Parameter | | Symbol | Min | Max | |
| Internal read command to first data | | tAA | 13.125 | 20.000 | ns |
| ACT to internal read or write delay time | | tRCD | 13.125 | - | ns |
| PRE command period | | tRP | 13.125 | - | ns |
| ACT to ACT or REF command period | | tRC | 49.125 | - | ns |
| ACT to PRE command period | | tRAS | 36.000 | 9*tREFI | ns |
| CL=5 | CWL=5 | tCK(AVG) | 3.000 | 3.300 | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=6 | CWL=5 | tCK(AVG) | 2.500 | 3.300 | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=7 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | 1.875* | <2.5* | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=8 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | 1.875 | <2.5 | ns |
| | CWL=7 | tCK(AVG) | Reserved | Reserved | ns |
| CL=9 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | 1.500 | <1.875 | ns |
| CL=10 | CWL=5 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=6 | tCK(AVG) | Reserved | Reserved | ns |
| | CWL=7 | tCK(AVG) | 1.500* | <1.875* | ns |
| Supported CL Settings | | | 5,6,7,8,9,(10) | | nCK |
| FtrSupported CWL Settings | | | 5,6,7 | | nCK |
| *: Optional | | | | | |

## AC Timing Specifications for DDR3 SDRAM Devices Used on Module (1066MHz)

| Parameter | Symbol | DDR3-1066 | | Units | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Clock Timing | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_OFF) | 8 | - | ns | |
| Average Clock Period | tCK(avg) | Refer to "Standard Speed Bins) | | ps | |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | Min.: tCK(avg)min + tJIT(per)min<br>Max.: tCK(avg)max + tJIT(per)max | | ps | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | - | tCK(avg) | |
| Absolute clock LOW pulse width | tCL(abs) | 0.43 | - | tCK(avg) | |
| Clock Period Jitter | JIT(per) | -90 | 90 | ps | |
| Clock Period Jitter during DLL locking period | JIT(per, lck) | -80 | 80 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | 180 | 180 | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | JIT(cc, lck) | 160 | 160 | ps | |
| Duty Cycle Jitter | tJIT(duty) | - | - | ps | |
| Cumulative error across 2 cycles | tERR(2per) | -132 | 132 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -157 | 157 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -175 | 175 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -188 | 188 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -200 | 200 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -209 | 209 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -217 | 217 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -224 | 224 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -231 | 231 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -237 | 237 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -242 | 242 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper) | tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min<br>tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max | | ps | |
| Data Timing | | | | | |
| DQS, DQS# to DQ skew, per group, per access | tDQSQ | - | 150 | ps | |
| DQ output hold time from DQS, DQS# | tQH | 0.38 | - | tCK(avg) | |
| DQ low-impedance time from CK, CK# | tLZ(DQ) | -600 | 300 | ps | |
| DQ high impedance time from CK, CK# | tHZ(DQ) | - | 300 | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base) AC175 | 25 | | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base) AC150 | 75 | | ps | |
| Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels | tDH(base) DC100 | 100 | | ps | |
| DQ and DM Input pulse width for each input | tDIPW | 490 | | ps | |
| Data Strobe Timing | | | | | |
| DQS,DQS# differential READ Preamble | tRPRE | 0.9 | Note 19 | tCK(avg) | |
| DQS, DQS# differential READ Postamble | tRPST | 0.3 | Note 11 | tCK(avg) | |
| DQS, DQS# differential output high time | tQSH | 0.38 | - | tCK(avg) | |
| DQS, DQS# differential output low time | tQSL | 0.38 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Preamble | tWPRE | 0.9 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Postamble | tWPST | 0.3 | - | tCK(avg) | |
| DQS, DQS# rising edge output access time from rising CK, CK# | tDQSCK | -300 | 300 | tCK(avg) | |
| DQS and DQS# low-impedance time (Referenced from RL - 1) | tLZ(DQS) | -600 | 300 | tCK(avg) | |
| DQS and DQS# high-impedance time (Referenced from RL + BL/2) | tHZ(DQS) | - | 300 | tCK(avg) | |
| DQS, DQS# differential input low pulse width | tDQSL | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# differential input high pulse width | tDQSH | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# rising edge to CK, CK# rising edge | tDQSS | -0.25 | 0.25 | tCK(avg) | |
| DQS, DQS# falling edge setup time to CK, CK# rising edge | tDSS | 0.2 | - | tCK(avg) | |
| DQS, DQS# falling edge hold time from CK, CK# rising edge | tDSH | 0.2 | - | tCK(avg) | |
| Command and Address Timing | | | | | |
| DLL locking time | tDLLK | 512 | - | nCK | |

| | | | | | |
|---|---|---|---|---|---|
| Internal READ Command to PRECHARGE Command delay | tRTP | tRTPmin.: max(4nCK, 7.5ns)<br>tRTPmax.: - | | | |
| Delay from start of internal write transaction to internal read command | tWTR | tWTRmin.: max(4nCK, 7.5ns)<br>tWTRmax.: | | | |
| WRITE recovery time | tWR | 15 | - | ns | |
| Mode Register Set command cycle time | tMRD | 4 | - | nCK | |
| Mode Register Set command update delay | tMOD | tMODmin.: max(12nCK, 15ns)<br>tMODmax.: | | | |
| ACT to internal read or write delay time | tRCD | | | | |
| PRE command period | tRP | | | | |
| ACT to ACT or REF command period | tRC | | | | |
| CAS# to CAS# command delay | tCCD | 4 | - | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | WR + roundup(tRP / tCK(avg)) | | nCK | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | nCK | |
| ACTIVE to PRECHARGE command period | tRAS | Standard Speed Bins | | | |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | max(4nCK, 7.5ns) | - | | |
| ACTIVE to ACTIVE command period for 2KB page size | tRRD | tRRDmin.: max(4nCK, 10ns)<br>tRRDmax.: | | | |
| Four activate window for 1KB page size | tFAW | 37.5 | - | ns | |
| Four activate window for 2KB page size | tFAW | 50 | - | ns | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 125 | - | ps | |
| Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 200 | - | ps | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) AC150 | 125+150 | - | ps | |
| Control and Address Input pulse width for each input | tIPW | 780 | - | ps | |
| Calibration Timing | | | | | |
| Power-up and RESET calibration time | tZQinit | 512 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 256 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 64 | - | nCK | |
| Reset Timing | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | tXPRmin.: max(5nCK, tRFC(min) + 10ns)<br>tXPRmax.: - | | | |
| Self Refresh Timings | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | tXSmin.: max(5nCK, tRFC(min) + 10ns)<br>tXSmax.: - | | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tXSDLLmin.: tDLLK(min)<br>tXSDLLmax.: - | | nCK | |
| Minimum CKE low width for Self Refresh entry to exit timing | tCKESR | tCKESRmin.: tCKE(min) + 1 nCK<br>tCKESRmax.: - | | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | tCKSREmin.: max(5 nCK, 10 ns)<br>tCKSREmax.: - | | | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | tCKSRXmin.: max(5 nCK, 10 ns)<br>tCKSRXmax.: - | | | |
| Power Down Timings | | | | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | tXPmin.: max(3nCK, 7.5ns)<br>tXPmax.: - | | | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | tXPDLLmin.: max(10nCK, 24ns)<br>tXPDLLmax.: - | | | |
| CKE minimum pulse width | tCKE | tCKEmin.: max(3nCK 5.625ns)<br>tCKEmax.: - | | | |
| Command pass disable delay | tCPDED | tCPDEDmin.: 1<br>tCPDEDmin.: - | | nCK | |
| Power Down Entry to Exit Timing | tPD | tPDmin.: tCKE(min)<br>tPDmax.: 9*tREFI | | | |
| Timing of ACT command to Power Down entry | tACTPDEN | tACTPDENmin.: 1<br>tACTPDENmax.: - | | nCK | |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | tPRPDENmin.: 1<br>tPRPDENmax.: - | | nCK | |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | tRDPDENmin.: RL+4+1<br>tRDPDENmax.: - | | nCK | |

| | | | | | |
|---|---|---|---|---|---|
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | tWRPDENmin.: WL + 4 + (tWR / tCK(avg)) tWRPDENmax.: - | | nCK | |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | tWRAPDENmin.: WL+4+WR+1 tWRAPDENmax.: - | | nCK | |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPDEN | tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: - | | nCK | |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAPDEN | tWRAPDENmin.: WL + 2 +WR + 1 tWRAPDENmax.: - | | nCK | |
| Timing of REF command to Power Down entry | tREFPDEN | tREFPDENmin.: 1 tREFPDENmax.: - | | nCK | |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMRSPDENmin.: tMOD(min) tMRSPDENmax.: - | | | |
| ODT Timings | | | | | |
| ODT high time without write command or with write command and BC4 | ODTH4 | ODTH4min.: 4 ODTH4max.: - | | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | ODTH8min.: 6 ODTH8max.: - | | nCK | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONPD | 2 | 8.5 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFPD | 2 | 8.5 | ns | |
| RTT turn-on | tAON | -300 | 300 | ps | |
| RTT_Nom and RTT_WR turn-off time from ODTLoff reference | tAOF | 0.3 | 0.7 | tCK(avg) | |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | tCK(avg) | |
| Write Leveling Timings | | | | | |
| First DQS/DQS# rising edge after write leveling mode is programmed | tWLMRD | 40 | - | nCK | |
| DQS/DQS# delay after write leveling mode is programmed | tWLDQSEN | 25 | - | nCK | |
| Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing | tWLS | 245 | - | ps | |
| Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing | tWLH | 245 | - | ps | |
| Write leveling output delay | tWLO | 0 | 9 | ns | |
| Write leveling output error | tWLOE | 0 | 2 | ns | |

## AC Timing Specifications for DDR3 SDRAM Devices Used on Module (1333MHz)

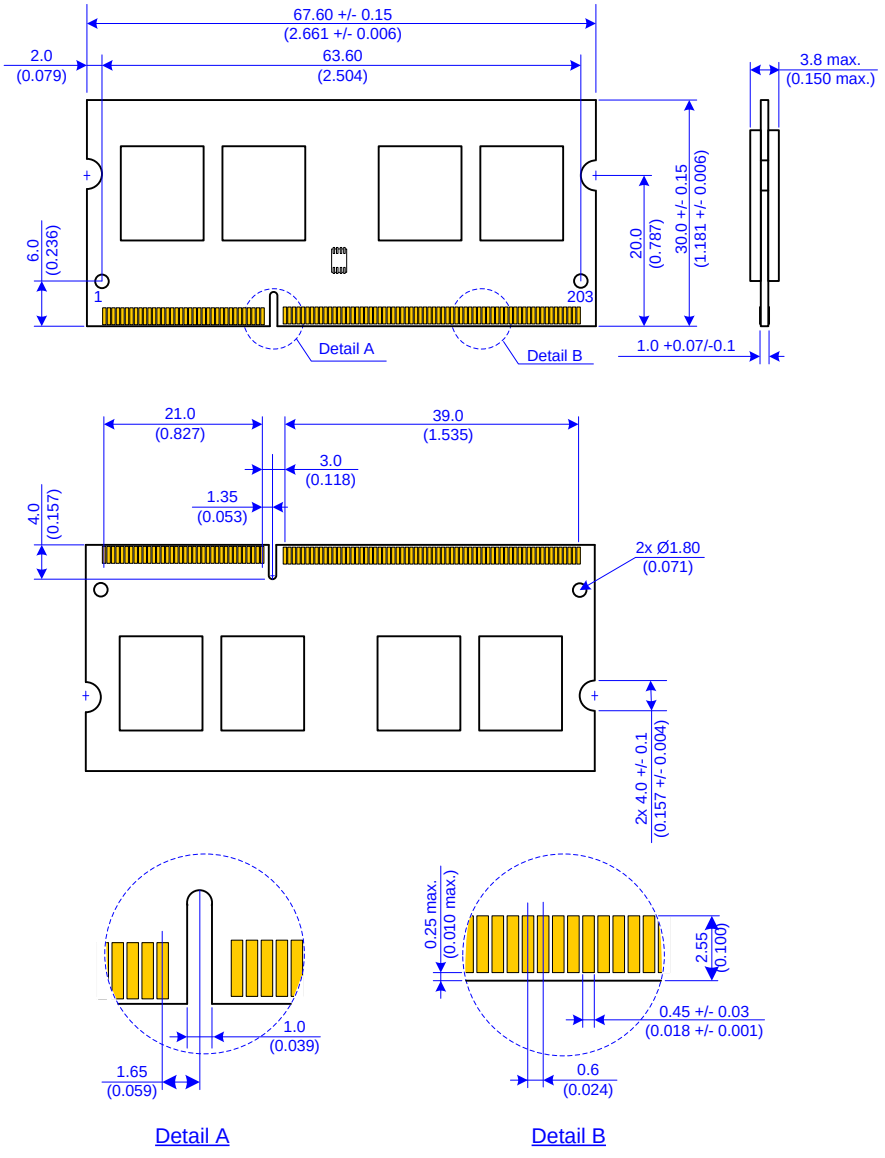
| Parameter | Symbol | DDR3-1333 | | Units | Notes |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Clock Timing | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK (DLL_OFF) | 8 | - | ns | |
| Average Clock Period | tCK(avg) | Refer to "Standard Speed Bins) | | ps | |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | tCK(avg) | |
| Absolute Clock Period | tCK(abs) | Min.: tCK(avg)min + tJIT(per)min<br>Max.: tCK(avg)max + tJIT(per)max | | ps | |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | - | tCK(avg) | |
| Absolute clock LOW pulse width | tCL(abs) | 0.43 | - | tCK(avg) | |
| Clock Period Jitter | JIT(per) | -80 | 80 | ps | |
| Clock Period Jitter during DLL locking period | JIT(per, lck) | -70 | 70 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | 160 | 160 | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | JIT(cc, lck) | 140 | 140 | ps | |
| Duty Cycle Jitter | tJIT(duty) | - | - | ps | |
| Cumulative error across 2 cycles | tERR(2per) | -118 | 118 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | -140 | 140 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | -155 | 155 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | -168 | 168 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | -177 | 177 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | -186 | 186 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | -193 | 193 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | -200 | 200 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | -205 | 205 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | -210 | 210 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | -215 | 215 | ps | |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper) | tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min<br>tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max | | ps | |
| Data Timing | | | | | |
| DQS, DQS# to DQ skew, per group, per access | tDQSQ | - | 125 | ps | |
| DQ output hold time from DQS, DQS# | tQH | 0.38 | - | tCK(avg) | |
| DQ low-impedance time from CK, CK# | tLZ(DQ) | -500 | 250 | ps | |
| DQ high impedance time from CK, CK# | tHZ(DQ) | - | 250 | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base)<br>AC175 | - | | ps | |
| Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | tDS(base)<br>AC150 | 30 | | ps | |
| Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels | tDH(base)<br>DC100 | 65 | | ps | |
| DQ and DM Input pulse width for each input | tDIPW | 400 | - | ps | |
| Data Strobe Timing | | | | | |
| DQS,DQS# differential READ Preamble | tRPRE | 0.9 | Note 19 | tCK(avg) | |
| DQS, DQS# differential READ Postamble | tRPST | 0.3 | Note 11 | tCK(avg) | |
| DQS, DQS# differential output high time | tQSH | 0.4 | - | tCK(avg) | |
| DQS, DQS# differential output low time | tQSL | 0.4 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Preamble | tWPRE | 0.9 | - | tCK(avg) | |
| DQS, DQS# differential WRITE Postamble | tWPST | 0.3 | - | tCK(avg) | |
| DQS, DQS# rising edge output access time from rising CK, CK# | tDQSCK | -255 | 255 | tCK(avg) | |
| DQS and DQS# low-impedance time<br>(Referenced from RL - 1) | tLZ(DQS) | -500 | 250 | tCK(avg) | |
| DQS and DQS# high-impedance time<br>(Referenced from RL + BL/2) | tHZ(DQS) | - | 250 | tCK(avg) | |
| DQS, DQS# differential input low pulse width | tDQSL | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# differential input high pulse width | tDQSH | 0.45 | 0.55 | tCK(avg) | |
| DQS, DQS# rising edge to CK, CK# rising edge | tDQSS | -0.25 | 0.25 | tCK(avg) | |
| DQS, DQS# falling edge setup time to CK, CK# rising edge | tDSS | 0.2 | - | tCK(avg) | |
| DQS, DQS# falling edge hold time from CK, CK# rising edge | tDSH | 0.2 | - | tCK(avg) | |
| Command and Address Timing | | | | | |
| DLL locking time | tDLLK | 512 | - | nCK | |

| | | | | | |
|---|---|---|---|---|---|
| Internal READ Command to PRECHARGE Command delay | tRTP | tRTPmin.: max(4nCK, 7.5ns)<br>tRTPmax.: - | | | |
| Delay from start of internal write transaction to internal read command | tWTR | tWTRmin.: max(4nCK, 7.5ns)<br>tWTRmax.: | | | |
| WRITE recovery time | tWR | 15 | - | ns | |
| Mode Register Set command cycle time | tMRD | 4 | - | nCK | |
| Mode Register Set command update delay | tMOD | tMODmin.: max(12nCK, 15ns)<br>tMODmax.: | | | |
| ACT to internal read or write delay time | tRCD | | | | |
| PRE command period | tRP | | | | |
| ACT to ACT or REF command period | tRC | | | | |
| CAS# to CAS# command delay | tCCD | 4 | | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | WR + roundup(tRP / tCK(avg)) | | nCK | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | nCK | |
| ACTIVE to PRECHARGE command period | tRAS | Standard Speed Bins | | | |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | tRRDmin.: max(4nCK, 6ns)<br>tRRDmax.: | | | |
| ACTIVE to ACTIVE command period for 2KB page size | tRRD | tRRDmin.: max(4nCK, 7.5ns)<br>tRRDmax.: | | | |
| Four activate window for 1KB page size | tFAW | 30 | 0 | ns | |
| Four activate window for 2KB page size | tFAW | 45 | 0 | ns | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) | 65 | - | ps | |
| Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels | tIH(base) | 140 | - | ps | |
| Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels | tIS(base) AC150 | 65+125 | - | ps | |
| Control and Address Input pulse width for each input | tIPW | 620 | - | ps | |
| Calibration Timing | | | | | |
| Power-up and RESET calibration time | tZQinit | 512 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 256 | - | nCK | |
| Normal operation Short calibration time | tZQCS | 64 | - | nCK | |
| Reset Timing | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | tXPRmin.: max(5nCK, tRFC(min) + 10ns)<br>tXPRmax.: - | | | |
| Self Refresh Timings | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | tXSmin.: max(5nCK, tRFC(min) + 10ns)<br>tXSmax.: - | | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tXSDLLmin.: tDLLK(min)<br>tXSDLLmax.: - | | nCK | |
| Minimum CKE low width for Self Refresh entry to exit timing | tCKESR | tCKESRmin.: tCKE(min) + 1 nCK<br>tCKESRmax.: - | | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | tCKSREmin.: max(5 nCK, 10 ns)<br>tCKSREmax.: - | | | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | tCKSRXmin.: max(5 nCK, 10 ns)<br>tCKSRXmax.: - | | | |
| Power Down Timings | | | | | |
| Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | tXPmin.: max(3nCK, 6ns)<br>tXPmax.: - | | | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | tXPDLLmin.: max(10nCK, 24ns)<br>tXPDLLmax.: - | | | |
| CKE minimum pulse width | tCKE | tCKEmin.: max(3nCK ,5.625ns)<br>tCKEmax.: - | | | |
| Command pass disable delay | tCPDED | tCPDEDmin.: 1<br>tCPDEDmin.: - | | nCK | |
| Power Down Entry to Exit Timing | tPD | tPDmin.: tCKE(min)<br>tPDmax.: 9*tREFI | | | |
| Timing of ACT command to Power Down entry | tACTPDEN | tACTPDENmin.: 1<br>tACTPDENmax.: - | | nCK | |
| Timing of PRE or PREA command to Power Down entry | tPRPDEN | tPRPDENmin.: 1<br>tPRPDENmax.: - | | nCK | |

| | | | | | |
|---|---|---|---|---|---|
| Timing of RD/RDA command to Power Down entry | tRDPDEN | tRDPDENmin.: RL+4+1<br>tRDPDENmax.: - | | nCK | |
| Timing of WR command to Power Down entry<br>(BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | tWRPDENmin.: WL + 4 + (tWR / tCK(avg))<br>tWRPDENmax.: - | | nCK | |
| Timing of WRA command to Power Down entry<br>(BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | tWRAPDENmin.: WL+4+WR+1<br>tWRAPDENmax.: - | | nCK | |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPDEN | tWRPDENmin.: WL + 2 + (tWR / tCK(avg))tWRPDENmax.: - | | nCK | |
| Timing of WRA command to Power Down entry<br>(BC4MRS) | tWRAPDEN | tWRAPDENmin.: WL + 2 +WR + 1<br>tWRAPDENmax.: - | | nCK | |
| Timing of REF command to Power Down entry | tREFPDEN | tREFPDENmin.: 1<br>tREFPDENmax.: - | | nCK | |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMRSPDENmin.: tMOD(min)<br>tMRSPDENmax.: - | | | |
| ODT Timings | | | | | |
| ODT high time without write command or<br>with write command and BC4 | ODTH4 | ODTH4min.: 4<br>ODTH4max.: - | | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | ODTH8min.: 6<br>ODTH8max.: - | | nCK | |
| Asynchronous RTT turn-on delay<br>(Power-Down with DLL frozen) | tAONPD | 2 | 8.5 | ns | |
| Asynchronous RTT turn-off delay<br>(Power-Down with DLL frozen) | tAOFPD | 2 | 8.5 | ns | |
| RTT turn-on | tAON | -250 | 250 | ps | |
| RTT_Nom and RTT_WR turn-off time<br>from ODTLoff reference | tAOF | 0.3 | 0.7 | tCK(avg) | |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | tCK(avg) | |
| Write Leveling Timings | | | | | |
| First DQS/DQS# rising edge after<br>write leveling mode is programmed | tWLMRD | 40 | - | nCK | |
| DQS/DQS# delay after write leveling mode is programmed | tWLDQSEN | 25 | - | nCK | |
| Write leveling setup time from rising CK, CK#<br>crossing to rising DQS, DQS# crossing | tWLS | 195 | - | ps | |
| Write leveling hold time from rising DQS, DQS#<br>crossing to rising CK, CK# crossing | tWLH | 195 | - | ps | |
| Write leveling output delay | tWLO | 0 | 9 | ns | |
| Write leveling output error | tWLOE | 0 | 2 | ns | |

## Package Dimensions

[2GB – 1 Rank, 256Mx8 DDR3 SDRAMs]

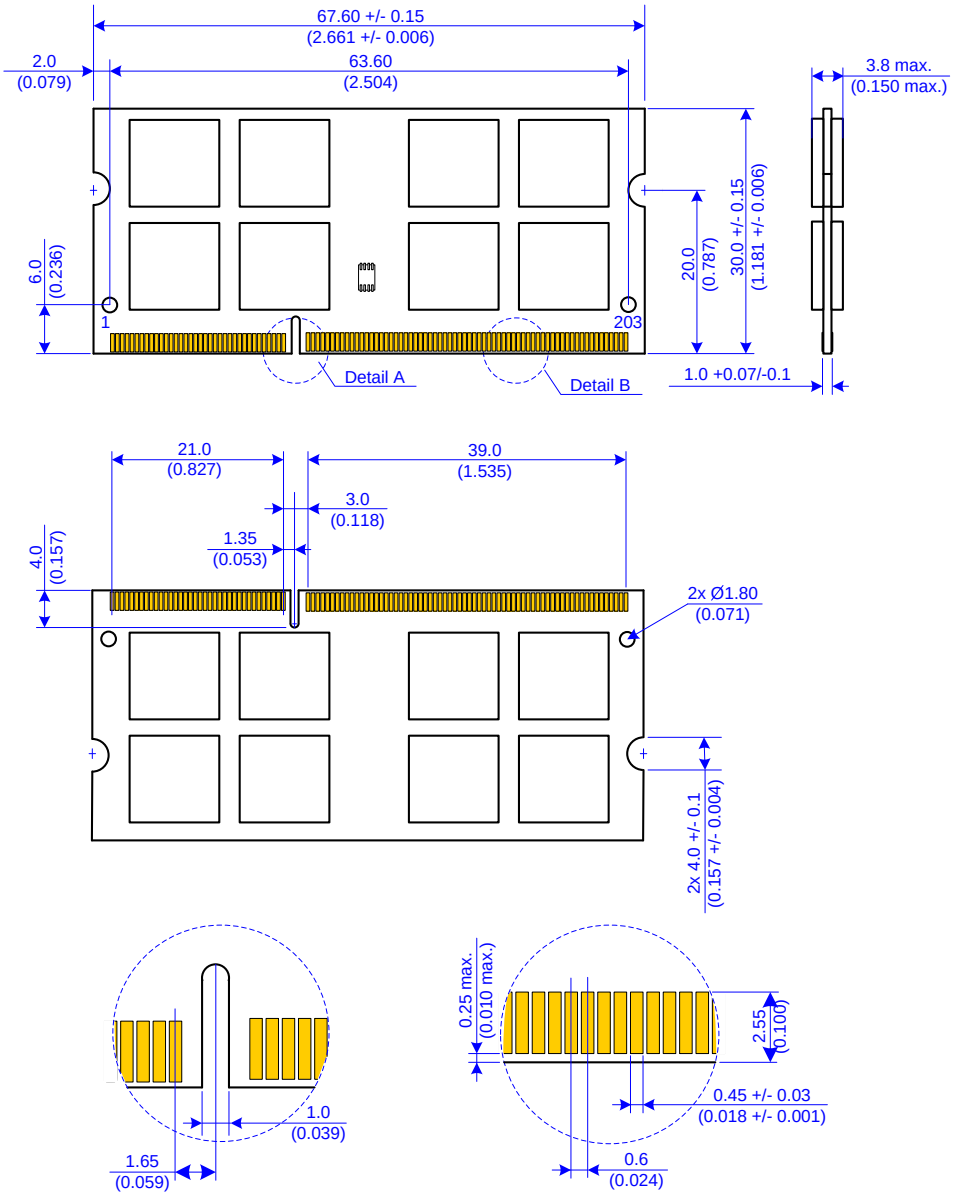



Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

## Package Dimensions

[4GB – 2 Ranks, 256Mx8 DDR3 SDRAMs]




Detail A Detail B

Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

## Revision Log

| Rev | Date | Modification |
|---|---|---|
| 0.1 | 02/2011 | Preliminary Release |
| 1.0 | 03/2011 | Official Release |