200 pin Unbuffered DDR2 SO-DIMM

Based on 2x128Mx8 (Stacking) DDR2 SDRAM

Features

- 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- 256Mx64 Unbuffered DDR2 SO-DIMM based on 2 ranks of 128Mx8 DDR2 SDRAM device.
- Performance:

	PC2-4200	PC2-5300	PC2-6400	Unit
Speed Sort	37B	3C	25D	
DIMM $\overline{CAS}$ Latency	4	5	6	
f_{CK} Clock Frequency	266	333	400	MHz
t_{CK} Clock Cycle	3.75	3	2.5	ns
f_{DQ} DQ Burst Frequency	533	667	800	MHz

- Intended for 266MHz, 333MHz and 400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 3, 4, 5 (-37B/-3C); 4, 5, 6 (-25D)
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 71-ball stacked BGA Package
- RoHS Compliance
- Halogen free - NT2GTT64U88B0US

Description

NT2GTT64U88B0UN and NT2GTT64U88B0US are unbuffered 200-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as two ranks of 256Mx64 high-speed memory array. Modules use eight 256Mx8 (2x128Mx8) 71-ball stacked BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 2.66" long space-saving footprint.

The DIMM is intended for use in applications operating up to 266MHz (333MHz or 400MHz) clock speeds and achieves high-speed data transfer rates of up to 533MHz (667MHz or 800 MHz). Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Power	Leads	Note
NT2GTT64U88B0UN –37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)	256Mx64	1.8V	Gold	Green
NT2GTT64U88B0UN –3C	DDR2-667	PC2-5300	333MHz (3.0ns @ CL = 5)				
NT2GTT64U88B0US –3C							
NT2GTT64U88B0UN –25D	DDR2-800	PC2-6400	400MHz (2.5ns @ CL =6)				
NT2GTT64U88B0US –25D							

Pin Description

CK0-CK1 $\overline{CK0}$-$\overline{CK1}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	$\overline{DQS0}$-$\overline{DQS7}$	Differential data strobes
$\overline{CAS}$	Column Address Strobe	DM0-DM7	Input Data Masks
$\overline{WE}$	Write Enable	V_{DD}	Power (1.8V)
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	V_{REF}	Ref. Voltage for SSTL_18 inputs
A0-A9, A11-A13	Address Inputs	V_{DDSPD}	Serial EEPROM positive power supply
A10/AP	Column Address Input/Auto-precharge	V_{SS}	Ground
BA0, BA1	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
ODT0, ODT1	Active termination control lines	SDA	Serial Presence Detect Data input/output
NC	No Connect	SA0, SA1	Serial Presence Detect Address Inputs

Pinout

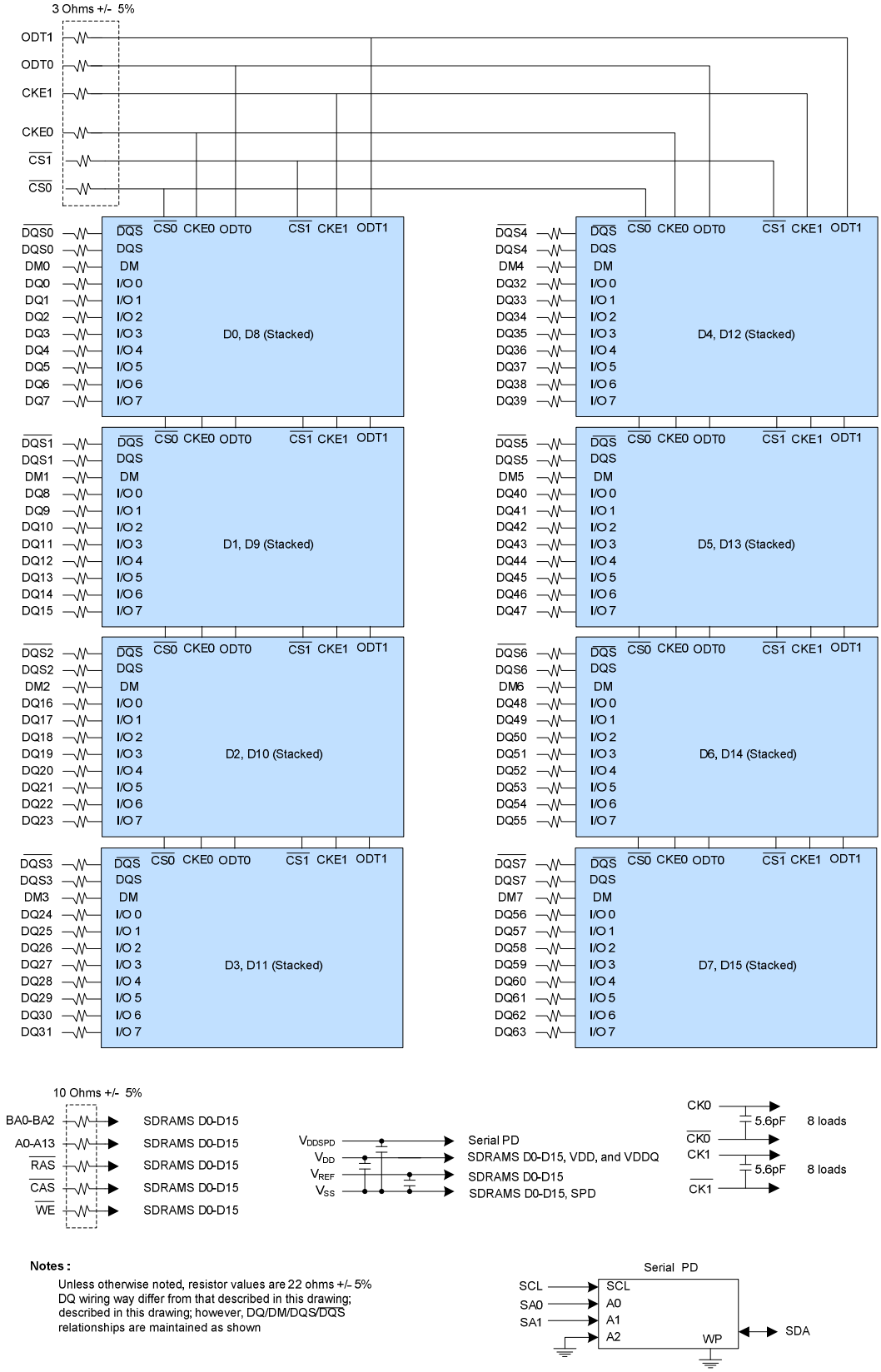
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	$\overline{WE}$	110	$\overline{CS0}$	159	DQ49	160	DQ53
11	$\overline{DQS0}$	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	$\overline{CS1}$	116	A13	165	V_{SS}	166	$\overline{CK1}$
17	DQ2	18	V_{SS}	67	DM3	68	$\overline{DQS3}$	117	V_{DD}	118	V_{DD}	167	$\overline{DQS6}$	168	V_{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1	120	NC	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	$\overline{DQS1}$	30	CK0	79	CKE0	80	CKE1	129	$\overline{DQS4}$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK0}$	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	NC	84	NC	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	BA2	86	NC	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS7}$
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	$\overline{DQS5}$	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS2}$	50	NC	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DDSPD}	200	SA1

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0-CK1, $\overline{CK0}$-$\overline{CK1}$	(SSTL)	Cross Point	The system clock inputs. All the DDR2 SDRAM address and control inputs are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
VREF	Supply		Reference voltage for SSTL-18 inputs.
ODT0, ODT1	Input	Active High	On-Die Termination control signals.
BA0 - BA2	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 – A13 defines the column address when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS7 $\overline{DQS0}$ – $\overline{DQS7}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data.
DM0 – DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

(2GB, 2Ranks, x8 DDR2 SDRAMs)



Notes :

Unless otherwise noted, resistor values are 22 ohms +/- 5%
DQ wiring way differ from that described in this drawing; described in this drawing; however, DQ/DM/DQS/$\overline{DQS}$ relationships are maintained as shown

Serial Presence Detect (Part 1 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		PC2-4200	PC2-5300	PC2-6400	PC2-4200	PC2-5300	PC2-6400	
		-37B	-3C	-25D	-37B	-3C	-25D	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2			08			
3	Number of Row Addresses on Assembly	15			0E			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Ranks	2 rank, Height=30mm			71			
6	Data Width of Assembly	64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at CL=5	3.75ns	3ns	2.5ns	3D	30	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	±0.5ns	±0.45ns	±0.4ns	50	45	40	
11	DIMM Configuration Type	Non parity/ECC			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDR2 SDRAM Width	X8			08			
14	Error Checking DDR2 SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8			08			
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	5,4,3		6,5,4	38		70	
19	DIMM Mechanical Characteristics	<3.80mm			01			
20	DDR2 SDRAM DIMM Type Information	Regular SODIMM (67.6mm)			04			
21	DDR2 SDRAM Module Attributes:	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver /50ohm ODT/ PASR			07			
23	Minimum Clock Cycle at CL=4	3.75ns		3ns	3D		30	
24	Maximum Data Access Time from Clock at CL=4	±0.5ns		±0.45ns	50		45	
25	Minimum Clock Cycle Time at CL=3	5.0ns		3.75ns	50		3D	
26	Maximum Data Access Time from Clock at CL=3	±0.6ns		±0.5ns	60		50	
27	Minimum Row Precharge Time (t_{RP})	15ns			3C			
28	Minimum Row Active to Row Active delay (t_{RRD})	7.5ns			1E			
29	Minimum RAS to CAS delay (t_{RCD})	15ns			3C			
30	Minimum RAS Pulse Width (t_{RAS})	45.0			2D			
31	Module Bank Density	1GB			01			
32	Address and Command Setup Time Before Clock (t_{IS})	0.25ns	0.2ns	0.17ns	25	20	17	
33	Address and Command Hold Time After Clock (t_{IH})	0.375ns	0.275ns	0.25	37	27	25	
34	Data Input Setup Time Before Clock (t_{DS})	0.10ns		0.05ns	10		05	
35	Data Input Hold Time After Clock (t_{DH})	0.225ns	0.175ns	0.12ns	22	17	12	
36	Write Recovery Time (t_{WR})	15.0ns			3C			
37	Internal Write to Read Command delay (t_{WTR})	7.5ns			1E			
38	Internal Read to Precharge delay (t_{RTP})	7.5ns			1E			
39	Reserved	Undefined			00			
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	The number below a decimal point of tRC=0 and tRFC=5, tRFC is less than 256ns			06		00	
41	Minimum Core Cycle Time (t_{RC})	60.0ns			3C			

Serial Presence Detect (Part 2 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		PC2-4200	PC2-5300	PC2-6400	PC2-4200	PC2-5300	PC2-6400	
		-37B	-3C	-25D	-37B	-3C	-25D	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	127.5ns		105ns	7F		69	
43	Maximum Clock Cycle Time (t_{CK})	8.0ns			80			
44	Max. DQS-DQ Skew Factor (t_{DQS})	0.30ns	0.24ns	0.2ns	1E	18	14	
45	Read Data Hold Skew Factor (t_{QHS})	0.40ns	0.34ns	0.30ns	28	22	1E	
46-61	Reserved	Undefined			00			
62	SPD Revision	1.2			12			
63	Checksum for Byte 0-62	Checksum data			6D	29	D7	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-91	Module Part Number	Module Part Number in ASCII			--			1
92-255	Reserved	Undefined			--			

Note1: NT2GTT64U88B0UN-37B ➔ 4E5432475454363455383842305 54E2D333742
NT2GTT64U88B0UN-3C ➔ 4E5432475454363455383842305 54E2D334320
NT2GTT64U88B0US-3C ➔ 4E5432475454363455383842305 5532D334320
NT2GTT64U88B0UN-25D ➔ 4E5432475454363455383842305 54E2D323544
NT2GTT64U88B0US-25D ➔ 4E5432475454363455383842305 5532D323544

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to +2.3	V
V_{DD}	Voltage on VDD pins relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ pins relative to Vss	-0.5 to +2.3	V
V_{DDL}	Voltage on VDDL pins relative to Vss	-0.5 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating temperature Conditions

Symbol	Parameter	Rating	Units
T_{OPR}	Operating Temperature (Ambient)	0 to 65	℃

Note: Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability
Barometric pressure up to 9850 ft.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units	Notes
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	DLL Supply Voltage	1.7	1.8	1.9	V	1
VDDQ	Output Supply Voltage	1.7	1.8	1.9	V	1
VREF	Input Reference Voltage	0.49VDDQ	0.50VDDQ	0.51VDDQ	V	1, 2
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	3

Note:
1. Inputs are not recognized as valid until VREF stabilizes.
2. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
3. VTT of transmitting device must track VREF of receiving device.

Input AC/DC logic level

Symbol	Parameter	PC2-4200 -37B		PC2-5300 -3C		PC2-6400 -25D		Units	Notes
		Min	Max	Min	Max	Min	Max		
VIH (AC)	Input High (Logic1) Voltage	VREF + 0.250	-	VREF + 0.200	-	VREF + 0.200	-	V	1
VIL (AC)	Input Low (Logic0) Voltage	-	VREF - 0.250	-	VREF - 0.200	-	VREF - 0.200	V	1
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.125	VDDQ + 0.3	VREF + 0.125	VDDQ + 0.3	VREF + 0.125	VDDQ + 0.3	V	
VIL (DC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.125	-0.3	VREF - 0.125	-0.3	VREF - 0.125	V	1

Operating, Standby, and Refresh Currents

T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = V_{DD} = 1.8V ± 0.1V [2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-4200 (-37B)	PC2-5300 (-3C)	PC2-6400 (-25D)	Unit
IDD0	Operating Current: one bank; active/precharge; t_{RC} = $t_{RC\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1440	1560	1680	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; t_{RC} = $t_{RC\ (MIN)}$; CL= 4; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	1560	1680	1840	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	320	320	320	mA
IDD2N	Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle	1040	1120	1280	mA
IDD2Q	Precharge Quiet Stand by Current	960	1040	1200	mA
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; Fast PDN Exit MRS(12) = 0mA	720	800	880	mA
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; Slow PDN Exit MRS(12) = 1mA	320	320	320	mA
IDD3N	Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; t_{RC} = $t_{RAS\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1120	1200	1280	mA
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL= 4; t_{CK} = $t_{CK\ (MIN)}$	1920	2040	2240	mA
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 4; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA	1760	1880	2080	mA
IDD5	Auto-Refresh Current: t_{RC} = $t_{RFC\ (MIN)}$	2320	2520	2720	mA
IDD6	Self-Refresh Current: CKE ≤ 0.2V	320	320	320	mA
IDD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = $t_{RC\ (min)}$; I_{OUT} = 0mA.	2720	3160	3440	mA

Note: Module IDD was calculated from component IDD. It may different from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-4200		PC2-5300		PC2-6400		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tCK	Clock Cycle Time	3750	8000					ps
	Clock Cycle Time (Average)			3000	8000	2500	8000	ps
tCH	CK high-level width	0.45	0.55	0.48	0.52	0.48	0.52	tCK
tCL	CK low-level width	0.45	0.55	0.48	0.52	0.48	0.52	tCK
WL	Write command to DQS associated clock edge	RL-1		RL-1		RL-1		tCK
tDQSS	Write command to 1st DQS latching transition	-0.25	0.25	-0.25	+0.25	-0.25	+0.25	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	0.35	-	tCK
tWPRE	Write preamble	0.35	-	0.35	-	0.35	-	tCK
tWPST	Write postamble	0.4	0.6	0.40	0.60	0.40	0.60	tCK
tIS	Address and control input setup time	250	-	200	-	175	-	ps
tIH	Address and control input hold time	375	-	275	-	250	-	ps
tIPW	Input pulse width	0.6	-	0.6	-	0.6	-	tCK
tDS	DQ and DM input setup time(differential data strobe)	100	-	100	-	50	-	ps
tDH	DQ and DM input hold time(differential data strobe)	225	-	175	-	125	-	ps
tDIPW	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	tCK
tAC	DQ output access time from CK/$\overline{CK}$	-500	500	-450	450	-400	400	ps
tDQSCK	DQS output access time from CK/$\overline{CK}$	-450	450	-400	+400	-350	+350	ps
tHZ	Data-out high-impedance time from CK/$\overline{CK}$	-	t_{AC} max	-	tACmax	-	tACmax	ps
tLZ(DQS)	DQS low-impedance time from CK/$\overline{CK}$	t_{AC} min	t_{AC} max	tACmin	tACmax	tACmin	tACmax	ps
tLZ(DQ)	DQ low-impedance time from CK/$\overline{CK}$	$2t_{AC}$ min	t_{AC} max	$2t_{AC}$ min	t_{AC} max	$2t_{AC}$ min	t_{AC} max	ps
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	300	-	240	-	200	ps
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	tCH or tCL	-	tCH or tCL	-	tCH or tCL	-	tCK
tQHS	Data hold Skew Factor	-	400	-	340	-	300	ps
tQH	Data output hold time from DQS	t_{HP} - t_{QHS}	-	tHP - tQHS	-	tHP - tQHS	-	ps
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	0.40	0.60	0.40	0.60	tCK
tRRD	Active bank A to Active bank B command	7.5	-	7.5	-	7.5	-	ns
tFAW	Four Activate Window for 1KB page size products	37.5	-	37.5	-	35	-	ns
tCCD	$\overline{CAS}$ to $\overline{CAS}$	2		2		2		tCK
tWR	Write recovery time without Auto-Precharge	15	-	15	-	15	-	ns
tDAL	Auto precharge write recovery + precharge time	WR+tRP	-	WR+tRP	-	WR+tRP	-	tCK
tWTR	Internal write to read command delay	7.5	-	7.5	-	7.5	-	ns
tRTP	Internal read to precharge command delay	7.5		7.5		7.5		ns
tCKE	CKE minimum pulse width	3		3		3		tCK
tXSNR	Exit self refresh to a Non-read command	tRFC+10	-	tRFC+10		tRFC+10		ns
tXSRD	Exit self refresh to a Read command	200	-	200		200		tCK
tXP	Exit precharge power down to any Non- read command	2	-			2	-	tCK

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ºC ~ 85 ºC; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	PC2-4200		PC2-5300		PC2-6400		Unit
		Min.	Min.	Max.	Max.	Min.	Max.	
tXARD	Exit active power down to read command	2	-	2	-	2	-	tCK
tXARDS	Exit active power down to read command	6-AL	-	7-AL	-	8-AL	-	tCK
tAOND	ODT turn-on delay	2	2	2	2	2	2	tCK
tAON	ODT turn-on	tAC (min)	tAC (max) +0.7	tAC (min)	tAC (max) +0.7	tAC (min)	tAC (max) +0.7	ns
tAONPD	ODT turn-on (Power down mode)	tAC (min) +2	2tCK + tAC(max) +1	tAC (min) +2	2tCK + tAC(max) +1	tAC (min) +2	2tCK + tAC(max) +1	ns
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	tCK
tAOF	ODT turn-off	tAC(min)	tAC(max) +0.6	tAC(min)	tAC(max) +0.6	tAC(min)	tAC(max) +0.6	ns
tAOFPD	ODT turn-off (Power down mode)	tAC (min)+2	2.5tCK + tAC(max) +1	tAC (min)+2	2.5tCK + tAC(max) +1	tAC (min)+2	2.5tCK + tAC(max) +1	ns
tANPD	ODT to power down entry latency	3	-	3		3	-	tCK
tAXPD	ODT power down exit latency	8	-	8		8	-	tCK
tMRD	Mode register set command cycle time	2	-	2	-	2	-	tCK
tMOD	MRS command to ODT update delay	0	12	0	12	0	12	ns
tOIT	OCD drive mode output delay	0	12	0	12	0	12	ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	$t_{IS}+t_{CK}+t_{IH}$	-	- tIS + tCK + tIH	-	tIS + tCK + tIH	-	ns
tREFI	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	3.9		3.9		3.9		µs
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	7.8		7.8		7.8		µs

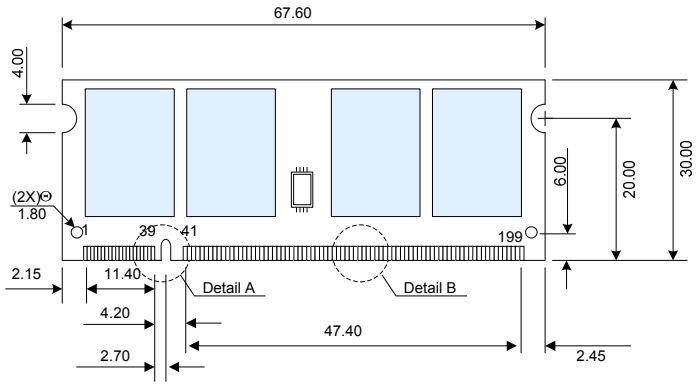
Speed Grade Definition

Symbol	Parameter	-37B		-3C		-25D		Unit
		Min	Max	Min	Max	Min	Max	
tRAS	Row Active Time	45	70,000	45	70,000	45	70,000	ns
tRC	Row Cycle Time	60	-	60	-	60	-	ns
tRCD	RAS to CAS delay	15	-	15	-	15	-	ns
tRP	Row Precharge Time	15	-	15	-	15	-	ns

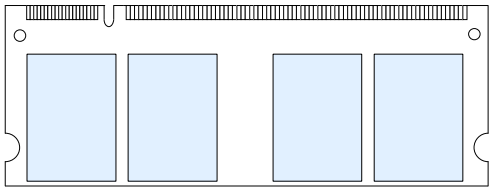
Package Dimensions

(2GB, 2Ranks, x8 DDR2 SDRAMs)

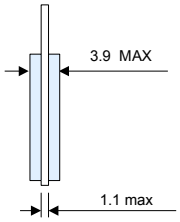
FRONT



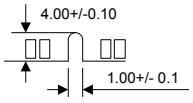
BACK



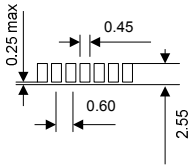
SIDE



Detail A



Detail B



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters

Revision Log

Rev	Date	Modification
0.1	12/2006	Preliminary release.
1.0	05/2007	Official Released.
1.1	07/2007	Added DDR2-800 (-25D) item information
1.2	09/2007	Added Halogen free part numbers
1.3	10/2007	Update Halogen free part numbers

Nanya Technology Corporation

Hwa Ya Technology Park 669

Fu Hsing 3rd Rd., Kueishan,

Taoyuan, 333, Taiwan, R.O.C.

Tel: +886-3-328-1688

Please visit our home page for more information: www.nanya.com

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