240pin Unbuffered DDR2 SDRAM MODULE

Based on 128Mx8 DDR2 SDRAM B-die

Features

Performance:

Speed Sort		PC2-4200	PC2-5300	PC2-6400	Unit
		-37B	-3C	-25D	
DIMM $\overline{CAS}$ Latency*		4	5	6	
f_{CK}	Clock Frequency	266	333	400	MHz
t_{CK}	Clock Cycle	3.75	3	2.5	ns
f_{DQ}	DQ Burst Frequency	533	667	800	MHz

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 256Mx64 DDR2 Unbuffered DIMM based on 128Mx8 DDR2 SDRAM B-die
- Intended for 266MHz/333MHz/400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ}$ = 1.8Volt ± 0.1
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- Bi-directional data strobe with one clock cycle preamble and one-half clock post-amble
- Address and control signals are fully synchronous to positive clock edge
- Write Latency = Read Latency - 1
- Programmable Operation:
  - Device $\overline{CAS}$ Latency: 4(-37B), 5 (-3C) and 6 (-25D)
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 14/10/2 Addressing (row/column/rank)
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect
- On Die Termination (ODT)
- Gold contacts
- SDRAMs in 68-ball BGA Package
- RoHs Compliance

Description

NT2GT64U8HB0JY is 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), organized as a two ranks 256Mx64 high-speed memory array. Modules use sixteen 128Mx8 DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

The DIMM is intended for use in applications operating up to 400MHz clock speeds and achieves high-speed data transfer rates of up to 800MHz. Prior to any access operation, the device $\overline{CAS}$ latency and burst / length /operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
NT2GT64U8HB0JY-37B	266MHz (3.75ns @ CL = 4)	DDR2-533	PC2-4200	256Mx64	GOLD	1.8V	
NT2GT64U8HB0JY-3C	333MHz (3.00ns @ CL = 5)	DDR2-667	PC2-5300				
NT2GT64U8HB0JY-25D	400MHz (2.50ns @ CL = 6)	DDR2-800	PC2-6400				

Pin Description

CK0~CK2 $\overline{CK0}$~$\overline{CK2}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS8	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM8	Input Data Mask
$\overline{CAS}$	Column Address Strobe	$\overline{DQS0}$-$\overline{DQS8}$	Differential data strobes
$\overline{WE}$	Write Enable	VDD	Power (1.8V)
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	VREF	Ref. Voltage for SSTL_18 inputs
A0 ~ A13	Address bus	VDDSPD	Serial EEPROM positive power supply
$\overline{CS0}$ ~ $\overline{CS1}$	DIMM Rank Select	VSS	Ground
BA0 ~ BA2	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RESET	Reset pin	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	On-die termination control lines	SA0 ~ SA2	Serial Presence Detect Address Inputs
NC	No Connect		

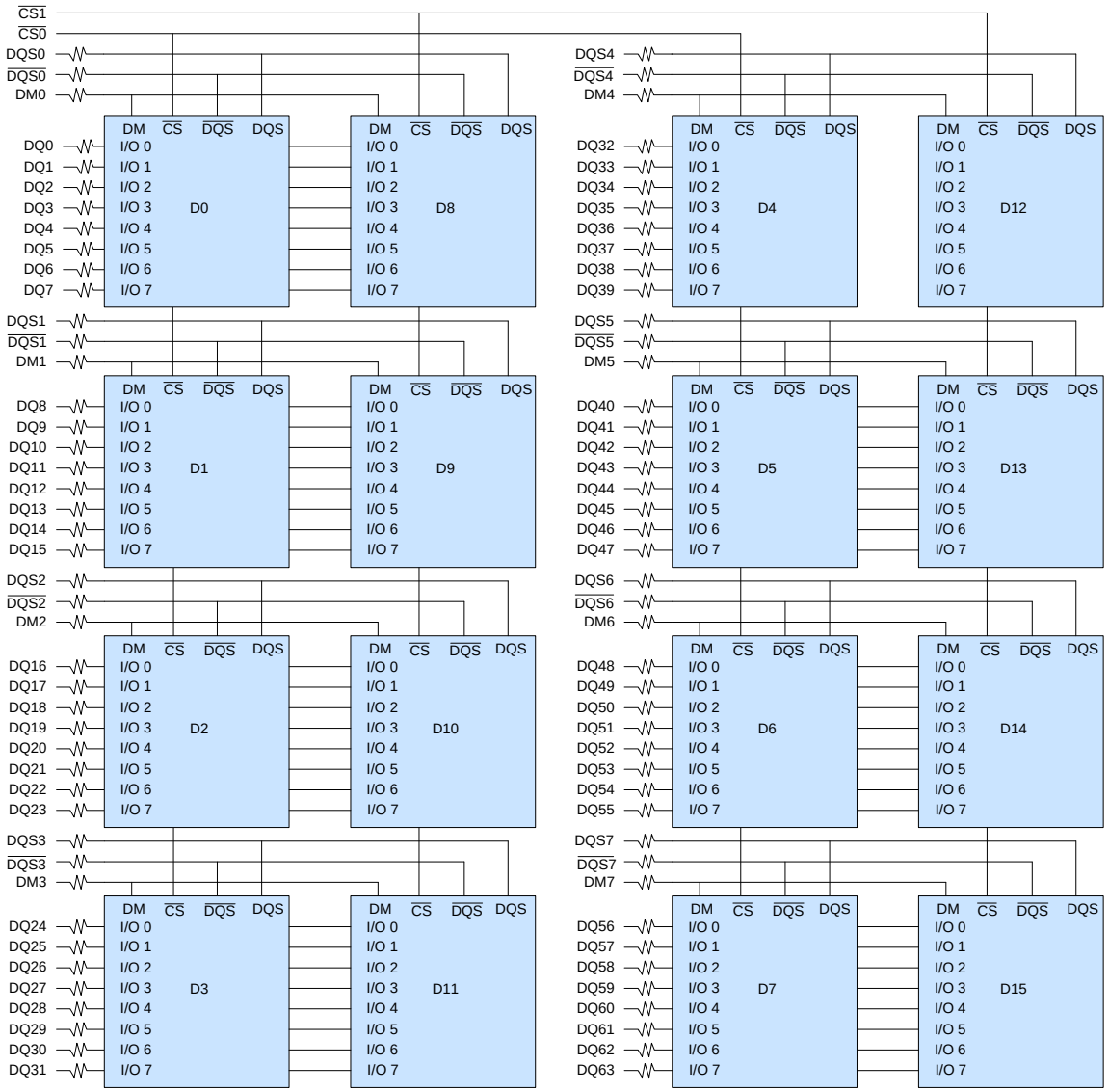
Pinout

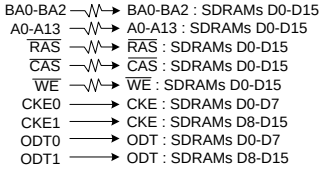
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{REF}	42	NC	82	V_{SS}	121	V_{SS}	162	NC	202	DM4
2	V_{SS}	43	NC	83	$\overline{DQS4}$	122	DQ4	163	V_{SS}	203	NC
3	DQ0	44	V_{SS}	84	DQS4	123	DQ5	164	DM8	204	V_{SS}
4	DQ1	45	$\overline{DQS8}$	85	V_{SS}	124	V_{SS}	165	NC	205	DQ38
5	V_{SS}	46	DQS8	86	DQ34	125	DM0	166	V_{SS}	206	DQ39
6	$\overline{DQS0}$	47	V_{SS}	87	DQ35	126	NC	167	NC	207	V_{SS}
7	DQS0	48	NC	88	V_{SS}	127	V_{SS}	168	NC	208	DQ44
8	V_{SS}	49	NC	89	DQ40	128	DQ6	169	V_{SS}	209	DQ45
9	DQ2	50	V_{SS}	90	DQ41	129	DQ7	170	V_{DDQ}	210	V_{SS}
10	DQ3	51	V_{DDQ}	91	V_{SS}	130	V_{SS}	171	CKE1	211	DM5
11	V_{SS}	52	CKE0	92	$\overline{DQS5}$	131	DQ12	172	V_{DD}	212	NC
12	DQ8	53	V_{DD}	93	DQS5	132	DQ13	173	NC	213	V_{SS}
13	DQ9	54	BA2	94	V_{SS}	133	V_{SS}	174	NC	214	DQ46
14	V_{SS}	55	NC	95	DQ42	134	DM1	175	V_{DDQ}	215	DQ47
15	$\overline{DQS1}$	56	V_{DDQ}	96	DQ43	135	NC	176	A12	216	V_{SS}
16	DQS1	57	A11	97	V_{SS}	136	V_{SS}	177	A9	217	DQ52
17	V_{SS}	58	A7	98	DQ48	137	CK1	178	V_{DD}	218	DQ53
18	NC	59	V_{DD}	99	DQ49	138	$\overline{CK1}$	179	A8	219	V_{SS}
19	NC	60	A5	100	V_{SS}	139	V_{SS}	180	A6	220	CK2
20	V_{SS}	61	A4	101	SA2	140	DQ14	181	V_{DDQ}	221	$\overline{CK2}$
21	DQ10	62	V_{DDQ}	102	NC	141	DQ15	182	A3	222	V_{SS}
22	DQ11	63	A2	103	V_{SS}	142	V_{SS}	183	A1	223	DM6
23	V_{SS}	64	V_{DD}	104	$\overline{DQS6}$	143	DQ20	184	V_{DD}	224	NC
24	DQ16	KEY		105	DQS6	144	DQ21	KEY		225	V_{SS}
25	DQ17	65	V_{SS}	106	V_{SS}	145	V_{SS}	185	CK0	226	DQ54
26	V_{SS}	66	V_{SS}	107	DQ50	146	DM2	186	$\overline{CK0}$	227	DQ55
27	$\overline{DQS2}$	67	VDD	108	DQ51	147	NC	187	VDD	228	V_{SS}
28	DQS2	68	NC	109	V_{SS}	148	V_{SS}	188	A0	229	DQ60
29	V_{SS}	69	VDD	110	DQ56	149	DQ22	189	V_{DD}	230	DQ61
30	DQ18	70	A10/AP	111	DQ57	150	DQ23	190	BA1	231	V_{SS}
31	DQ19	71	BA0	112	V_{SS}	151	V_{SS}	191	V_{DDQ}	232	DM7
32	V_{SS}	72	VDDQ	113	$\overline{DQS7}$	152	DQ28	192	$\overline{RAS}$	233	NC
33	DQ24	73	$\overline{WE}$	114	DQS7	153	DQ29	193	$\overline{CS0}$	234	V_{SS}
34	DQ25	74	$\overline{CAS}$	115	V_{SS}	154	V_{SS}	194	V_{DDQ}	235	DQ62
35	V_{SS}	75	V_{DDQ}	116	DQ58	155	DM3	195	ODT0	236	DQ63
36	$\overline{DQS3}$	76	$\overline{CS1}$	117	DQ59	156	NC	196	A13	237	V_{SS}
37	DQS3	77	ODT1	118	V_{SS}	157	V_{SS}	197	V_{DD}	238	V_{DDSPD}
38	V_{SS}	78	V_{DDQ}	119	SDA	158	DQ30	198	V_{SS}	239	SA0
39	DQ26	79	V_{SS}	120	SCL	159	DQ31	199	DQ36	240	SA1
40	DQ27	80	DQ32			160	V_{SS}	200	DQ37		
41	V_{SS}	81	DQ33			161	NC	201	V_{SS}		

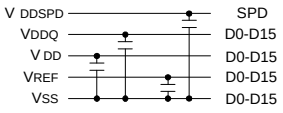
Input/Output Functional Description

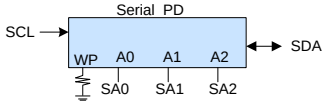
Symbol	Type	Polarity	Function
CK0, CK1, CK2	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-18 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0 – BA2	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0 – DQS8 $\overline{DQS0}$ – $\overline{DQS8}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram (2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)









Serial Presence Detect -- Part 1 of 2

256Mx64 2 RANKs UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		533 -37B	667 -3C	800 -25D	533 -37B	667 -3C	800 -25D	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2			08			
3	Number of Row Addresses on Assembly	14			0E			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Bank	2 rank, Height=30mm			61			
6	Data Width of Assembly	64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at CL=5	3.75ns	3ns	2.5ns	3D	30	25	
10	DDR2 SDRAM Device Access Time from Clock at CL=5	±0.5ns	±0.45ns	±0.4ns	50	45	40	
11	DIMM Configuration Type	Non parity/ECC			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDR SDRAM Width	X8			08			
14	Error Checking DDR SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8			08			
18	DDR2 SDRAM Device Attributes: CAS Latencies Supported	3,4,5		4,5,6	38		70	
19	DIMM Mechanical Characteristic	<4.10mm			01			
20	DDR2 SDRAM DIMM Type Information	Regular UDIMM (133.5mm)			02			
21	DDR2 SDRAM Module Attributes:	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR			07			
23	Minimum Clock Cycle at reduced $\overline{CAS}$ latency; x-1	3.75ns		3ns	3D		30	
24	Maximum Data Access Time (tAC) from Clock at CL X-1	±0.5ns		±0.45ns	50		45	
25	Minimum Clock Cycle Time at CL X-2	5.0ns		3.75ns	50		3D	
26	Maximum Data Access Time (tAC) from Clock at CL X-2	±0.6ns		±0.5ns	60		50	
27	Minimum Row Precharge Time (tRP)	15ns			3C			
28	Minimum Row Active to Row Active delay (tRRD)	7.5ns			1E			
29	Minimum RAS to CAS delay (tRCD)	15ns			3C			
30	Minimum RAS Pulse Width (tRAS)	45.0			2D			
31	Module Bank Density	1GB			01			
32	Address and Command Setup Time Before Clock (tIS)	0.25ns	0.2ns	0.175ns	25	20	17	
33	Address and Command Hold Time After Clock (tIH)	0.375ns	0.275ns	0.25ns	37	27	25	
34	Data Input Setup Time Before Clock (tDS)	0.10ns	0.10ns	0.05ns	10	10	05	
35	Data Input Hold Time After Clock (tDH)	0.225ns	0.175ns	0.125ns	22	17	12	
36	Write Recovery Time (tWR)	15.0ns			3C			
37	Internal Write to Read Command delay (tWTR)	7.5ns			1E			
38	Internal Read to Precharge delay (tRTP)	7.5ns			1E			
39	Reserved	Undefined			00			

Serial Presence Detect -- Part 2 of 2

256Mx64 2 RANKs UNBUFFERED DDR2 SDRAM DIMM based on 128Mx8, 4Banks, 8K Refresh, 1.8V DDR2 SDRAMs with SPD

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Note
		533 -37B	667 -3C	800 -25D	533 -37B	667 -3C	800 -25D	
40	Extension of Byte 41 tRC and Byte 42 tRFC	-			06		00	
41	Minimum Core Cycle Time (tRC)	60.0ns			3C			
42	Min. Auto Refresh Command Cycle Time (tRFC)	127.5ns		105ns	7F		69	
43	Maximum Clock Cycle Time (tCK)	8.0ns			80			
44	Max. DQS-DQ Skew Factor (tQHS)	0.30ns	0.24ns	0.20ns	1E	18	14	
45	Read Data Hold Skew Factor (tQHS)	0.40ns	0.34ns	0.30ns	28	22	1E	
46	PLL Relock Time	N/A			00			
46-61	Reserved	TBD			--			
62	SPD Revision	1.2			12			
63	Checksum for bytes 0-62	Check Sum			5B	17	C5	
64-71	Manufacture's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing Code			--			
73-91	Module Part number	Module Part Number in ASCII			--			1
92-255	Reserved	Undefined			--			

Note 1:

NT2GT64U8HB0JY-37B ➔ 4E543247543634553848423 04A592D33374220
NT2GT64U8HB0JY-3C ➔ 4E543247543634553848423 04A592D33432020
NT2GT64U8HB0JY-25D ➔ 4E543247543634553848423 04A592D32354420

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.5 to 2.3	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to Vss	-0.5 to 2.3	V
V_{DDQL}	Voltage on V_{DDQL} supply relative to Vss	-0.5 to 2.3	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +2.3	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +2.3	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Operating Conditions

Symbol	Parameter	Rating	Units	Note
T_{CASE}	Operating Temperature (Ambient)	0 to 95	°C	1,2,3
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	
I_L	Short Circuit Output Current	-5 to 5	µA	

Note:
1. Case temperature is measured at top and center side of any DRAMs.
2. t_{CASE} > 85°C ➔ t_{REFI} = 3.9 µs
3. All DRAM specification only support 0°C < t_{CASE} < 85°C

DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
VDD	Supply Voltage	1.7	1.9	V	1
VDDQ	Supply Voltage for Output	1.7	1.9	V	1, 3
VDDL	Supply Voltage for VDDQL	1.7	1.9	V	3
VREF	I/O Reference Voltage	0.49VDDQ	0.51VDDQ	V	2
VTT	Termination Voltage	VREF – 0.04	VREF + 0.04	V	4
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.125	VDDQ + 0.3	V	
VIL (DC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.125	V	

Note:
1. Inputs are not recognized as valid until VREF stabilizes.
2. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
3. VDDQ tracks with VDD, VDDL tracks with VDD.
4. VTT of transmitting device track VREF of receiving device.

Environmental Parameters

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a tress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature shall not exceed the value specified in the component spec.

Operating, Standby, and Refresh Currents

T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} = 1.8V ± 0.1V (2GB, 2 Rank, 128Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-4200 (-37B)	PC2-5300 (-3C)	PC2-6400 (-25D)	Unit
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = $t_{RC\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1408	1496	1804	mA
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = $t_{RC\ (MIN)}$; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	1540	1628	1892	mA
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	230	230	230	mA
I_{DD2N}	Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle	968	1056	1144	mA
I_{DD2Q}	Precharge Quiet Standby Current: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; t_{CK} = $t_{CK\ (MIN)}$; Other control and address inputs are stable, Data bus inputs are floating.	880	1056	1144	mA
I_{DD3PF}	Active Power-Down Current: All banks open; t_{CK} = $t_{CK\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **low** (Fast Power-down Exit).	616	704	792	mA
I_{DD3PS}	Active Power-Down Current: All banks open; t_{CK} = $t_{CK\ (MIN)}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are floating. MRS A12 bit is set to **high** (Slow Power-down Exit).	352	352	440	mA
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; t_{RC} = $t_{RAS\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1056	1232	1584	mA
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$	1936	2112	2552	mA
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA	1760	1936	2508	mA
I_{DD5}	Auto-Refresh Current: t_{RC} = $t_{RFC\ (MIN)}$	2288	2552	2772	mA
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	230	230	230	mA
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	2728	3256	3520	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	PC2-4200		PC2-5300		PC2-6400		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tCK	Clock Cycle Time	3750	8000					ps
	Clock Cycle Time (Average)			3000	8000	2500	800	ps
tCH	CK high-level width	0.45	0.55	0.48	0.52	0.48	0.52	tCK
tCL	CK low-level width	0.45	0.55	0.48	0.52	0.48	0.52	tCK
WL	Write command to DQS associated clock edge	RL-1		RL-1		RL-1		tCK
tDQSS	Write command to 1st DQS latching transition	-0.25	0.25	-0.25	+0.25	-0.25	+0.25	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	0.35	-	0.35	-	tCK
tWPRE	Write preamble	0.35	-	0.35	-	0.35	-	tCK
tWPST	Write postamble	0.4	0.6	0.40	0.60	0.40	0.60	tCK
tIS	Address and control input setup time	250	-	200	-	175	-	ps
tIH	Address and control input hold time	375	-	275	-	250	-	ps
tIPW	Input pulse width	0.6	-	0.6	-	0.6	-	tCK
tDS	DQ and DM input setup time(differential data strobe)	100	-	100	-	50	-	ps
tDH	DQ and DM input hold time(differential data strobe)	225	-	175	-	125	-	ps
tDIPW	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	tCK
tAC	DQ output access time from CK/$\overline{CK}$	-500	500	-450	450	-400	+400	ps
tDQSCK	DQS output access time from CK/$\overline{CK}$	-450	450	-400	+400	-350	+350	ps
tHZ	Data-out high-impedance time from CK/$\overline{CK}$	-	t_{AC} max	-	tACmax	-	tACmax	ps
tLZ(DQS)	DQS low-impedance time from CK/$\overline{CK}$	t_{AC} min	t_{AC} max	tACmin	tACmax	tACmin	tACmax	ps
tLZ(DQ)	DQ low-impedance time from CK/$\overline{CK}$	$2t_{AC}$ min	t_{AC} max	$2t_{AC}$ min	t_{AC} max	$2t_{AC}$ min	t_{AC} max	ps
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	300	-	024	-	200	ps
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	tCH or tCL	-	tCH or tCL	-	tCH or tCL	-	tCK
tQHS	Data hold Skew Factor	-	400	-	340	-	300	ps
tQH	Data output hold time from DQS	t_{HP} - t_{QHS}	-	tHP - tQHS	-	tHP - tQHS	-	ps
tRPRE	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	0.40	0.60	0.40	0.60	tCK
tRRD	Active bank A to Active bank B command	7.5	-	7.5	-	7.5	-	ns
tFAW	Four Activate Window for 1KB page size products	37.5	-	37.5	-	37.5	-	ns
tCCD	$\overline{CAS}$ to $\overline{CAS}$	2		2		2		tCK
tWR	Write recovery time without Auto-Precharge	15	-	15	-	15	-	ns
tDAL	Auto precharge write recovery + precharge time	WR+tRP	-	WR+tRP	-	WR+tRP	-	tCK
tWTR	Internal write to read command delay	7.5	-	7.5	-	7.5		ns
tRTP	Internal read to precharge command delay	7.5		7.5		7.5		ns
tCKE	CKE minimum pulse width	3		3		3		tCK
tXSNR	Exit self refresh to a Non-read command	tRFC+10	-	tRFC+10		tRFC+10		ns
tXSRD	Exit self refresh to a Read command	200	-	200		200		tCK
tXP	Exit precharge power down to any Non- read command	2	-	2	-	2	-	tCK

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

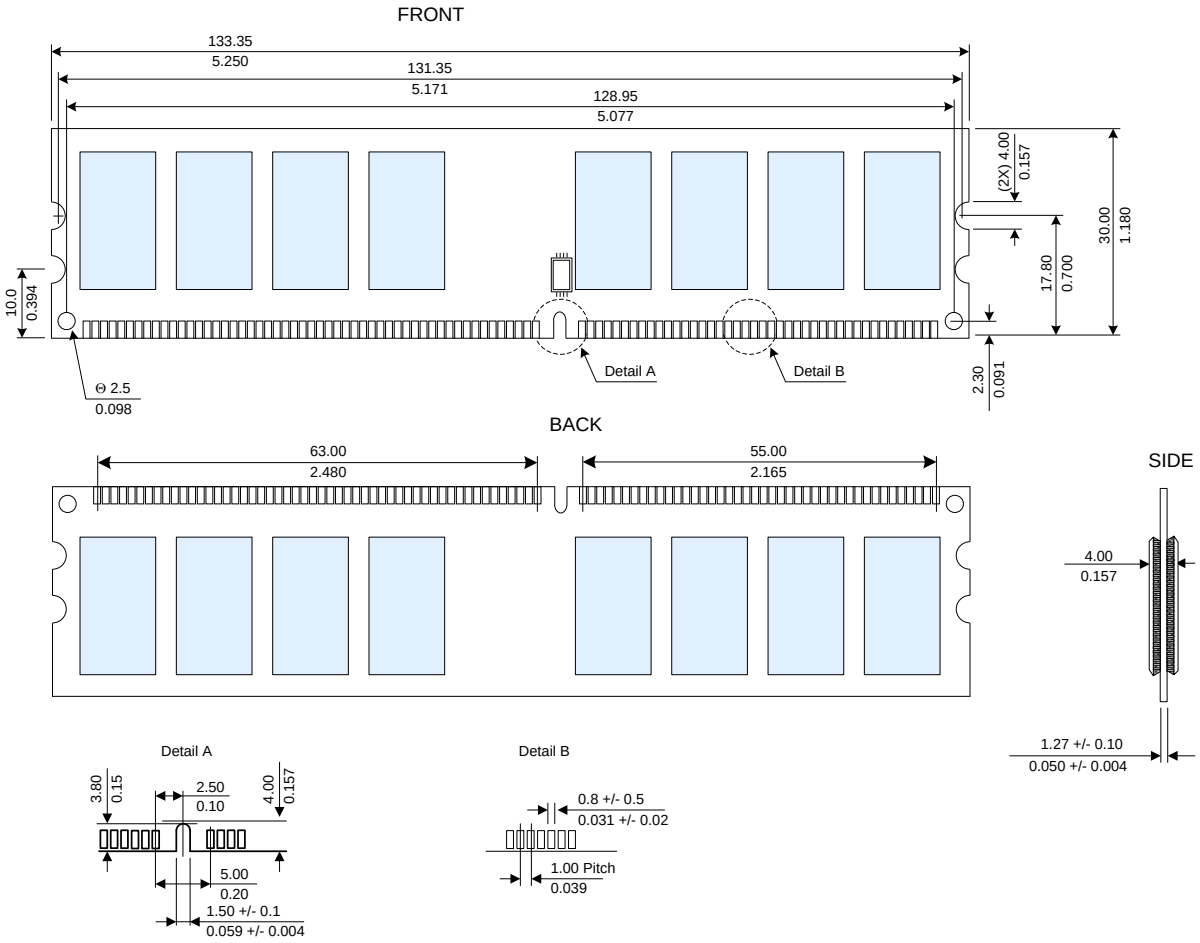
Symbol	Parameter	PC2-4200		PC2-5300		PC2-6400		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tXARD	Exit active power down to read command	2	-	2	-	2	-	tCK
tXARDS	Exit active power down to read command	6-AL		7-AL		8-AL		tCK
tAOND	ODT turn-on delay	2	2	2	2	2	2	tCK
tAON	ODT turn-on	tAC (min)	tAC (max) +1	tAC (min)	tAC (max) +0.7	tAC (min)	tAC (max) +0.7	ns
tAONPD	ODT turn-on (Power down mode)	tAC (min) +2	2tCK + tAC(max) +1	tAC (min) +2	2tCK + tAC(max) +1	tAC (min) +2	2tCK + tAC(max) +1	ns
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	tCK
tAOF	ODT turn-off	tAC(min)	tAC(max) +0.6	tAC(min)	tAC(max) +0.6	tAC(min)	tAC(max) +0.6	ns
tAOFPD	ODT turn-off (Power down mode)	tAC (min)+2	2.5tCK + tAC(max) +1	tAC (min)+2	2.5tCK + tAC(max) +1	tAC (min)+2	2.5tCK + tAC(max) +1	ns
tANPD	ODT to power down entry latency	3		3	-	3	-	tCK
tAXPD	ODT power down exit latency	8		8		8		tCK
tMRD	Mode register set command cycle time	2	-	2	-	2	-	tCK
tMOD	MRS command to ODT update delay	0	12	0	12	0	12	ns
tOIT	OCD drive mode output delay	0	12	0	12	0	12	ns
tDelay	Minimum time clocks remains ON after CKE asynchronously drops Low	$t_{IS}+t_{CK}+t_{IH}$		tIS + tCK + tIH	-	tIS + tCK + tIH	-	ns
tRFC	Refresh to active/Refresh command time	127.5		127.5		127.5		ns
tREFI	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	3.9		3.9		3.9		µs
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	7.8		7.8		7.8		µs

Speed Grade Definition

Symbol	Parameter	-37B		-3C		-25D		Unit
		Min	Max	Min	Max	Min	Max	
tRAS	Row Active Time	45	70,000	45	70,000	45	70,000	ns
tRC	Row Cycle Time	60	-	60	-	60	-	ns
tRCD	RAS to CAS delay	15	-	15	-	15	-	ns
tRP	Row Precharge Time	15	-	15	-	15	-	ns

Package Dimensions

(2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 (0.006) unless otherwise stated.

Units: Millimeters (Inches)

Revision Log

Rev	Date	Modification
1.0	08/2006	PC2-4200 & PC2-5300 UDIMM official release
1.1	09/2007	Add -25D spec