NT2GC72B89B0NJ/NT2GC72B89B0NK
NT4GC72B8PB0NJ/NT4GC72B8PB0NL/NT4GC72B4PB0NJ/NT4GC72B4PB0NL
NT8GC72B4NB1NJ/NT8GC72B4NB1NK/NT16TC72B4NB1NJ/NT16TC72B4NB1NL

2GB: 256M x 72 / 4GB: 512M x 72 / 8GB: 1G x 72 / 16GB: 2G x 72
PC3-8500 / PC3-10600
Registered DDR3 SDRAM DIMM

Based on DDR3-1066/1333 256Mx8 (2GB/4GB) / 512Mx4 (4GB/8GB) SDRAM B-Die
Based on DDR3-1066 1Gx4 (DDP) (16GB) SDRAM B-Die

Features

•Performance:

Speed Sort	PC3-8500	PC3-10600	Unit
	-BE	-CG	
DIMM CAS Latency	7	9	
fck – Clock Frequency	533	667	MHz
tck – Clock Cycle	1.875	1.5	ns
fDQ – DQ Burst Frequency	1066	1333	Mbps

- 240-Pin Registered Dual In-Line Memory Module (RDIMM)
- 2GB/4GB: 256Mx72/512Mx72 DDR3 Registered DIMM based on 256Mx8 DDR3 SDRAM B-Die devices
- 4GB/8GB: 512Mx72/1024Mx72 DDR3 Registered DIMM based on 512Mx4 DDR3 SDRAM B-Die devices
- 16GB: 2Gx72 DDR3 Registered DIMM based on 1024Mx4 (DDP) DDR3 SDRAM B-Die devices
- Intended for 533MHz/667MHz applications
- Inputs and outputs are SSTL-15 compatible
- V_{DD} = V_{DDQ} = 1.5V ± 0.075V
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Nominal and Dynamic On-Die Termination support
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 6,7,8,9
  - Burst Type: Sequential or Interleave
  - Burst Length: BC4, BL8
  - Operation: Burst Read and Write
- Two different termination values (Rtt_Nom & Rtt_WR)
- 14/11/1 (row/column/rank) Addressing for 2GB
- 14/12/1 (row/column/rank) Addressing for 4GB (512Mx4 Device)
- 14/11/2 (row/column/rank) Addressing for 4GB (256Mx8 Device)
- 14/12/2 (row/column/rank) Addressing for 8GB
- 14/12/4 (row/column/rank) Addressing for 16GB
- Extended operating temperature rage
- Auto Self-Refresh option
- Serial Presence Detect
- Gold contacts
- SDRAMs are in 78-ball BGA Package
- RoHS compliance
- Halogen free product

Description

NT2GC72B89B0NJ,NT2GC72B89B0NK,NT4GC72B8PB0NJ,NT4GC72B8PB0NL,NT4GC72B4PB0NJ,NT4GC72B4PB0NL,NT8GC72B4NB1NJ,NT8GC72B4NB1NK,NT16TC72B4NB1NJ, and NT16TC72B4NB1NL are 240-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Registered Dual In-Line Memory Module, organized as one rank of 256Mx72 (2GB), one rank or two ranks of 512Mx72 (4GB), two ranks of 1Gx72 (8GB) and four ranks of 2Gx72 (16GB) high-speed memory array. Modules use nine 256Mx8 (2GB) 78-ball BGA packaged devices, eighteen 256Mx8 (4GB) 78-ball BGA packaged devices, thirty-six 512Mx4 (8GB) 78-ball BGA packaged devices and thirty-six 1Gx4 (DDP) (16GB) 78-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR3 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

The DIMM is intended for use in applications operating of 533MHz/667MHz clock speeds and achieves high-speed data transfer rates of 1066Mbps/1333Mbps. Prior to any access operation, the device $\overline{CAS}$ latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0~BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Power	Leads	Note
NT2GC72B89B0NK-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)	256Mx72	1.5V	Gold	
NT2GC72B89B0NJ-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				
NT4GC72B8PB0NL-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)	512Mx72			
NT4GC72B8PB0NJ-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				
NT4GC72B4PB0NL-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				
NT4GC72B4PB0NJ-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				
NT8GC72B4NB1NK-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)	1Gx72			
NT8GC72B4NB1NJ-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				
NT16TC72B4NB1NL-BE	DDR3-1066	PC3-8500	533MHz (1.875ns @ CL = 7)	2Gx72			
NT16TC72B4NB1NJ-BE	DDR3-1066	PC3-8500	533MHz (1.875ns @ CL = 7)				

Pin Description

Pin Name	Description	Pin Name	Description
CK0, CK1	Clock Inputs, positive line	ODT0, ODT1	Active termination control lines
$\overline{CK0}$, $\overline{CK1}$	Clock Inputs, negative line	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS17	Data strobes
$\overline{RAS}$	Row Address Strobe	$\overline{DQS0}$-$\overline{DQS17}$	Data strobes complement
$\overline{CAS}$	Column Address Strobe	TDQS9-TDQS17	Termination data strobes
$\overline{WE}$	Write Enable	$\overline{TDQS9}$-$\overline{TDQS17}$	Termination data strobes
$\overline{S0}$-$\overline{S3}$	Chip Selects	DM0-DM8	Data Masks
A0-A9, A11, A13	Address Inputs	CB0-CB7	ECC Check Bits
A10/AP	Address Input/Auto-Precharge	$\overline{EVENT}$	Temperature event pin
A12/$\overline{BC}$	Address Input/Burst Chop	$\overline{RESET}$	Reset pin
BA0-BA2	SDRAM Bank Address Inputs	V_{REFDQ} , V_{REFCA}	Input/Output Reference
SCL	Serial Presence Detect Clock Input	V_{DDSPD}	SPD and Temp sensor power
SDA	Serial Presence Detect Data input/output	SA0, SA1, SA2	Serial Presence Detect Address Inputs
Par_In	Parity bit for the Address and Control bus	Vtt	Termination voltage
$\overline{Err\_Out}$	Parity error found on the Address and Control bus	V_{SS}	Ground
NC	No Connect	V_{DD}	Core and I/O power

DDR3 SDRAM Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REFDQ}	121	V_{SS}	31	DQ25	151	V_{SS}	61	A2	181	A1	91	DQ41	211	V_{SS}
2	V_{SS}	122	DQ4	32	V_{SS}	152	DM3/DQS12 /TDQS12	62	V_{DD}	182	V_{DD}	92	V_{SS}	212	DM5/DQS14 /TDQS14
3	DQ0	123	DQ5	33	$\overline{DQS3}$	153	NC/$\overline{DQS12}$ /$\overline{TDQS12}$	63	NC	183	V_{DD}	93	$\overline{DQS5}$	213	NC/$\overline{DQS14}$ /$\overline{TDQS14}$
4	DQ1	124	V_{SS}	34	DQS3	154	V_{SS}	64	NC	184	CK0	94	DQS5	214	V_{SS}
5	V_{SS}	125	DM0/DQS9/ TDQS9	35	V_{SS}	155	DQ30	65	V_{DD}	185	$\overline{CK0}$	95	V_{SS}	215	DQ46
6	$\overline{DQS0}$	126	NC/$\overline{DQS9}$ /$\overline{TDQS9}$	36	DQ26	156	DQ31	66	V_{DD}	186	V_{DD}	96	DQ42	216	DQ47
7	DQS0	127	V_{SS}	37	DQ27	157	V_{SS}	67	V_{REFCA}	187	$\overline{EVENT}$	97	DQ43	217	V_{SS}
8	V_{SS}	128	DQ6	38	V_{SS}	158	CB4	68	Par_In/NC	188	A0	98	V_{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0	159	CB5	69	V_{DD}	189	V_{DD}	99	DQ48	219	DQ53
10	DQ3	130	V_{SS}	40	CB1	160	V_{SS}	70	A10/AP	190	BA1	100	DQ49	220	V_{SS}
11	V_{SS}	131	DQ12	41	V_{SS}	161	DM8/DQS17 /TDQS17	71	BA0	191	V_{DD}	101	V_{SS}	221	DM6/DQS15 /TDQS15
12	DQ8	132	DQ13	42	$\overline{DQS8}$	162	NC/$\overline{DQS17}$ /$\overline{TDQS17}$	72	V_{DD}	192	$\overline{RAS}$	102	$\overline{DQS6}$	222	NC/$\overline{DQS15}$ /$\overline{TDQS15}$
13	DQ9	133	V_{SS}	43	DQS8	163	V_{SS}	73	$\overline{WE}$	193	$\overline{S0}$	103	DQS6	223	V_{SS}
14	V_{SS}	134	DM1/DQS10 /TDQS10	44	V_{SS}	164	CB6	74	$\overline{CAS}$	194	V_{DD}	104	V_{SS}	224	DQ54
15	$\overline{DQS1}$	135	NC/$\overline{DQS10}$ /$\overline{TDQS10}$	45	CB2	165	CB7	75	V_{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	V_{SS}	46	CB3	166	V_{SS}	76	$\overline{S1}$/NC	196	A13	106	DQ51	226	V_{SS}
17	V_{SS}	137	DQ14	47	V_{SS}	167	NC	77	ODT1/NC	197	V_{DD}	107	V_{SS}	227	DQ60
18	DQ10	138	DQ15	48	V_{TT}/NC	168	$\overline{RESET}$	78	V_{DD}	198	$\overline{S3}$/NC	108	DQ56	228	DQ61
19	DQ11	139	V_{SS}	49	V_{TT}/NC	169	CKE1/NC	79	$\overline{S2}$/NC	199	V_{SS}	109	DQ57	229	V_{SS}
20	V_{SS}	140	DQ20	50	CKE0	170	V_{DD}	80	V_{SS}	200	DQ36	110	V_{SS}	230	DM7/DQS16 /TDQS16
21	DQ16	141	DQ21	51	V_{DD}	171	NC	81	DQ32	201	DQ37	111	$\overline{DQS7}$	231	NC/$\overline{DQS16}$ /$\overline{TDQS16}$
22	DQ17	142	V_{SS}	52	BA2	172	NC	82	DQ33	202	V_{SS}	112	DQS7	232	V_{SS}
23	V_{SS}	143	DM2/DQS11 /TDQS11	53	$\overline{Err\_Out}$/NC	173	V_{DD}	83	V_{SS}	203	DM4/DQS13 /TDQS13	113	V_{SS}	233	DQ62
24	$\overline{DQS2}$	144	NC/$\overline{DQS11}$ /$\overline{TDQS11}$	54	V_{DD}	174	A12/$\overline{BC}$	84	$\overline{DQS4}$	204	NC/$\overline{DQS13}$ /$\overline{TDQS13}$	114	DQ58	234	DQ63
25	DQS2	145	V_{SS}	55	A11	175	A9	85	DQS4	205	V_{SS}	115	DQ59	235	V_{SS}
26	V_{SS}	146	DQ22	56	A7	176	V_{DD}	86	V_{SS}	206	DQ38	116	V_{SS}	236	V_{DDSPD}
27	DQ18	147	DQ23	57	V_{DD}	177	A8	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V_{SS}	58	A5	178	A6	88	DQ35	208	V_{SS}	118	SCL	238	SDA
29	V_{SS}	149	DQ28	59	A4	179	V_{DD}	89	V_{SS}	209	DQ44	119	SA2	239	V_{SS}
30	DQ24	150	DQ29	60	V_{DD}	180	A3	90	DQ40	210	DQ45	120	V_{TT}	240	V_{TT}

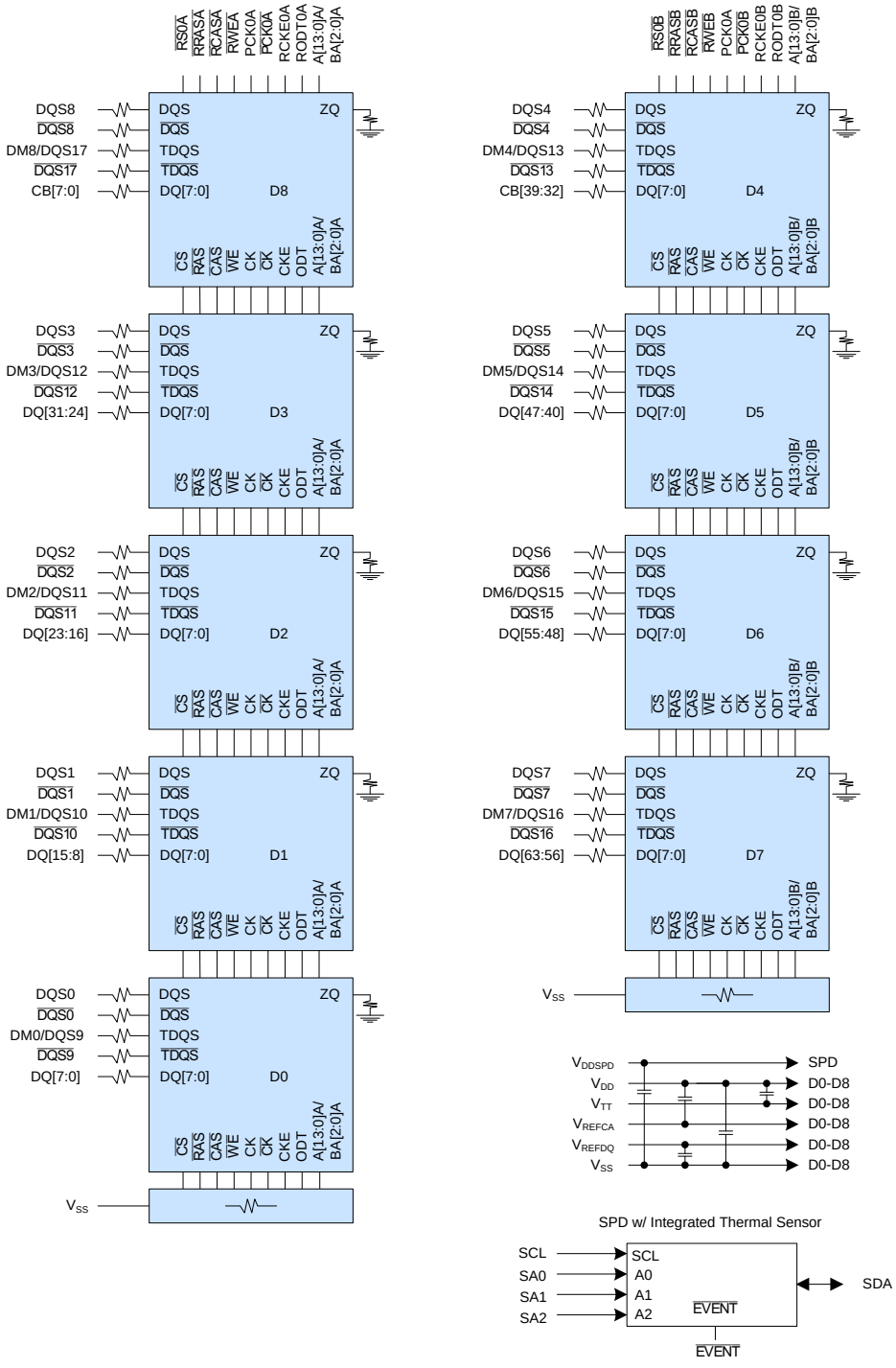
Note: 1. CKE1, $\overline{S1}$ and ODT1 are for 2GB/4GB/8GB only.
2. $\overline{S2}$ and $\overline{S3}$ are for 8GB only.
3. TDQS9-TDQS17 and $\overline{TDQS9}$-$\overline{TDQS17}$ are for 1GB/2GB only.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1 $\overline{CK0}$, $\overline{CK1}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock. However, CK1 and $\overline{CK1}$ are terminated but not used on RDIMMs.
CKE0, CKE1	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$ – $\overline{S3}$	Input	Active Low	Enable the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, $\overline{S2}$ and $\overline{S3}$ operate similarly to $\overline{S0}$ and $\overline{S1}$ for the second set of register outputs or register control words.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
ODT0, ODT1	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0 – DQS17 $\overline{DQS0}$ – $\overline{DQS17}$	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the cross point of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to V_{SS} and DDR3 SDRAM mode registers programmed appropriately.
TDQS9 – TDQS17 $\overline{TDQS9}$ – $\overline{TDQS17}$	Output		TDQS/$\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via mode register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function $\overline{TDQS}$ is not used. X4/x16 DRAMs must disable the TDQS function via mode register A11=0 in MR1.
BA0, BA1, BA2	Input	-	Selects which DDR3 SDRAM internal bank of four or eight is activated.
A0 – A9 A10/AP A11 A12/$\overline{BC}$ A13	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0 – DQ63	Input	-	Data Input/Output pins.
CB0 – CB7	I/O	-	Check bits are used for ECC.
V_{DD}, V_{DDSPD}, V_{SS}	Supply	-	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ}, V_{REFCA}	Supply	-	Reference voltage for SSTL15 inputs.
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and temp sensor. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0 – SA2	Input	-	Address pins used to select the Serial Presence Detect and Temp sensor base address.
$\overline{EVENT}$	Output	-	The $\overline{EVENT}$ pin is reserved for use to flag critical module temperature.
$\overline{RESET}$	Input	-	This signal resets the DDR3 SDRAM.
Par_In	Input	-	Parity bit for the Address and Control bus.
$\overline{Err\_Out}$	Output	-	Parity error detected on the Address and Control bus. A resistor may be connected from bus line to V_{DD} on the system planar to act as a pull up.

Functional Block Diagram (Part 1 of 2)

[2GB – 1 Rank, 256Mx8 DDR3 SDRAMs]

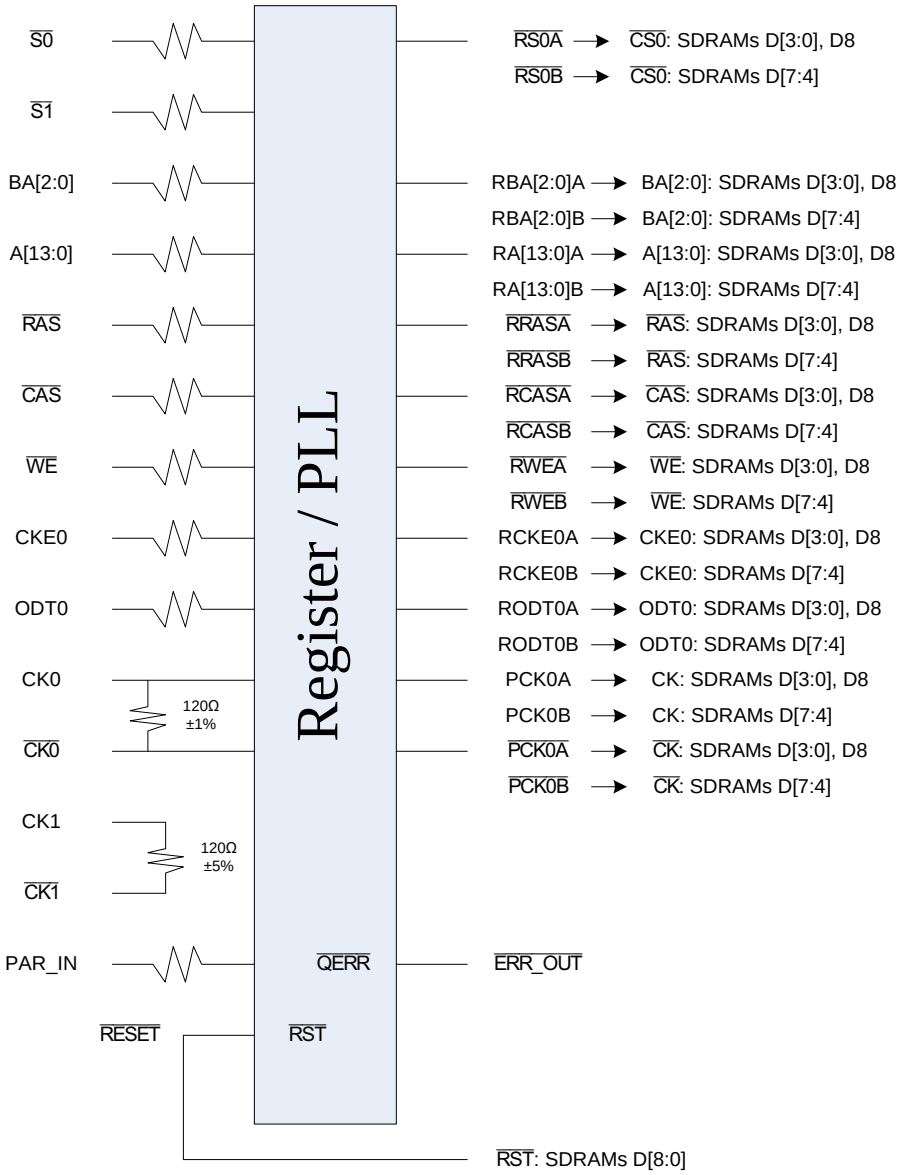


Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.

Functional Block Diagram (Part 2 of 2)

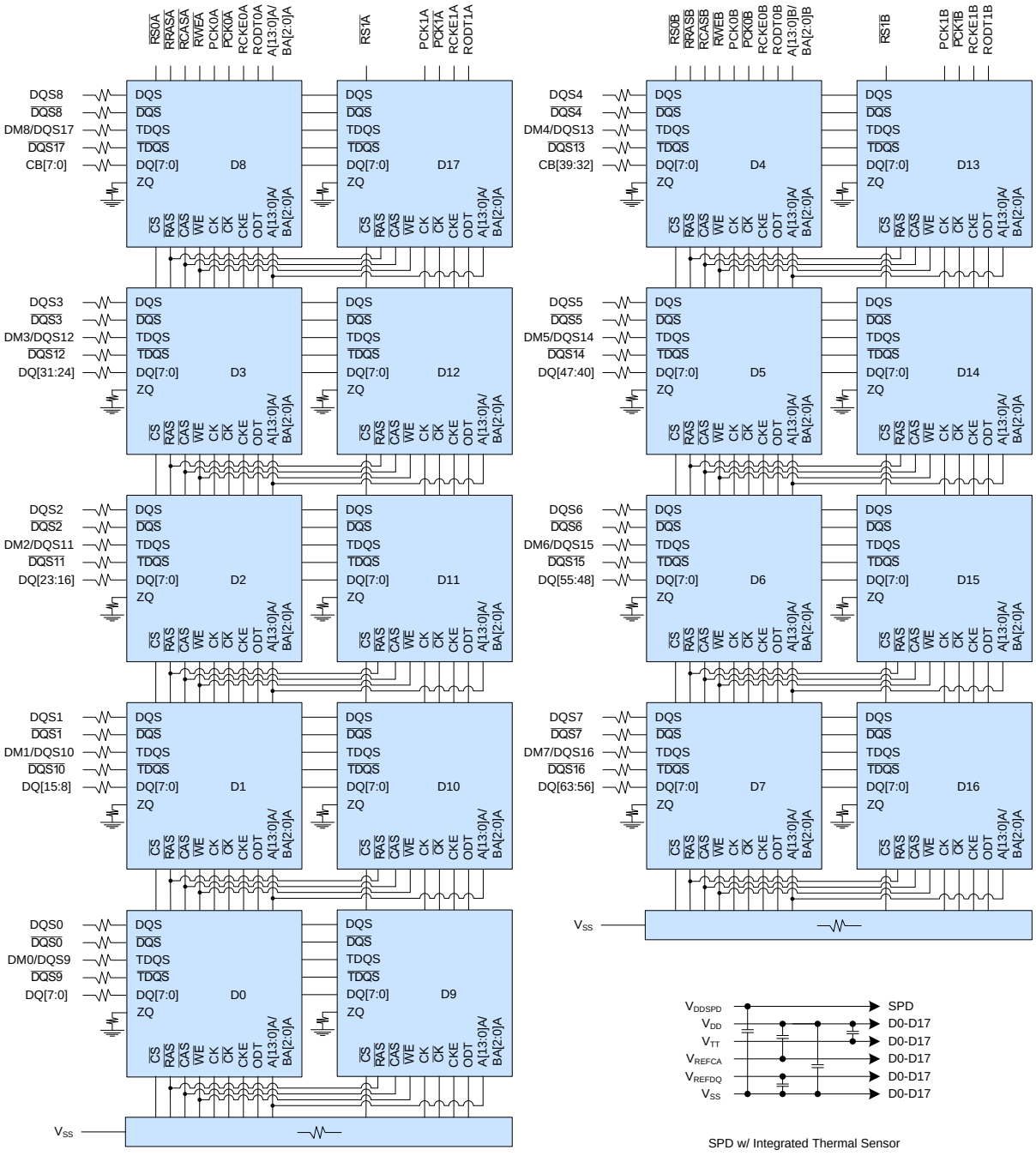
[2GB – 1 Rank, 256Mx8 DDR3 SDRAMs]



Note: S[3:2], CKE1, ODT1 are NC
(Unused register inputs ODT1 and CKE1 have a 330Ω resistor to ground)

Functional Block Diagram (Part 1 of 2)

[4GB – 2 Ranks, 256Mx8 DDR3 SDRAMs]

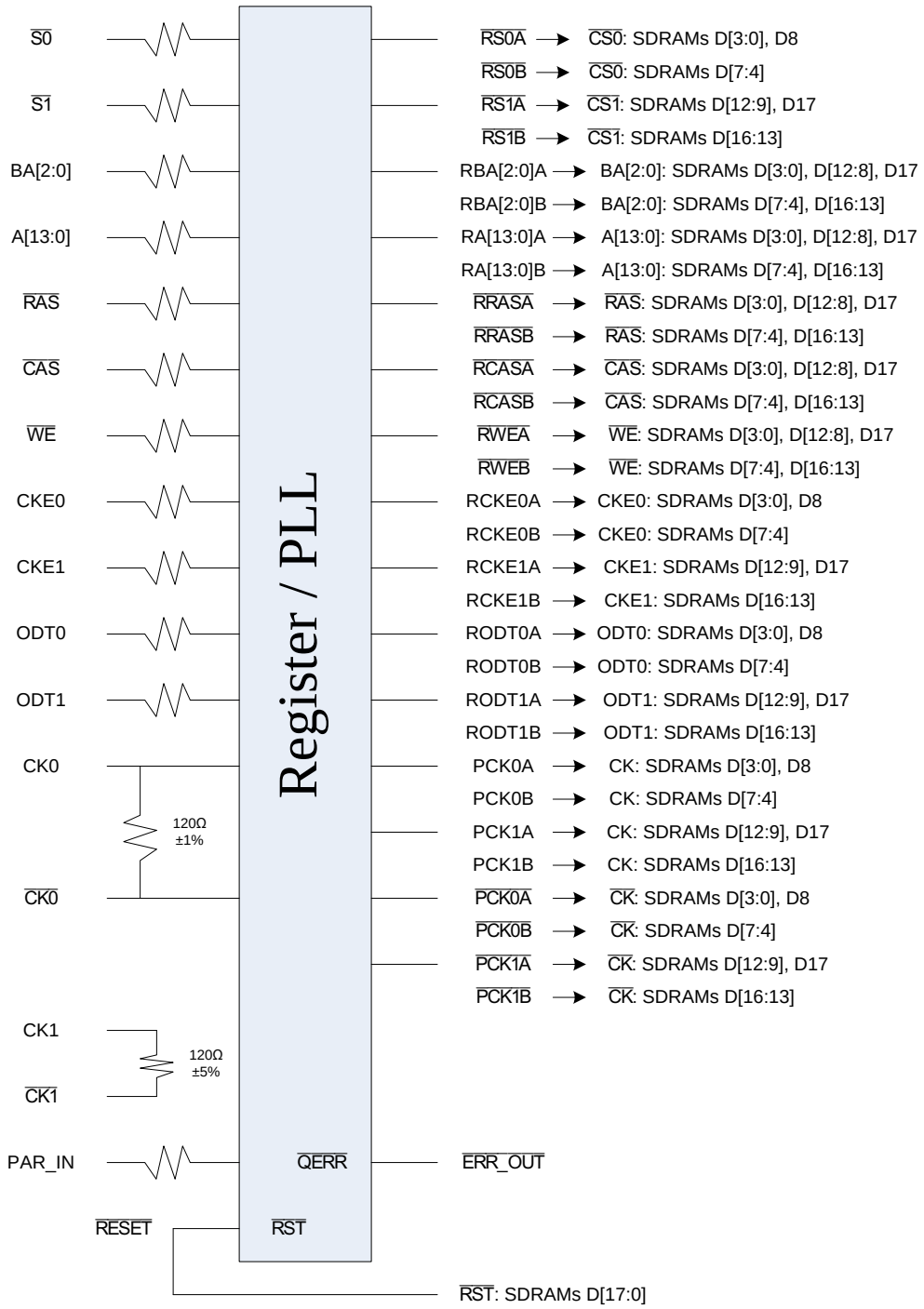


Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
3. Unless otherwise noted, resistor values are 15Ω ± 5%.
4. See the wiring diagrams for all resistors associated with the command, address and control bus.

Functional Block Diagram (Part 2 of 2)

[4GB – 2 Ranks, 256Mx8 DDR3 SDRAMs]



Functional Block Diagram (Part 1 of 3)

[4GB – 1 Rank, 512Mx4 DDR3 SDRAMs]

Notes :
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
3. Unless otherwise noted, resistor values are 15Ω ± 5%.
4. See the wiring diagrams for all resistors associated with the command, address and control bus.

SPD w/ Integrated Thermal Sensor

Functional Block Diagram (Part 2 of 3)

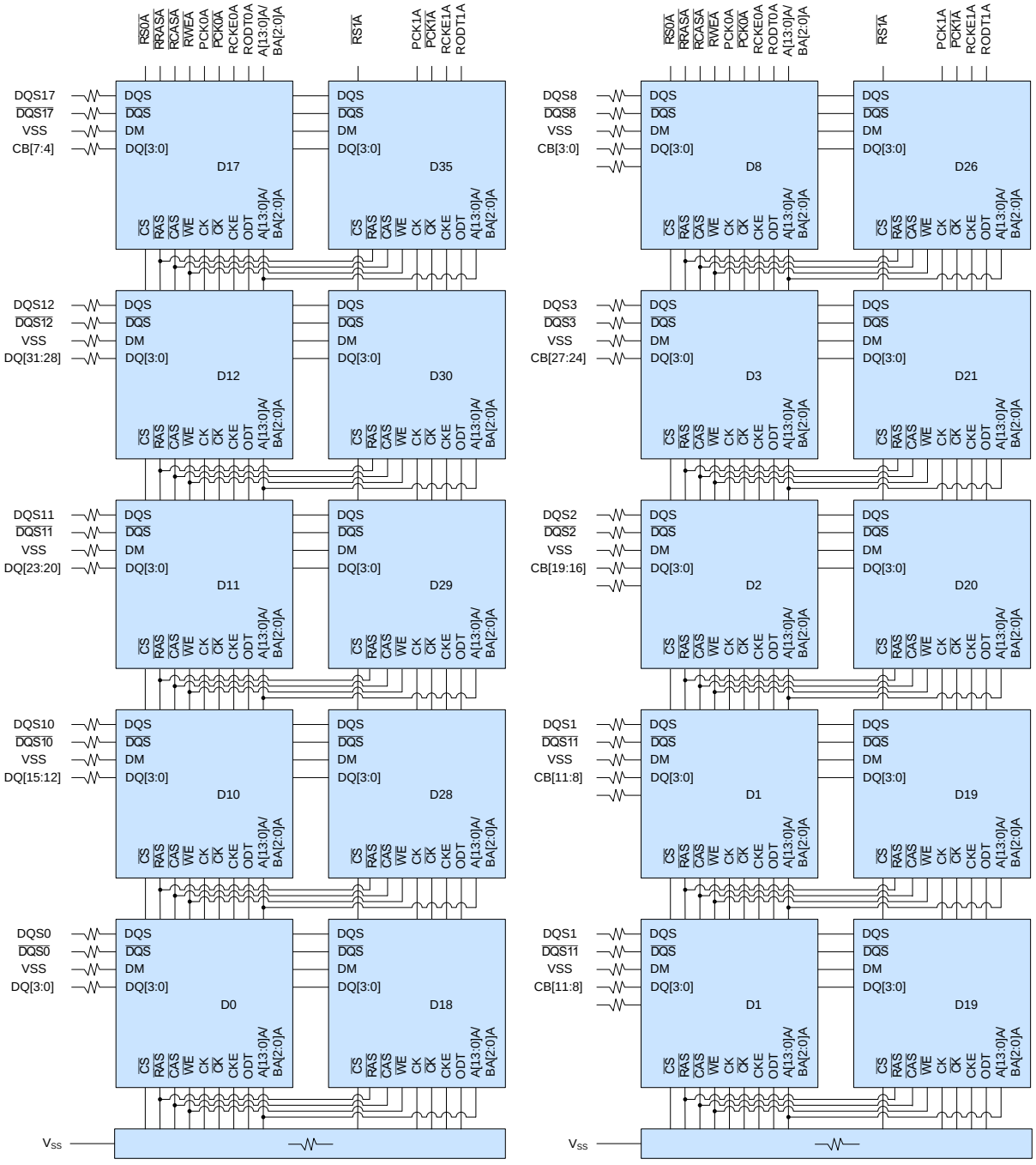
[4GB – 1 Rank, 512Mx4 DDR3 SDRAMs]

Functional Block Diagram (Part 3 of 3)

[4GB – 1 Rank, 512Mx4 DDR3 SDRAMs]

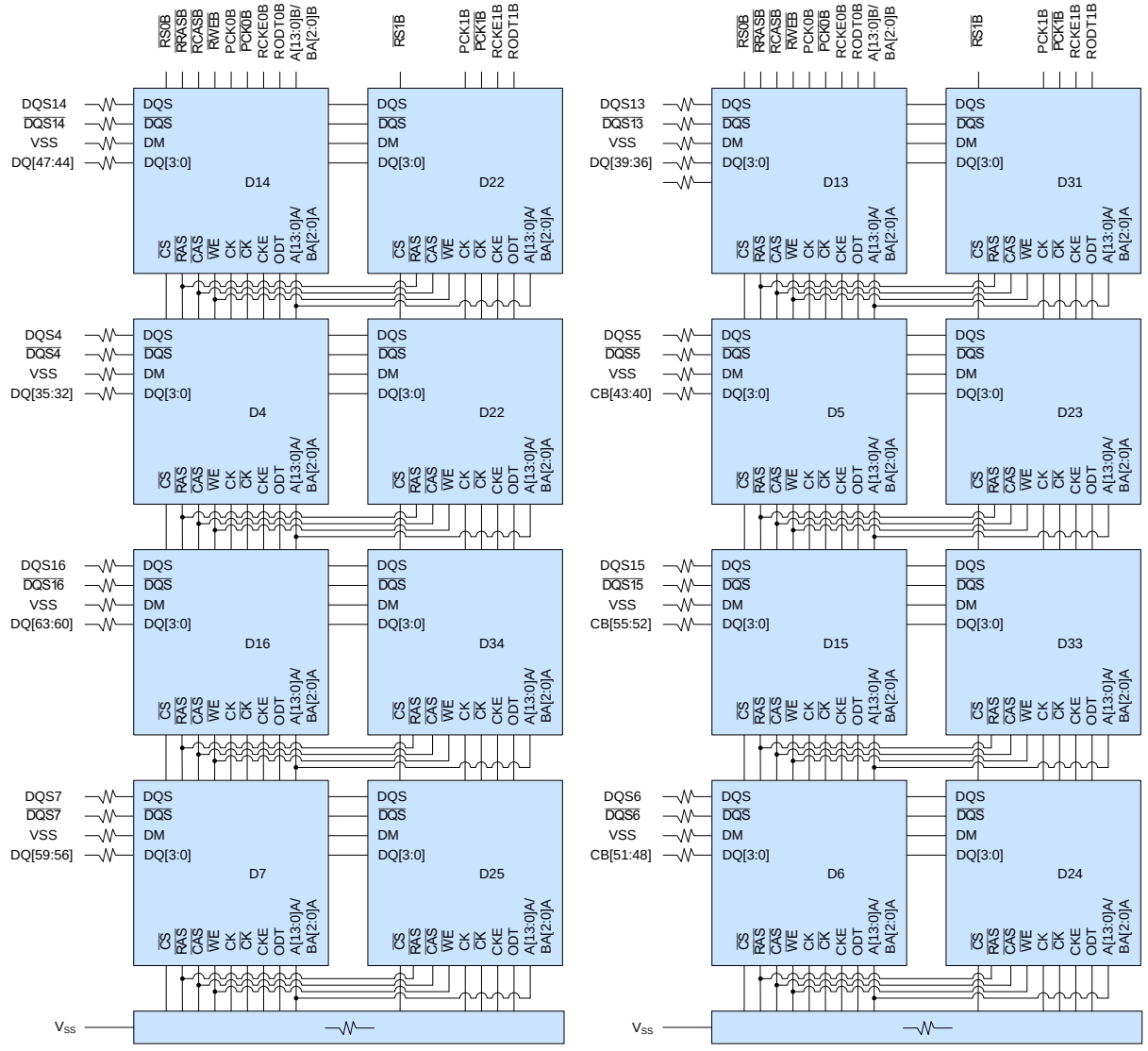
Functional Block Diagram (Part 1 of 3)

[8GB – 2 Ranks, 512Mx4 DDR3 SDRAMs]



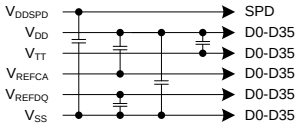
Functional Block Diagram (Part 2 of 3)

[8GB – 2 Ranks, 512Mx4 DDR3 SDRAMs]

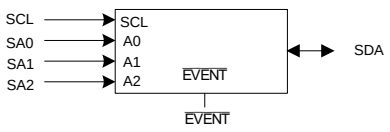


Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ pins of each SDRAM are connected to individual RZQ resistors (240Ω ± 1%).
3. See the wiring diagrams for resistor values.

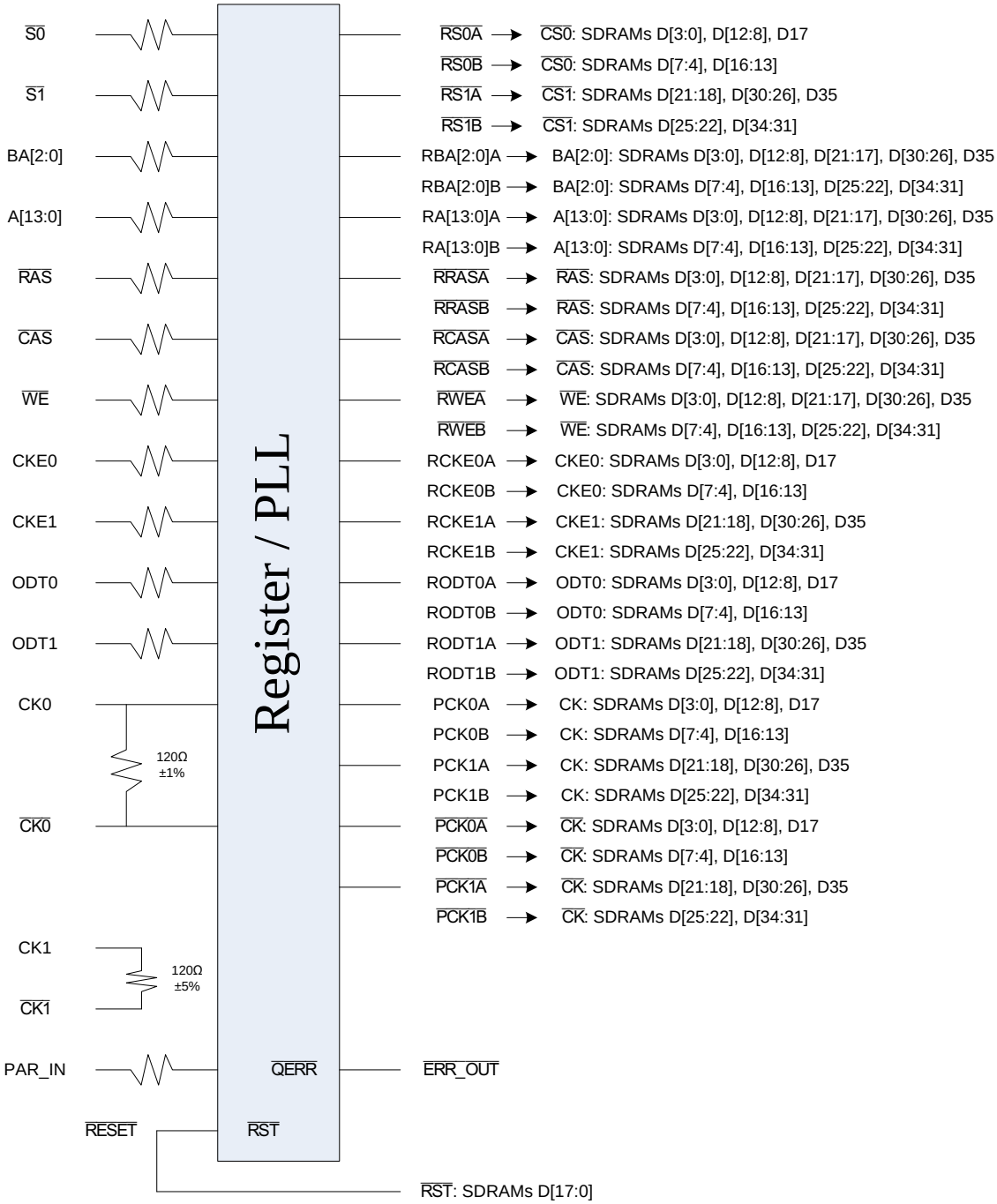


SPD w/ Integrated Thermal Sensor



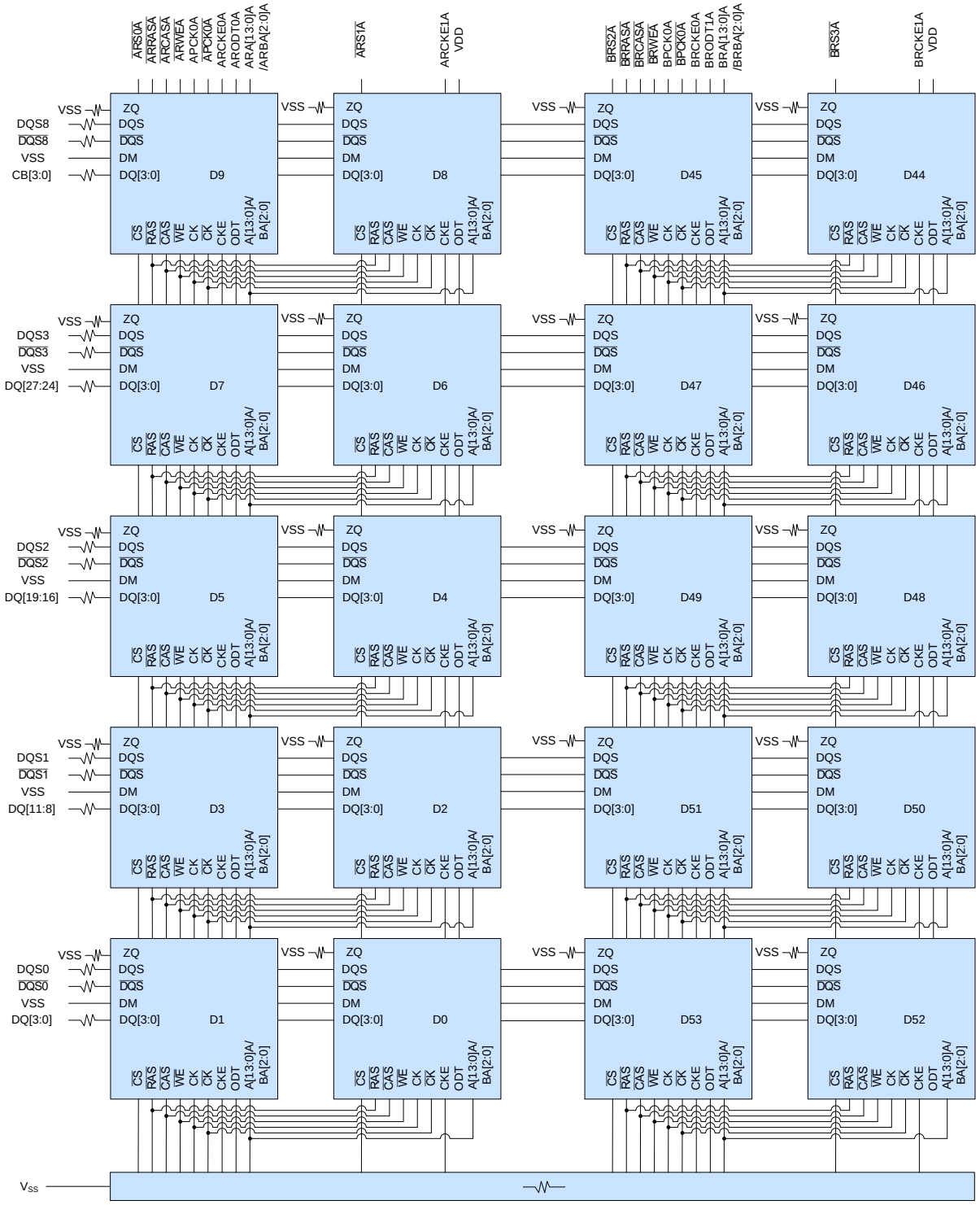
Functional Block Diagram (Part 3 of 3)

[8GB – 2 Ranks, 512Mx4 DDR3 SDRAMs]



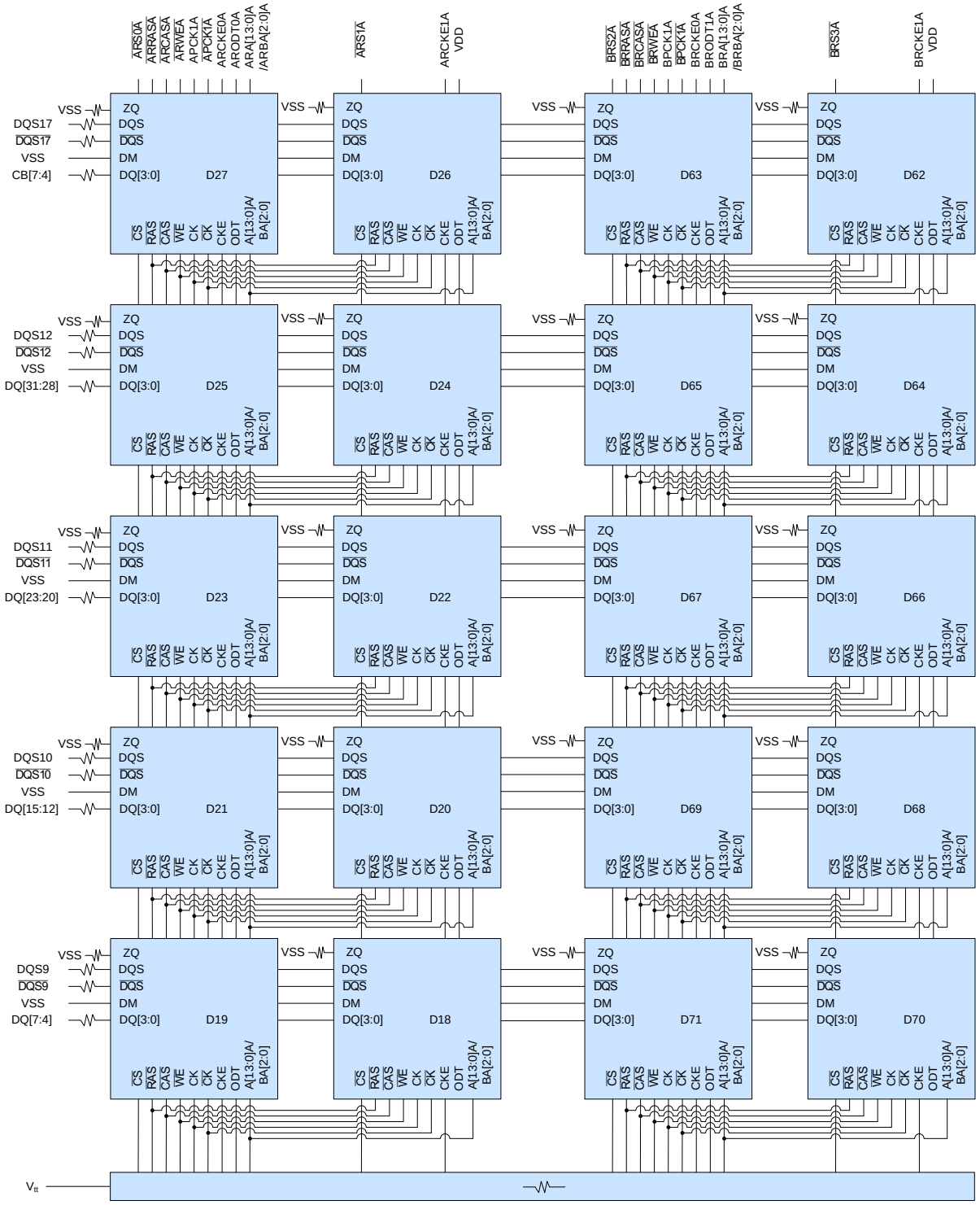
Functional Block Diagram (Part 1 of 5)

[16GB – 4 Ranks, 1Gx4 (DDP) DDR3 SDRAMs]



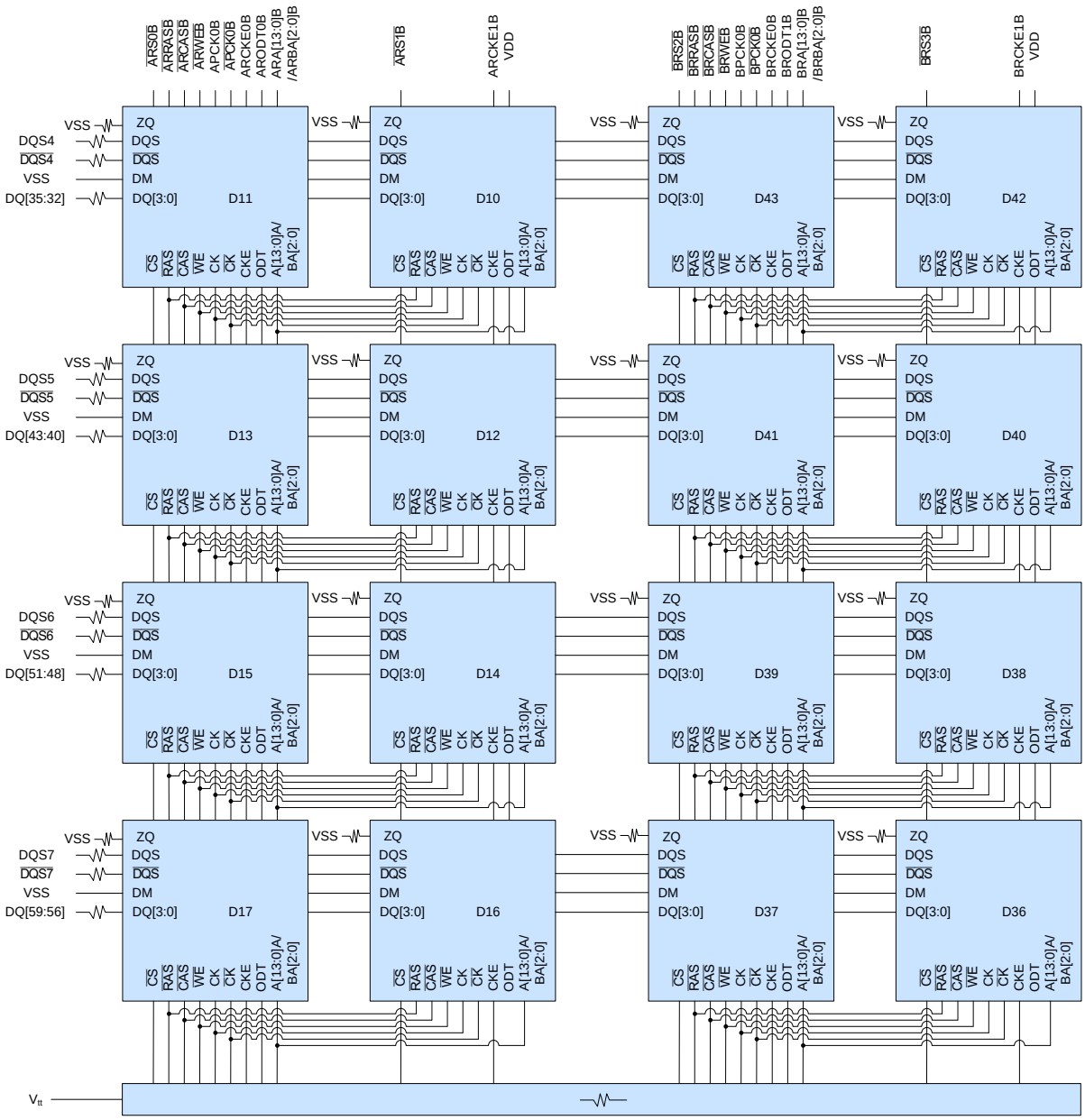
Functional Block Diagram (Part 2 of 5)

[16GB – 4 Ranks, 1Gx4 (DDP) DDR3 SDRAMs]



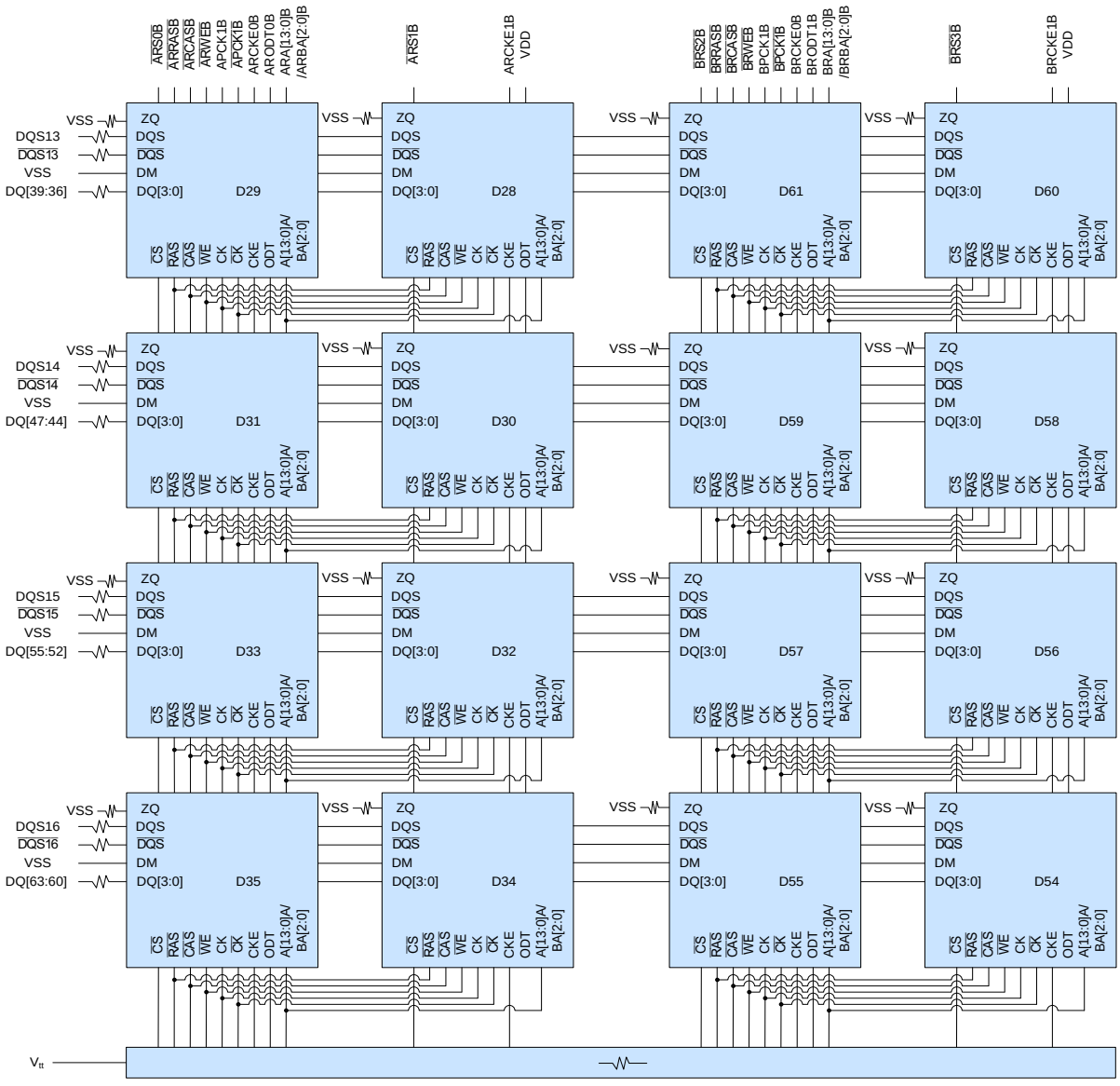
Functional Block Diagram (Part 3 of 5)

[16GB – 4 Ranks, 1Gx4 (DDP) DDR3 SDRAMs]



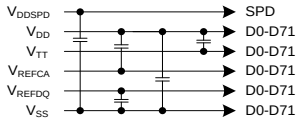
Functional Block Diagram (Part 4 of 5)

[16GB – 4 Ranks, 1Gx4 (DDP) DDR3 SDRAMs]



Notes :

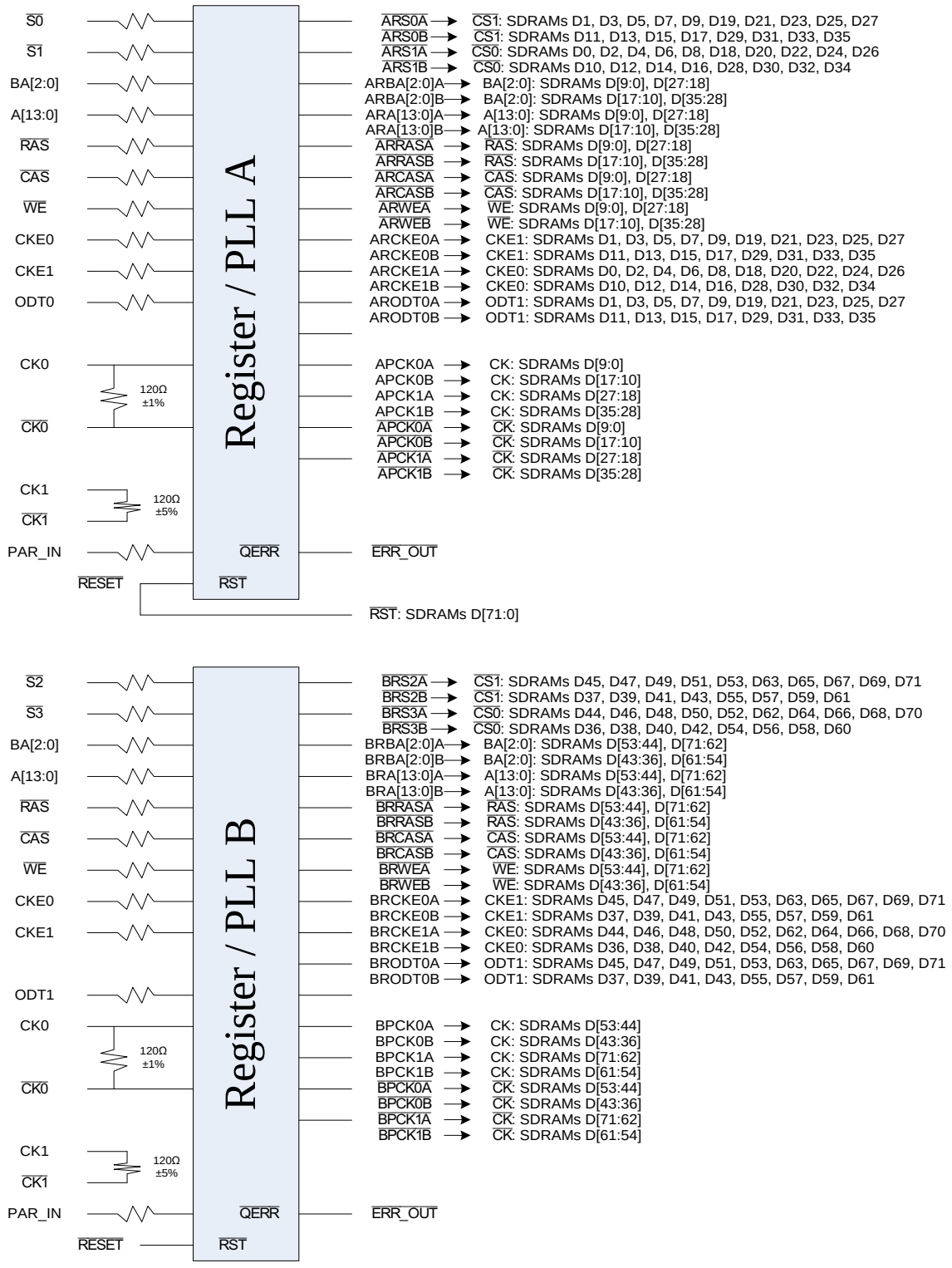
1. DQ-to-I/O wiring is may be changed within a nibble.
2. Resistor values are 15Ω ± 5%.
3. ZQ resistors are 240Ω ± 1%.
4. See the wiring diagrams for resistor values.



SPD w/ Integrated Thermal Sensor

Functional Block Diagram (Part 5 of 5)

[16GB – 4 Ranks, 1Gx4 (DDP) DDR3 SDRAMs]



Environmental Requirements

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:
1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature shall not exceed the value specified in the component spec.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
V_{DD}	Voltage on VDD pins relative to Vss	-0.4 V ~ 1.975 V	V	1, 3
V_{DDQ}	Voltage on VDDQ pins relative to Vss	-0.4 V ~ 1.975 V	V	1, 3
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1, 2
	Extended Temperature Range (Optional)	85 to 95	°C	1, 3

Note:
1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Output Supply Voltage	1.425	1.5	1.575	V	1,2

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Units	Note
		Min.	Max.	Min.	Max.		
VIH.CA(DC)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.CA(DC)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.CA(AC)	AC Input Logic High	Vref + 0.175	Note 2	Vref + 0.175	Note 2	V	1, 2
VIL.CA(AC)	AC Input Logic Low	Note 2	Vref - 0.175	Note 2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC Input Logic High	-	-	Vref + 0.15	Note 2	V	1, 2
VIL.CA(AC150)	AC Input Logic Low	-	-	Note 2	Vref - 0.15	V	1, 2
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:
1. For input only pins except $\overline{RESET}$. Vref = VrefCA(DC).
2. See “Overshoot and Undershoot Specifications” in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Units	Note
		Min.	Max.	Min.	Max.		
VIH.DQ(DC)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.DQ(DC)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.DQ(AC)	AC Input Logic High	Vref + 0.175	Note 2	Vref + 0.15	Note 2	V	1, 2, 5
VIL.DQ(AC)	AC Input Logic Low	Note 2	Vref - 0.175	Note 2	Vref - 0.15	V	1, 2, 5
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:
1. For input only pins except $\overline{RESET}$. Vref = VrefDQ(DC).
2. See “Overshoot and Undershoot Specifications” in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. Single-ended swing requirement for DQS, DQS# is 350 mV (peak to peak). Differential swing requirement for DQS - DQS# is 700 mV (peak to peak).

Speed Bins

Speed Bin			DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit
CL-nRCD-nRP			7-7-7		9-9-9		
Parameter		Symbol	min	max	min	max	
Internal read command to first data		tAA	13.125	20	13.5	20	ns
ACT to internal read or write delay		tRCD	13.125	-	13.5	-	ns
PRE command period		tRP	13.125	-	13.5	-	ns
ACT to ACT or REF command period		tRC	50.625	-	49.5	-	ns
ACT to PRE command period		tRAS	37.5	9*tREFI	36	9*tREFI	ns
CL	CWL						
6	5	tCK(avg)	2.5	3.3	2.5	3.3	ns
	6	tCK(avg)	Reserved		Reserved		ns
	7,8	tCK(avg)	Reserved		Reserved		ns
7	5	tCK(avg)	Reserved		Reserved		ns
	6	tCK(avg)	1.875	<2.5	Reserved		ns
	7,8	tCK(avg)	Reserved		Reserved		ns
8	5	tCK(avg)	Reserved		Reserved		ns
	6	tCK(avg)	1.875	<2.5	1.875	<2.5	ns
	7	tCK(avg)	Reserved		Reserved		ns
9	5,6	tCK(avg)	Reserved		Reserved		ns
	7	tCK(avg)	Reserved		1.5	<1.875	ns
	8	tCK(avg)	Reserved		Reserved		ns
Supported CL settings			6,7,8		6,8,9		nCK
Supported CWL settings			5,6		5,6,7		nCK

AC Timing Specifications for DDR3 SDRAM Devices Used on Module

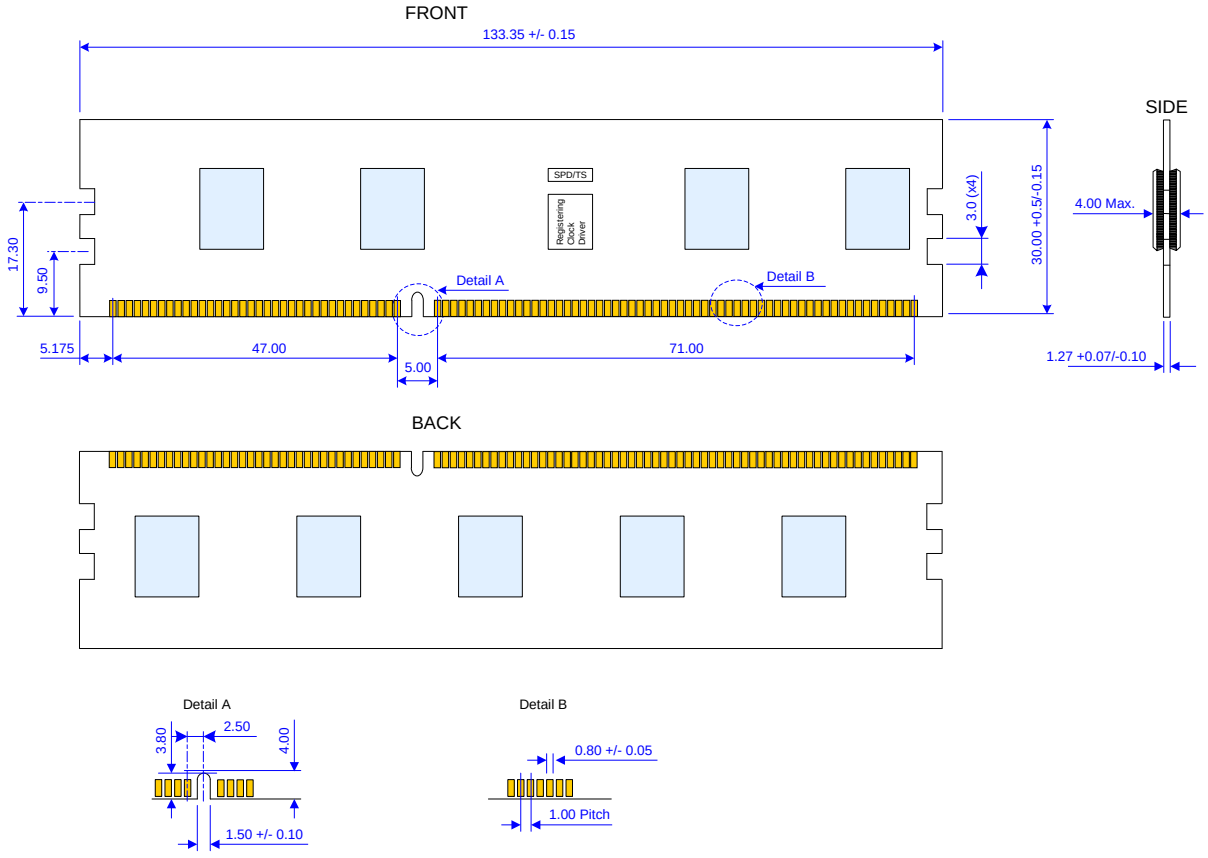
Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit
		min	max	min	max	
Clock Timing						
tCK(DLL_OF	Minimum Clock Cycle Time (DLL off mode)	8	-	8	-	ns
tCK(avg)	Average Clock Period(Refer to "Standard Speed					
tCH(avg)	Average high pulse width	0.47	0.53	0.47	0.53	tCK(avg)
tCL(avg)	Average low pulse width	0.47	0.53	0.47	0.53	tCK(avg)
tCK(abs)	Absolute Clock Period	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps
tCH(abs)	Absolute high pulse width	0.43	-	0.43	-	tCK(avg)
tCL(abs)	Absolute low pulse width	0.43	-	0.43	-	tCK(avg)
JIT(per)	Clock Period Jitter	-90	90	-80	80	ps
tJIT(per,lck)	Clock Period Jitter during DLL locking period	-80	80	-70	70	ps
tJIT(cc)	Cycle to Clcyle Period Jitter	180		160		ps
tJIT(cc,lck)	Cycle to Cycle Period Jitter	160		140		ps
tERR(2per)	Cumulative error accross 2 cycles	-132	132	-118	118	ps
tERR(3per)	Cumulative error accross 3 cycles	-157	157	-140	140	ps
tERR(4per)	Cumulative error accross 4cycles	-175	175	-155	155	ps
tERR(5per)	Cumulative error accross 5cycles	-188	188	-168	168	ps
tERR(6per)	Cumulative error accross 6 cycles	-200	200	-177	177	ps
tERR(7per)	Cumulative error accross 7 cycles	-209	209	-186	186	ps
tERR(8per)	Cumulative error accross 8 cycles	-217	217	-193	193	ps
tERR(9per)	Cumulative error accross 9 cycles	-224	224	-200	200	ps
tERR(10per)	Cumulative error accross 10 cycles	-231	231	-205	205	ps
tERR(11per)	Cumulative error accross 11 cycles	-237	237	-210	210	ps
tERR(12per)	Cumulative error accross 12 cycles	-242	242	-215	215	ps
tERR(nper)	Cumulative error accross n=13,14,..,49,50 cycles	tERR(npr)min = (1+ 0.68ln(n)) * tJIT(per)min	tERR(npr)max = (1+ 0.68ln(n)) * tJIT(per)max	tERR(npr)min = (1+ 0.68ln(n)) * tJIT(per)min	tERR(npr)max = (1+ 0.68ln(n)) * tJIT(per)max	ps
Data Timing						
tDQSQ	DQS, DQS to DQ skew per group, per access	-	150	-	125	ps
tQH	DQ output hold time from DQS, DQS	0.38	-	0.38	-	tCK(avg)
tLZ(DQ)	DQ low-impedence time from CK / $\overline{CK}$	-600	300	-500	250	ps
tHZ(DQ)	DQ high-impedence time from CK / $\overline{CK}$	-	300	-	250	ps
tDS(base)	Data Setup time to DQS, DQS referenced to Vih(ac)/ Vil(ac) levels	25		30		ps
tDH(base)	Data Hold time to DQS, DQS referenced to Vih(dc)/ Vil(dc) levels	100		65		ps
Data Strobe Timing						
tRPRE	DQS, DQS differential READ Preamble	0.9	-	0.9	-	tCK(avg)
tRPST	DQS, DQS differential READ Postamble	0.3	-	0.3	-	tCK(avg)
tQSH	DQS, DQS differential output high time	0.38	-	0.4	-	tCK(avg)
tQSL	DQS, DQS differential output low time	0.38	-	0.4	-	tCK(avg)
tWPRE	DQS, DQS differential WRITE Preamble	0.9	-	0.9	-	tCK(avg)
tWPST	DQS, DQS differential WRITE Postamble	0.3	-	0.3	-	tCK(avg)
tDQSCK	DQS, DQS rising edge output access time from rising CK, $\overline{CK}$	-300	300	-255	255	ps
tLZ(DQS)	DQS, DQS low-impedance time (Referenced from	-600	300	-500	250	ps
tHZ(DQS)	DQS, DQS high-impedance time (Referenced from RL+BL/2)	-	300	-	250	ps
tDQSL	DQS, DQS differential input low pulse width	0.45	0.55	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS differential input high pulse width	0.45	0.55	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS rising edge to CK, $\overline{CK}$ rising edge	-0.25	0.25	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS falling edge setup time to CK, $\overline{CK}$ rising edge	0.2	-	0.2	-	tCK(avg)
tDSH	DQS, DQS falling edge hold time to CK, $\overline{CK}$ rising	0.2	-	0.2	-	tCK(avg)

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit
		min	max	min	max	
Command and Address Timing						
tDLLK	DLL Locking time	512	-	512	-	nCK
tRTP	Internal READ command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to internal read command	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	
tCCD	CAS to CAS command delay	4	-	4	-	nCK
tDAL	Auto Precharge write recovery + precharge time	WR + roundup (tRP/tCK(avg))		WR + roundup (tRP/tCK(avg))		nCK
tMPRR	End of MPR Read burst to MSR for MPR (exit)	1	-	1	-	nCK
tRRD	ACTIVE to ACTIVE command period (1k page size -x4/x8)	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period (2k page size -x16)	max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-	
tFAW	Four activate window (1k page size - x4/x8)	37.5	-	30	0	ns
tFAW	Four activate window (2k page size - x16)	50	-	45	0	ns
tIS(base)	Command and Address setup time to CK, $\overline{CK}$ referenced Vih(ac) / Vil(ac) levels	125		65		ps
tIH(base)	Command and Address hold time from CK, $\overline{CK}$ referenced Vih(ac) / Vil(ac) levels	200		140		ps
tIS(base) AC150	Commad and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	-	-	65+125		ps
Calibration Timing						
tZQinit	Power-up and RESET calibration time	512	-	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	256	-	nCK
tZQCS	normal operation Short calibration time	64	-	64	-	nCK
Reset Timing						
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, tRFC(min) +10ns)	-	max(5nCK, tRFC(min) +10ns)	-	
Self RefreshTimings						
tXS	Exit Self Refresh to Commands not requiring a locked DLL	max(5nCK, tRFC(min) +10ns)	-	max(5nCK, tRFC(min) +10ns)	-	
tXSDLL	Exit Self Refresh to Commands requiring a locked	tDLLK(min)	-	tDLLK(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power Down Entry (PDE)	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit(SRX) or Power-Down Exit (PDX) or Reset Exit	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Power Down Timings						
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 7.5ns)	-	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	
tCKE	CKE minimm pulse width	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	
tCPDED	Command Pass disable delay	1	-	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9tREFI	tCKE(min)	9tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down	1	-	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL + 4 + 1	-	RL + 4 + 1	-	nCK

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit
		min	max	min	max	
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	tMOD(min)	-	
ODT Timings						
tODTH4	ODT high time without write command or with write command and BC4	4	-	4	-	nCK
tODTH8	ODT high time without write command oand BL8	6	-	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	1	9	1	9	ns
tAOFPD	Asynchronous RTT turn-off delay (Power Down with DLL frozen)	1	9	1	9	ns
tAON	RTT turn-on	-300	300	-250	250	ps
tAOF	RTT_NOM and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timings						
tWLMRD	First DQS/DQS rising edge after write leveling mode is programmed	40	-	40	-	nCK
tWLDQSEN	DQS/DQS delay after write leveling mode is	25	-	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	245	-	195	-	ps
tWLH	Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	245	-	195	-	ps
tWLO	Write leveling output delay	0	9	0	9	ns
tWLOE	Write levleing output error	0	2	0	2	ns
tRFC	REF command to ACT or REF command time	110		110		ns
tREFI	Average period refresh interval (0°C ≤ tCASE ≤ 85°C)	7.8		7.8		us
tREFI	Average period refresh interval (85°C < tCASE ≤ 95°C)	3.9		3.9		us

Package Dimensions

[2GB – 1 Rank, 256Mx8 DDR3 SDRAMs]

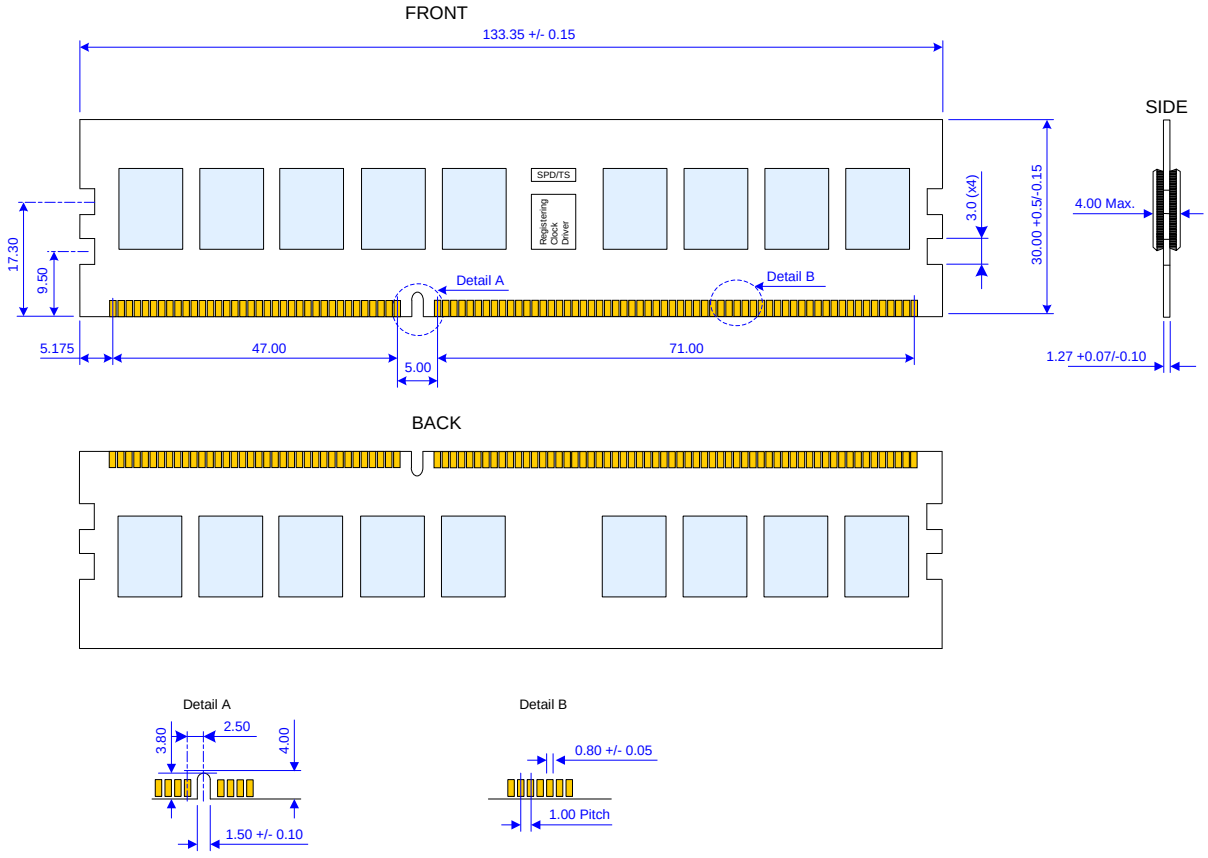


Units: Millimeters

Note: Device position and scale are only for reference.

Package Dimensions

[4GB – 2 Ranks, 256Mx8 DDR3 SDRAMs]

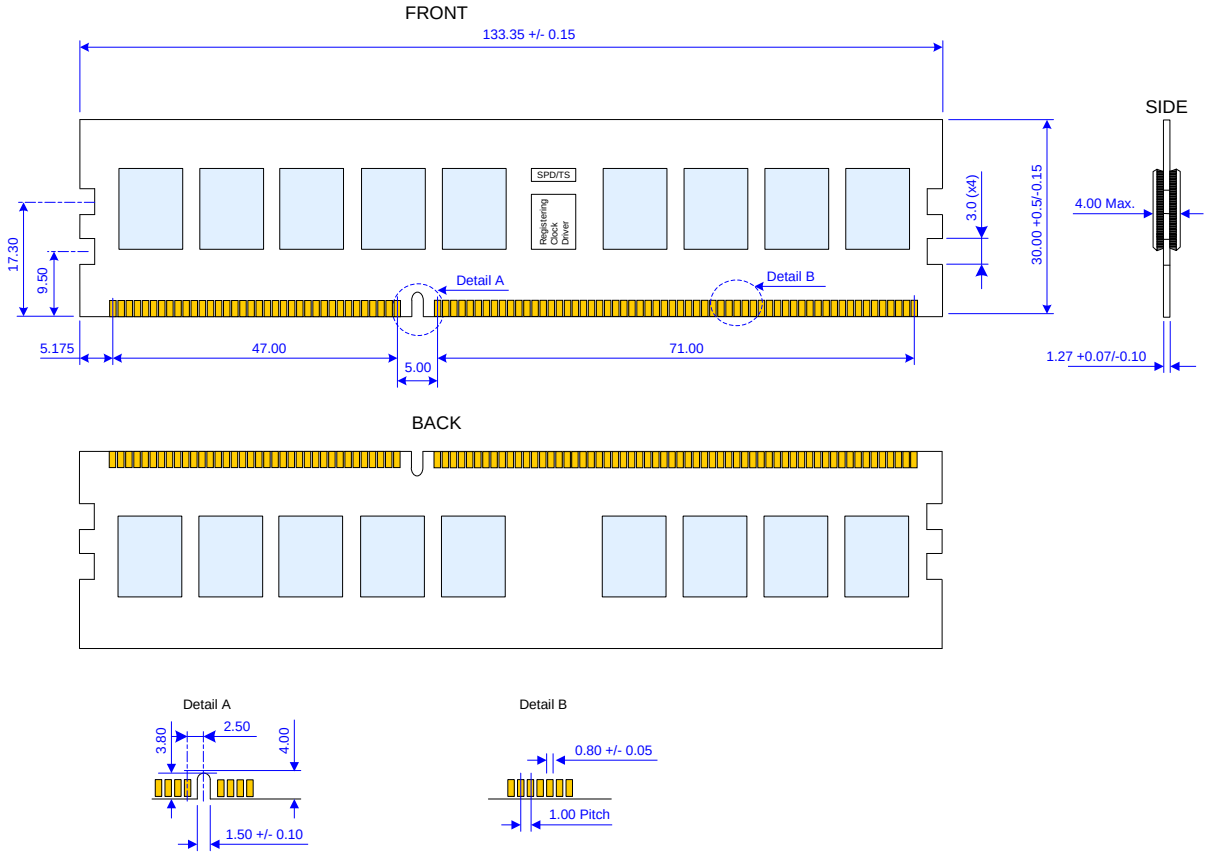


Units: Millimeters

Note: Device position and scale are only for reference.

Package Dimensions

[4GB – 1 Rank, 512Mx4 DDR3 SDRAMs]

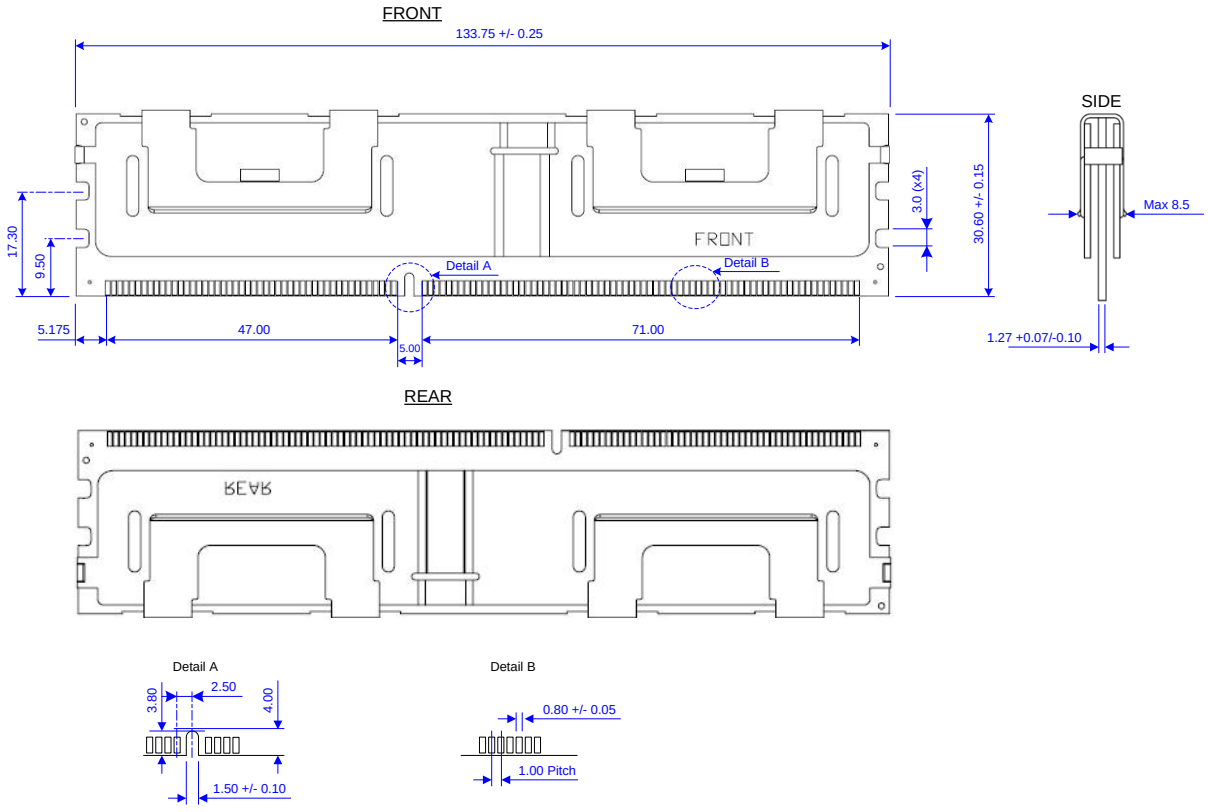


Units: Millimeters

Note: Device position and scale are only for reference.

Package Dimensions

[8GB – 2 Ranks, 512Mx4 DDR3 SDRAMs]

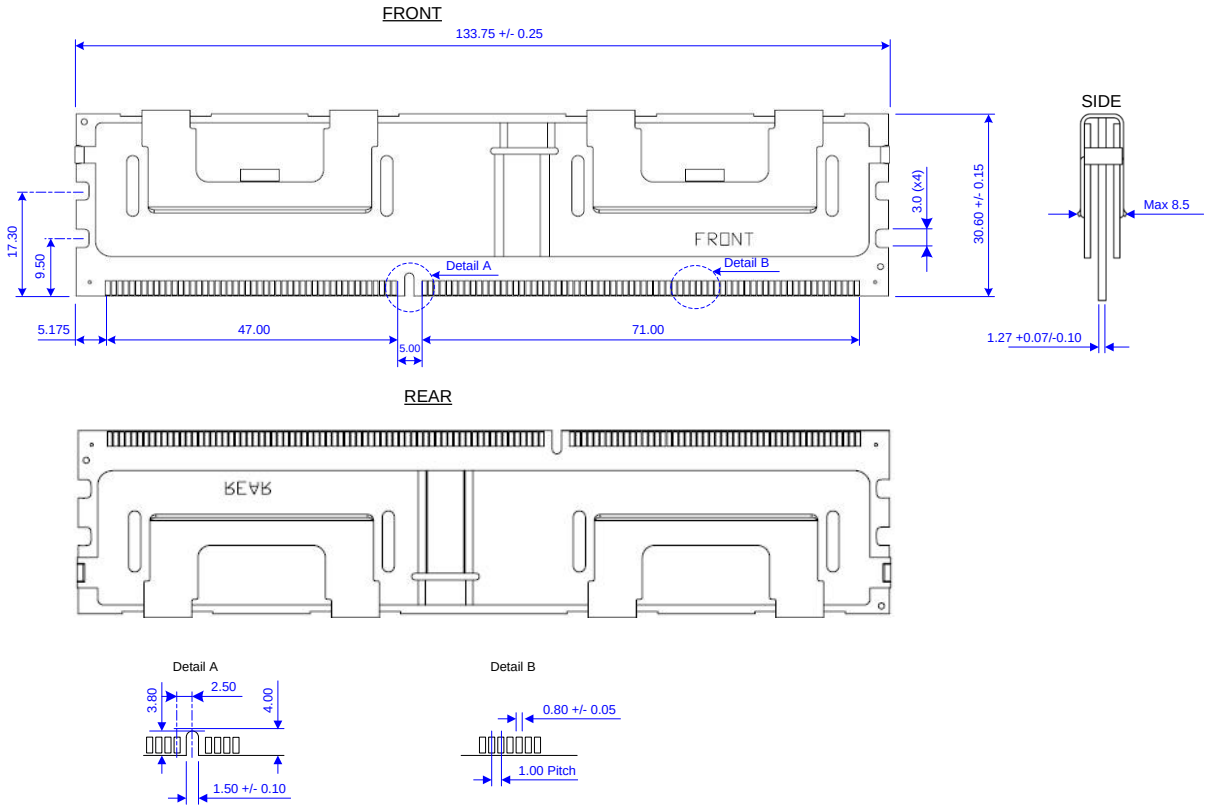


Units: Millimeters

Note: Device position and scale are only for reference.

Package Dimensions

[16GB – 4 Ranks, 1Gx4 (DDP) DDR3 SDRAMs]



Units: Millimeters

Note: Device position and scale are only for reference.

Revision Log

Rev	Date	Modification
0.1	02/2010	Preliminary Release

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