200 pin Unbuffered DDR SO-DIMM

Based on DDR333 512Mb bit B Die device

Features

- 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- Unbuffered DDR SO-DIMM based on 110nm 512M bit die B device, organized as 64Mx8 and 32Mx16 DDR SDRAM
- Performance:

	PC2700	Unit
Speed Sort	6K	
DIMM $\overline{CAS}$ Latency	2.5	
f_{CK} Clock Frequency	166	MHz
t_{CK} Clock Cycle	6	ns
f_{DQ} DQ Burst Frequency	333	MHz

- Intended for 166 MHz applications
- Inputs and outputs are SSTL-2 compatible
- $V_{DD} = V_{DDQ} = 2.5V \pm 0.2V$
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 2, 2.5
  - Burst Type: Sequential or Interleave
  - Burst Length: 2, 4, 8
  - Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 7.8 µs Max. Average Periodic Refresh Interval
- Serial Presence Detect EEPROM
- Gold contacts on module PCB
- Available in “Green” packaging (lead & halogen free)

Description

NT1GD64S8HB0FM, NT512D64SH8B0GM, NT256D64SH4B0GM, NT1GD64S8HB0FN, NT512D64SH8B0GN, and NT256D64SH4B0GN are un-buffered 200-Pin Double Data Rate (DDR) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM). All devices on these modules are based on Nanya’s 110nm die B generation of 512M bit devices. NT1GD64S8HB0FN, NT512D64SH8B0GN and NT256D64SH4B0GN are the corresponding part numbers that are in “Green” packaging and they are identical in both physical and electrical characteristics as non-green parts.

The NT1GD64S8HB0FM and NT1GD64S8HB0FN are organized as two ranks of 64Mx64 high-speed memory array and use sixteen 64Mx8 DDR SDRAMs BGA packages. The NT512D64SH8B0GM and NT512D64SH8B0GN are organized as two ranks of 32Mx64 high-speed memory array and use eight 32Mx16 DDR SDRAMs TSOP packages. The NT256D64SH4B0GM and NT256D64SH4B0GN are organized a single rank of 32Mx64 high-speed memory array and use four 32Mx16 DDR SDRAMs TSOP packages.

The DIMMs are intended for use in applications operating up to 166 MHz clock speeds and achieves high-speed data transfer rates of up to 333 MHz. Prior to any access operation, the device $\overline{CAS}$ latency and burst type/ length/operation type must be programmed into the DIMM by address inputs and I/O inputs BA0 and BA1 using the mode register set cycle.

The SO-DIMM uses a serial EEPROM and through the use of a standard IIC protocol the serial presence-detect implementation (SPD) data can be accessed. The first 128 bytes of the SPD data are programmed with the module characteristics as defined by JEDEC.

Ordering Information

Part Number	Size	Speed			Power	Leads
NT1GD64S8HB0FM-6K	128Mx64	DDR333 Devices	PC2700 2.5-3-3	166MHz (6ns @ CL = 2.5) 133MHz (7.5ns @ CL = 2)	2.5V	Gold
NT512D64SH8B0GM-6K	64Mx64					
NT256D64SH4B0GM-6K	32Mx64					

"Green" Part Number	Size	Speed			Power	Leads
NT1GD64S8HB0FN-6K	128Mx64	DDR333 Devices	PC2700 2.5-3-3	166MHz (6ns @ CL = 2.5) 133MHz (7.5ns @ CL = 2)	2.5V	Gold (lead and halogen free)
NT512D64SH8B0GN-6K	64Mx64					
NT256D64SH4B0GN-6K	32Mx64					

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Pin Description

CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	Differential Clock Inputs.	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe	DM0-DM7	Input Data Mask
$\overline{CAS}$	Column Address Strobe	V_{DD}	Power
$\overline{WE}$	Write Enable	V_{DDQ}	Supply voltage for DQs
$\overline{S0}$, $\overline{S1}$	Chip Selects	V_{SS}	Ground
A0-A9, A11, A12	Address Inputs	NC	No Connect
A10/AP	Address Input/Auto-precharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
V_{REF}	Ref. Voltage for SSTL_2 inputs	SA0-2	Serial Presence Detect Address Inputs
V_{DDID}	V_{DD} Identification flag.	V_{DDSPD}	Serial EEPROM positive power supply

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{REF}	51	V_{SS}	52	V_{SS}	101	A9	102	A8	151	DQ42	152	DQ46
3	V_{SS}	4	V_{SS}	53	DQ19	54	DQ23	103	V_{SS}	104	V_{SS}	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	V_{DD}	156	V_{DD}
7	DQ1	8	DQ5	57	V_{DD}	58	V_{DD}	107	A5	108	A4	157	V_{DD}	158	$\overline{CK1}$
9	V_{DD}	10	V_{DD}	59	DQ25	60	DQ29	109	A3	110	A2	159	V_{SS}	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	V_{SS}	162	V_{SS}
13	DQ2	14	DQ6	63	V_{SS}	64	V_{SS}	113	V_{DD}	114	V_{DD}	163	DQ48	164	DQ52
15	V_{SS}	16	V_{SS}	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	$\overline{RAS}$	167	V_{DD}	168	V_{DD}
19	DQ8	20	DQ12	69	V_{DD}	70	V_{DD}	119	$\overline{WE}$	120	$\overline{CAS}$	169	DQS6	170	DM6
21	V_{DD}	22	V_{DD}	71	NC	72	NC	121	$\overline{S0}$	122	$\overline{S1}$	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	NC	74	NC	123	DU	124	DU	173	V_{SS}	174	V_{SS}
25	DQS1	26	DM1	75	V_{SS}	76	V_{SS}	125	V_{SS}	126	V_{SS}	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	DQS8	78	NC	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	NC	80	NC	129	DQ33	130	DQ37	179	V_{DD}	180	V_{DD}
31	DQ11	32	DQ15	81	V_{DD}	82	V_{DD}	131	V_{DD}	132	V_{DD}	181	DQ57	182	DQ61
33	V_{DD}	34	V_{DD}	83	NC	84	NC	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	V_{DD}	85	DU	86	DU	135	DQ34	136	DQ38	185	V_{SS}	186	V_{SS}
37	$\overline{CK0}$	38	V_{SS}	87	V_{SS}	88	V_{SS}	137	V_{SS}	138	V_{SS}	187	DQ58	188	DQ62
39	V_{SS}	40	V_{SS}	89	CK2	90	V_{SS}	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	$\overline{CK2}$	92	V_{DD}	141	DQ40	142	DQ44	191	V_{DD}	192	V_{DD}
43	DQ17	44	DQ21	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}	193	SDA	194	SA0
45	V_{DD}	46	V_{DD}	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	V_{DDSPD}	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	V_{SS}	150	V_{SS}	199	V_{DDID}	200	DU

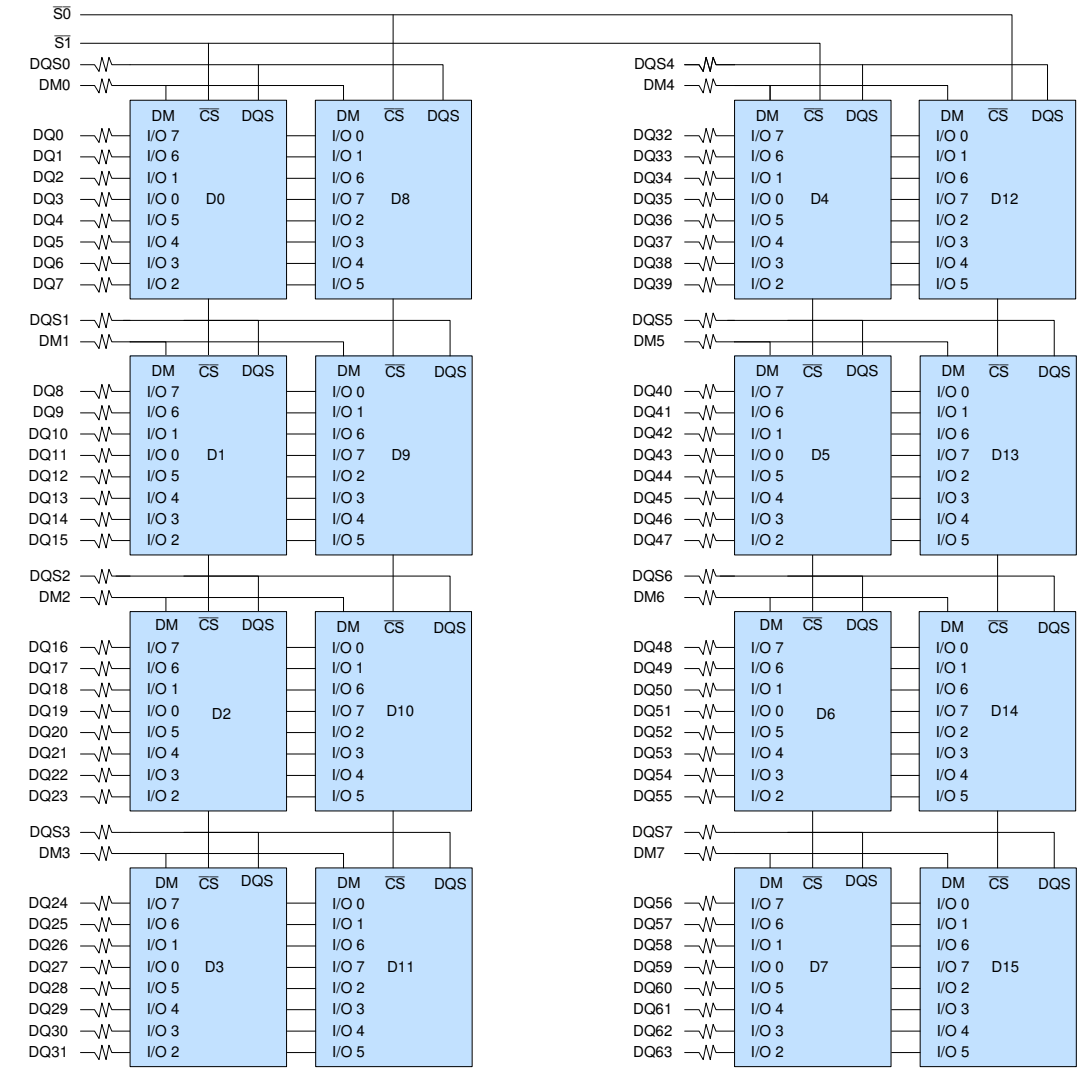
Note: All pin assignments are consistent for all 8-byte unbuffered versions.

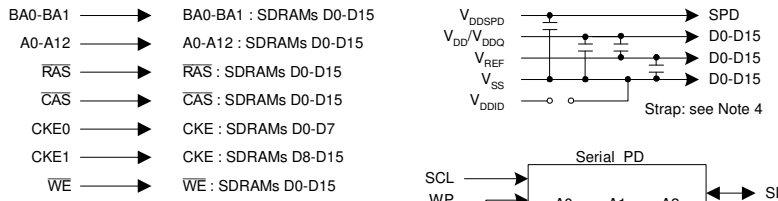
Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	(SSTL)	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	(SSTL)	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by S0; Bank 1 is selected by S1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11 - A13	(SSTL)	-	During a Bank Activate command cycle, these lines define the row address when sampled at the rising clock edge. During a Read or Write command cycle, these lines defines the column address when sampled at the rising clock edge. In addition to the column address, AP is used to invoke auto-precharge operation at the end of the Burst Read or Write cycle. If AP is high, auto-precharge is selected and BA0/BA1 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQS0 – DQS8	(SSTL)	Active High	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data. DQS8 is used for ECC modules (CB0-CB7) and is not used on x64 modules.
CB0 – CB7	(SSTL)	-	Data Check Bit Input/Output pins. Used on ECC modules and is not used on x64 modules.
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pull-up.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

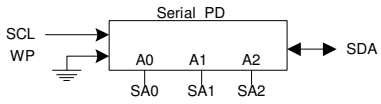
Functional Block Diagram

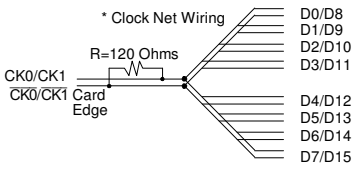
2 Ranks, 16 devices, 64Mx8 DDR SDRAMs (1GB)





Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	8 SDRAMs
CK1/CK1	8 SDRAMs
CK2/CK2	NC



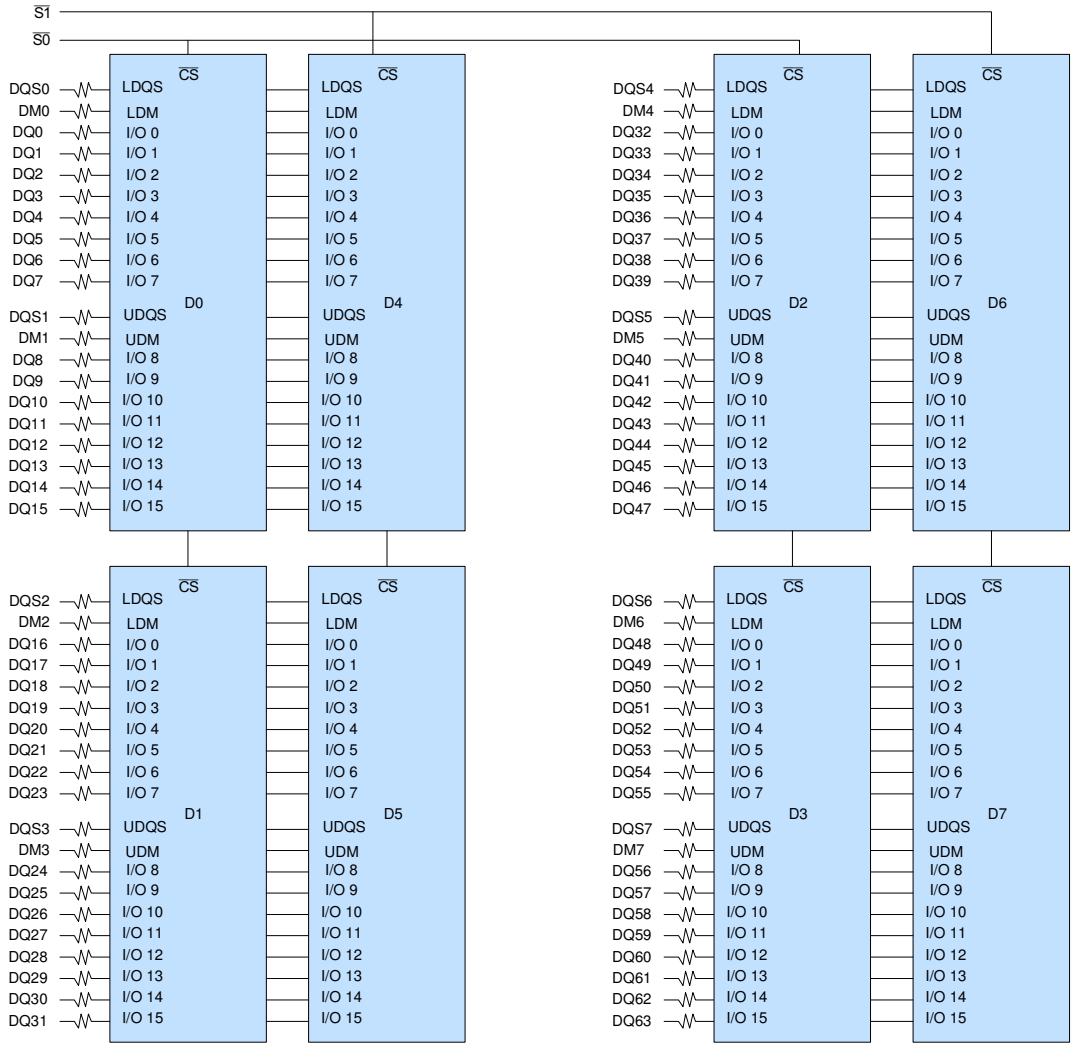


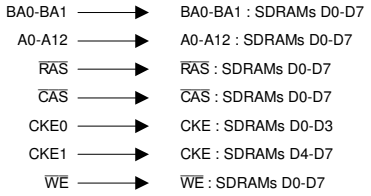
Notes :

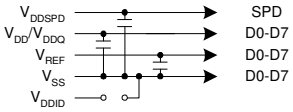
1. DQ-to-I/O wring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Functional Block Diagram

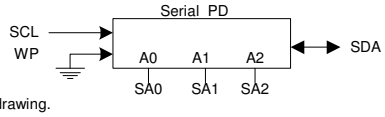
2 Ranks, 8 devices, 32Mx16 DDR SDRAMs (512MB)

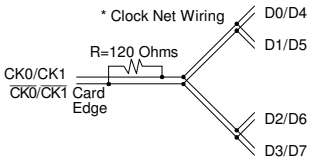






Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	4 SDRAMs
CK1/CK1	4 SDRAMs
CK2/CK2	NC



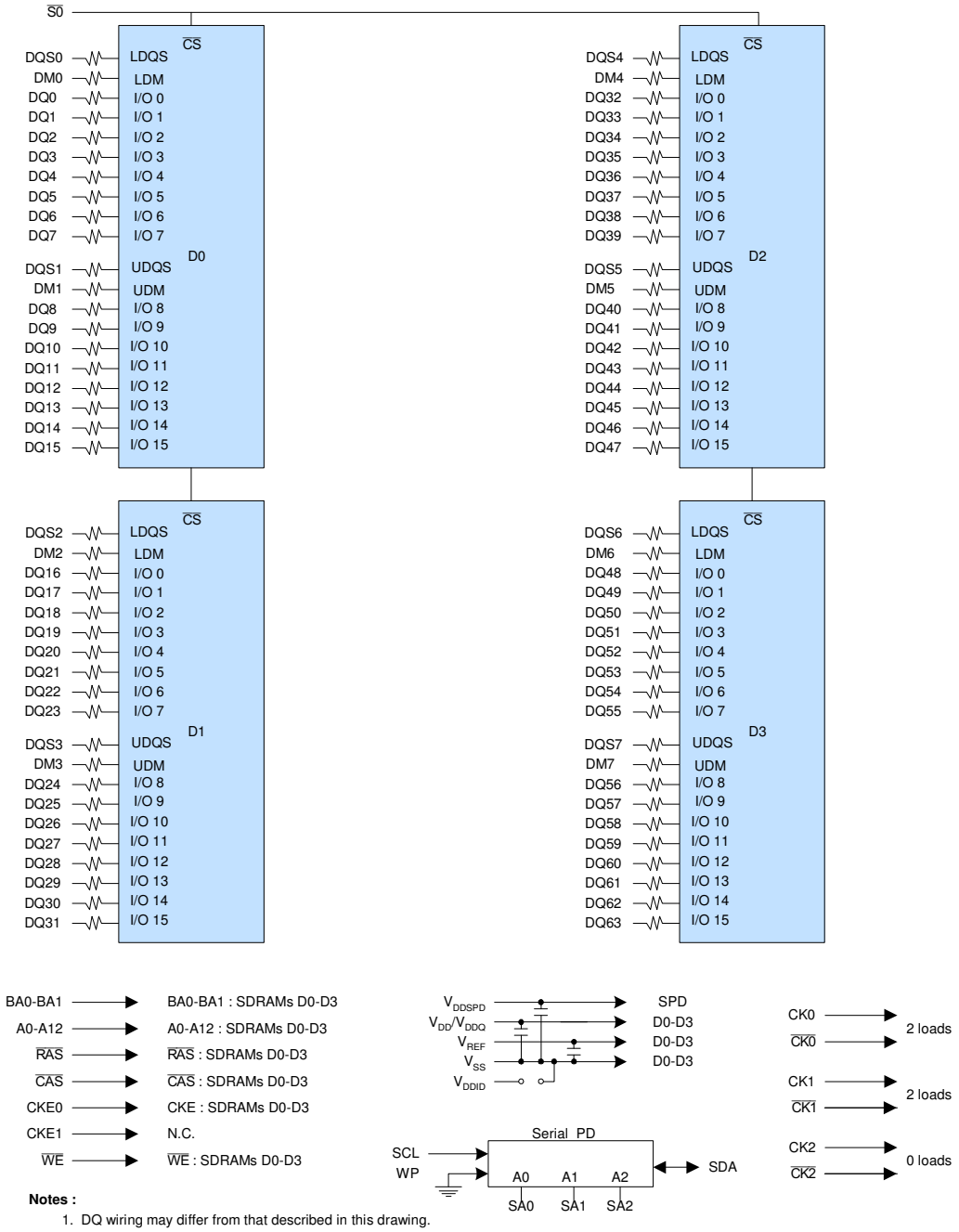


Notes :

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22+/- 5% Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Functional Block Diagram

1 Rank, 4 devices, 32Mx16 DDR SDRAMs (256MB)



Notes :

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22+/- 5% Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Serial Presence Detect

Byte	Description	Byte	Description
0	Number of Serial PD Bytes Written during Production	27	Minimum Row Precharge Time (t_{RP})
1	Total Number of Bytes in Serial PD device	28	Minimum Row Active to Row Active delay (t_{RRD})
2	Fundamental Memory Type	29	Minimum RAS to CAS delay (t_{RCD})
3	Number of Row Addresses on Assembly	30	Minimum RAS Pulse Width (t_{RAS})
4	Number of Column Addresses on Assembly	31	Module Bank Density
5	Number of DIMM Rank	32	Address and Command Setup Time Before Clock
6	Data Width of Assembly	33	Address and Command Hold Time After Clock
7	Data Width of Assembly (cont')	34	Data Input Setup Time Before Clock
8	Voltage Interface Level of this Assembly	35	Data Input Hold Time After Clock
9	DDR SDRAM Device Cycle Time CL=2.5	36-40	Reserved
10	DDR SDRAM Device Access Time from Clock CL=2.5	41	Minimum Active/Auto-refresh Time (t_{RC})
11	DIMM Configuration Type	42	Auto-refresh to Active/Auto-refresh Command Period (t_{RFC})
12	Refresh Rate/Type	43	Max Cycle Time ($t_{CK\ max}$)
13	Primary DDR SDRAM Width	44	Maximum DQS-DQ Skew Time (t_{DQSQ})
14	Error Checking DDR SDRAM Device Width	45	Maximum Read Data Hold Skew Factor (t_{QHS})
15	DDR SDRAM Device Attr: Min CLK Delay, Random Col Access	46	Reserved
16	DDR SDRAM Device Attributes: Burst Length Supported	47	Dimm Height
17	DDR SDRAM Device Attributes: Number of Device Banks	48-61	Reserved
18	DDR SDRAM Device Attributes: CAS Latencies Supported	62	SPD Revision
19	DDR SDRAM Device Attributes: CS Latency	63	Checksum Data
20	DDR SDRAM Device Attributes: WE Latency	64-71	Manufacturer's JEDEC ID Code
21	DDR SDRAM Device Attributes:	72	Module Manufacturing Location
22	DDR SDRAM Device Attributes: General	73-90	Module Part number
23	Minimum Clock Cycle CL=2.5	91-92	Module Revision Code
24	Maximum Data Access Time from Clock at CL=2	93-94	Module Manufacturing Data yy= Binary coded decimal year code, 0-99(Decimal), 00-63(Hex) ww= Binary coded decimal year code, 01-52(Decimal), 01-34(Hex)
25	Minimum Clock Cycle Time at CL=1	95-98	Module Serial Number
26	Maximum Data Access Time from Clock at CL=1	99-127	Reserved

SPD Values for NT1GD64S8HB0FM / NT1GD64S8HB0FN

	PC2700 (6K)	
Byte	Value	Hex
0	128	80
1	256	08
2	SDRAM DDR	07
3	13	0D
4	11	0B
5	2	02
6	x64	40
7	x64	00
8	SSTL 2.5V	04
9	6.0ns	60
10	7.0ns	70
11	Non-Parity	00
12	SR/1x(7.8us)	82
13	x8	08
14	N/A	00
15	1 Clock	01
16	2,4,8	0E
17	4	04
18	2/2.5	0C
19	0	01
20	1	02
21	Differential Clock	20
22	±0.2V Tolerance	C0
23	7.5ns	75
24	0.75ns	75
25	N/A	00
26	N/A	00
27	18ns	48
28	12ns	30
29	18ns	48
30	42ns	2A
31	512MB	80
32	0.75ns	75
33	0.75ns	75
34	0.45ns	45
35	0.45ns	45
36-40	Reserved	00
41	60ns	3C
42	72ns	48
43	12ns	30
44	0.40ns	28
45	0.50ns	50
46	Reserved	00
47	31.75mm	01
48-61	Reserved	00
62	SPD 1.0	10
63	Checksum	4E
64-71	NANYA	7F7F7F0B 00000000
72	Assembly	--
73-90	Module PN	--
91-92	Revision	--
93-94	Year/Week Code	--
95-98	Serial Number	--
99-255	Reserved	--

SPD Values for NT512D64SH8B0GM / NT512D64SH8B0GN

	PC2700 (6K)	
Byte	Value	Hex
0	128	80
1	256	08
2	SDRAM DDR	07
3	13	0D
4	10	0A
5	2	02
6	x64	40
7	x64	00
8	SSTL 2.5V	04
9	6.0ns	60
10	7.0ns	70
11	Non-Parity	00
12	SR/1x(7.8us)	82
13	x16	10
14	N/A	00
15	1 Clock	01
16	2,4,8	0E
17	4	04
18	2/2.5	0C
19	0	01
20	1	02
21	Differential Clock	20
22	±0.2V Tolerance	C0
23	7.5ns	75
24	0.75ns	75
25	N/A	00
26	N/A	00
27	18ns	48
28	12ns	30
29	18ns	48
30	42ns	2A
31	256MB	40
32	0.75ns	75
33	0.75ns	75
34	0.45ns	45
35	0.45ns	45
36-40	Reserved	00
41	60ns	3C
42	72ns	48
43	12ns	30
44	0.45ns	2D
45	0.55ns	55
46	Reserved	00
47	31.75mm	01
48-61	Reserved	00
62	SPD 1.0	10
63	Checksum	1F
64-71	NANYA	7F7F7F0B 00000000
72	Assembly	--
73-90	Module PN	--
91-92	Revision	--
93-94	Year/Week Code	--
95-98	Serial Number	--
99-255	Reserved	--

SPD Values for NT256D64SH4B0GM / NT256D64SH4B0GN

	PC2700 (6K)	
Byte	Value	Hex
0	128	80
1	256	08
2	SDRAM DDR	07
3	13	0D
4	10	0A
5	1	01
6	x64	40
7	x64	00
8	SSTL 2.5V	04
9	6.0ns	60
10	7.0ns	70
11	Non-Parity	00
12	SR/1x(7.8us)	82
13	x16	10
14	N/A	00
15	1 Clock	01
16	2,4,8	0E
17	4	04
18	2/2.5	0C
19	0	01
20	1	02
21	Differential Clock	C0
22	±0.2V Tolerance	00
23	7.5ns	75
24	0.75ns	75
25	N/A	00
26	N/A	00
27	18ns	48
28	12ns	30
29	18ns	48
30	42ns	2A
31	256MB	40
32	0.75ns	75
33	0.75ns	75
34	0.45ns	45
35	0.45ns	45
36-40	Reserved	00
41	60ns	3C
42	72ns	48
43	12ns	30
44	0.45ns	2D
45	0.55ns	55
46	Reserved	00
47	31.75mm	01
48-61	Reserved	00
62	SPD 1.0	10
63	Checksum	1E
64-71	NANYA	7F7F7F0B 00000000
72	Assembly	--
73-90	Module PN	--
91-92	Revision	--
93-94	Year/Week Code	--
95-98	Serial Number	--
99-255	Reserved	--

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to V_{SS}	-0.5 to V_{DDQ} +0.5	V
V_{IN}	Voltage on Input relative to V_{SS}	-0.5 to +3.6	V
V_{DD}	Voltage on V_{DD} supply relative to V_{SS}	-0.5 to +3.6	V
V_{DDQ}	Voltage on V_{DDQ} supply relative to V_{SS}	-0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	℃
T_{STG}	Storage Temperature (Plastic)	-55 to +150	℃
P_D	Power Dissipation (per device component)	1	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics and Operating Conditions

T_A = 0 ℃ ~ 70 ℃; V_{DDQ} = V_{DD} = 2.5V ± 0.2V

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	V_{REF} - 0.15	V	1
$V_{IN\ (DC)}$	Input Voltage Level, CK and $\overline{CK}$ Inputs	-0.3	V_{DDQ} + 0.3	V	1
$V_{ID\ (DC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
I_I	Input Leakage Current Any input 0V ≤ V_{IN} ≤ V_{DD}; (All other pins not under test = 0V)	-10	10	µA	1
I_{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ Vout ≤ V_{DDQ}	-10	10	µA	1
I_{OH}	Output High Current (V_{OUT} = V_{DDQ} -0.373V, min V_{REF}, min V_{TT})	-16.8	-	mA	1
I_{OL}	Output Low Current (V_{OUT} = 0.373, max V_{REF}, max V_{TT})	16.8	-	mA	1

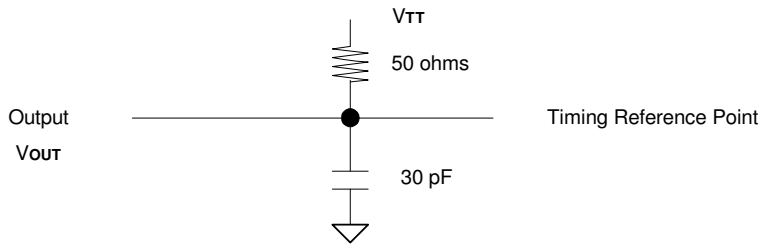
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

AC Characteristics

Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, IDD, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and IDD tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between $V_{IL\,(AC)}$ and $V_{IH\,(AC)}$ unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuits



AC Operating Conditions

T_A = 0 ℃ ~ 70 ℃; V_{DDQ} = V_{DD} = 2.5V ± 0.2V

Symbol	Parameter/Condition	Min	Max	Unit	Notes
$V_{IH\,(AC)}$	Input High (Logic 1) Voltage.	V_{REF} + 0.31		V	1, 2
$V_{IL\,(AC)}$	Input Low (Logic 0) Voltage.		V_{REF} - 0.31	V	1, 2
$V_{ID\,(AC)}$	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
$V_{IX\,(AC)}$	Input Differential Pair Cross Point Voltage, CK and $\overline{CK}$ Inputs	(0.5* V_{DDQ}) - 0.2	(0.5* V_{DDQ}) + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

T_A = 0 ℃ ~ 70 ℃; V_{DDQ} = V_{DD} = 2.5V ± 0.2V

Symbol	Parameter/Condition	Notes
IDD0	Operating Current: one bank; active/precharge; t_{RC} = $t_{RC\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1,2
IDD1	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = $t_{RC\ (MIN)}$; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA; address and control inputs changing once per clock cycle	1,2
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	1,2
IDD2N	Idle Standby Current: CS ≥ $V_{IH\ (MIN)}$; all banks idle; CKE ≥ $V_{IH\ (MIN)}$; t_{CK} = $t_{CK\ (MIN)}$; address and control inputs changing once per clock cycle	1,2
IDD3P	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ $V_{IL\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$	1,2
IDD3N	Active Standby Current: one bank; active/precharge; CS ≥ $V_{IH\ (MIN)}$; CKE ≥ $V_{IH\ (MIN)}$; t_{RC} = $t_{RAS\ (MAX)}$; t_{CK} = $t_{CK\ (MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1,2
IDD4R	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = $t_{CK\ (MIN)}$; I_{OUT} = 0mA	1,2
IDD4W	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = $t_{CK\ (MIN)}$	1,2
IDD5	Auto-Refresh Current: t_{RC} = $t_{RFC\ (MIN)}$	1,2,3
IDD6	Self-Refresh Current: CKE ≤ 0.2V	1,2
IDD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = $t_{RC\ (min)}$; I_{OUT} = 0mA.	1,2

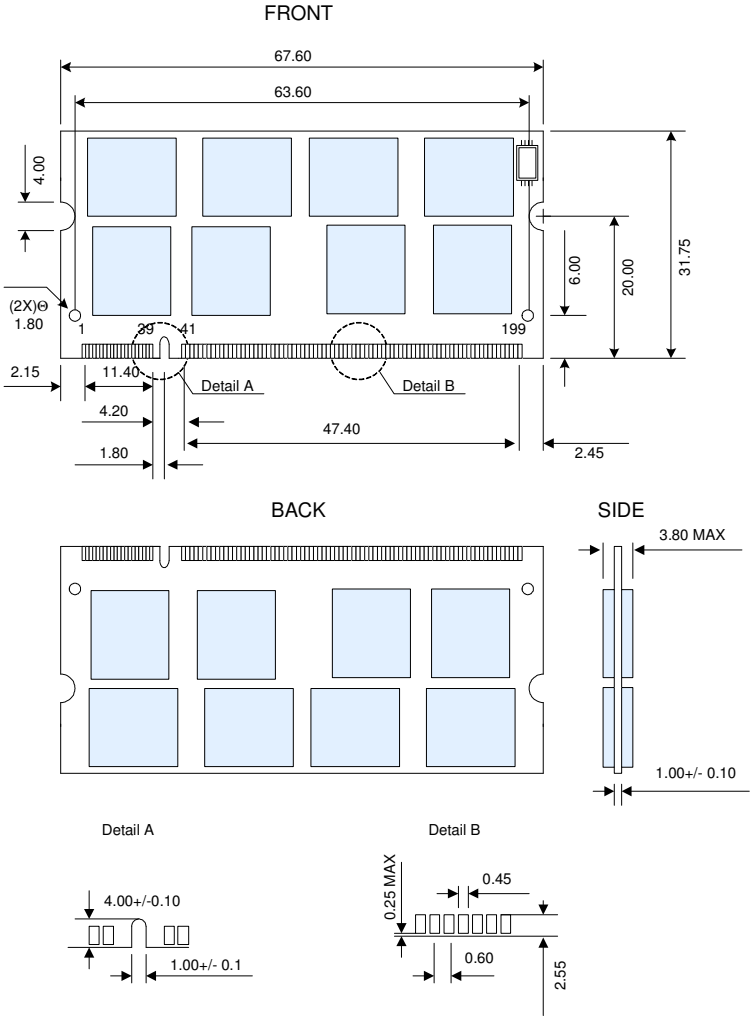
1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ ns.
3. Current at 7.8 µs is time averaged value of IDD5 at $t_{RFC\ (MIN)}$ and IDD2P over 7.8 µs.

All IDD current values are calculated from device level.

	NT1GD64S8HB0FM NT1GD64S8HB0FN	NT512D64SH8B0GM NT512D64SH8B0GN	NT256D64SH4B0GM NT256D64SH4B0GN	
Symbol	PC2700 (6K)	PC2700 (6K)	PC2700 (6K)	
IDD0	1575	810	382	mA
IDD1	1634	839	397	mA
IDD2P	57	30	13	mA
IDD2N	420	222	99	mA
IDD3P	195	103	46	mA
IDD3N	767	406	180	mA
IDD4R	1705	875	415	mA
IDD4W	1910	977	466	mA
IDD5	3125	1585	770	mA
IDD6	38	20	9	mA
IDD7	4961	2503	1229	mA

Package Dimensions

Non-ECC, 16 BGA devices, NT1GD64S8HB0FM / NT1GD64S8HB0FN



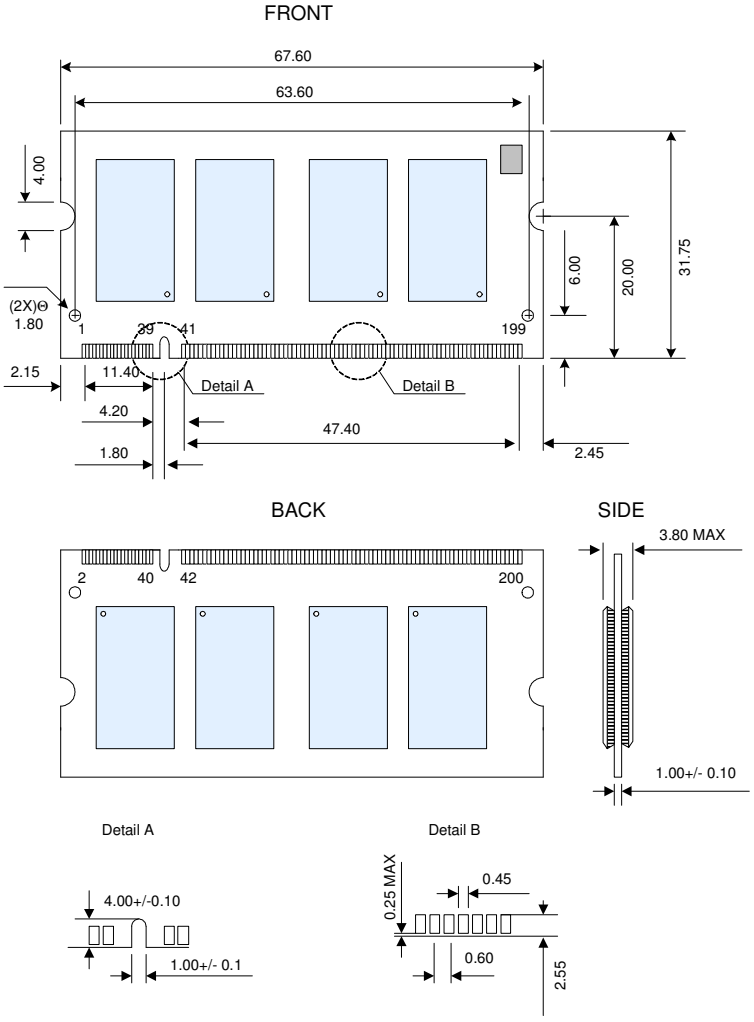
Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Note: Devices are not to scale and are there as references only.

Package Dimensions

Non-ECC, 8 TSOP devices, NT512D64SH8B0GM / NT512D64SH8B0GN



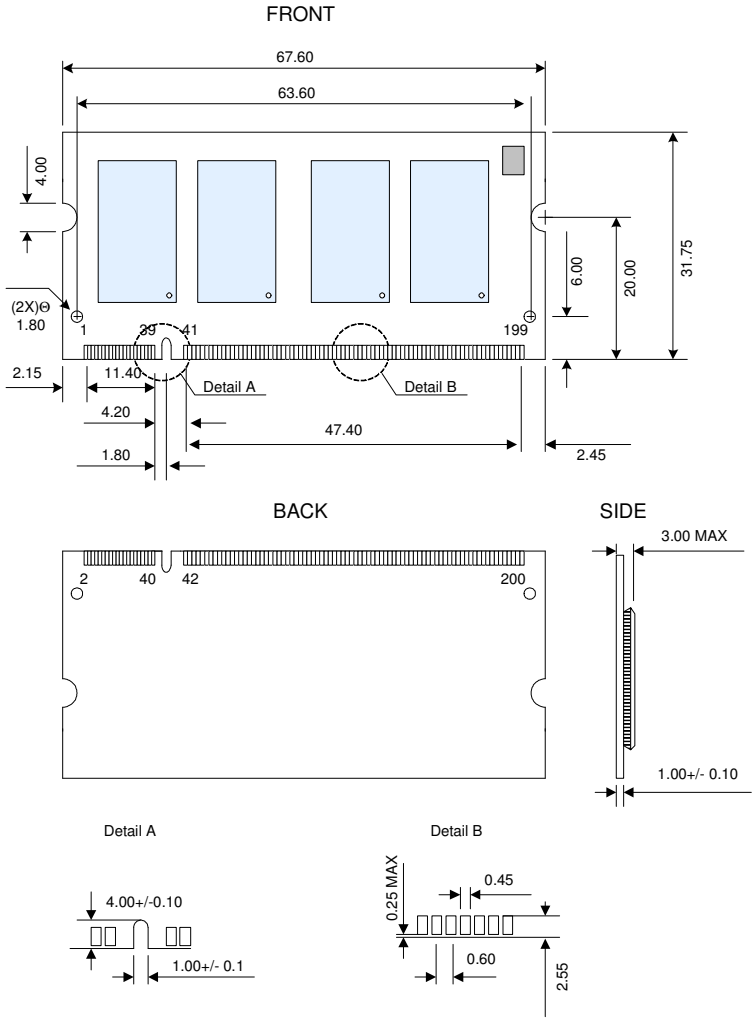
Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Note: Devices are not to scale and are there as references only.

Package Dimensions

Non-ECC, 4 TSOP devices, NT256D64SH40GM / NT256D64SH40GN



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Note: Devices are not to scale and are there as references only.

Revision Log

Rev	Date	Modification
0.1	May 11, 2004	Initial release: 1GB: NT1GD64S8HB0GM – 75B/6K 512MB: NT512D64SH8B0FM – 75B/6K 256MB: NT256D64SH4B0FM – 75B/6K
0.2	Sep 2, 2004	Corrected part numbers as: NT1GD64S8HB0FM NT512D64SH8B0GM NT256D64SH4B0GM
1.0	Nov 9, 2004	Updated IDD 333 and SPD values for all modules Added 'Green' part numbers
1.1	April 28, 2005	Remove 75B speed grade products
1.2	June 3, 2005	Updated Functional Block Diagram.
1.3	Nov 17, 2005	Update Package Dimension

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