

NT1GC64BH8A1PS / NT2GC64B8HA1NS
1GB: 128M x 64 / 2GB: 256M x 64
PC3-8500 / PC3-10600
Unbuffered DDR3 SO-DIMM



Based on DDR3-1066/1333 64Mx16 (1GB) / 128Mx8 (2GB) SDRAM A-Die

Features

•Performance:

Speed Sort	PC3-8500	PC3-10600	Unit
	-BE	-CG	
DIMM CAS Latency	7	9	
fck – Clock Frequency	533	667	MHz
tck – Clock Cycle	1.875	1.5	ns
fDQ – DQ Burst Frequency	1066	1333	Mbps

- 204-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- 1GB: 128Mx64 Unbuffered DDR3 SO-DIMM based on 64Mx16 DDR3 SDRAM A-Die devices.
- 2GB: 256Mx64 Unbuffered DDR3 SO-DIMM based on 128Mx8 DDR3 SDRAM A-Die devices.
- Intended for 533MHz/667MHz applications
- Inputs and outputs are SSTL-15 compatible
- $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge

- Programmable Operation:
 - DIMM \overline{CAS} Latency: 6,7,8,9
 - Burst Type: Sequential or Interleave
 - Burst Length: BC4, BL8
 - Operation: Burst Read and Write
- Two different termination values (Rtt_Nom & Rtt_WR)
- 13/10/2 (row/column/rank) Addressing for 1GB
- 14/10/2 (row/column/rank) Addressing for 2GB
- Extended operating temperature range
- Auto Self-Refresh option
- Serial Presence Detect
- Gold contacts
- 1GB: SDRAMs are in 96-ball BGA Package
- 2GB: SDRAMs are in 78-ball BGA Package
- RoHS compliance + Halogen Free

Description

NT1GC64BH8A1PS-BE and NT2GC64B8HA1NS-BE are unbuffered 204-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as two ranks of 128Mx64 (1GB) and 256Mx64 (2GB) high-speed memory array. Modules use eight 64Mx16 (1GB) 96-ball BGA packaged devices and sixteen 128Mx8 (2GB) 78-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR3 SODIMMs provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 533MHz/667MHz clock speeds and achieves high-speed data transfer rates of 1066Mbps/1333Mbps. Prior to any access operation, the device \overline{CAS} latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A12 (1GB)/A0-A13 (2GB) and I/O inputs BA0–BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Power	Leads	Note
NT1GC64BH8A1PS-BE	DDR3-1066	PC3-8500	533MHz (1.875ns @ CL = 7)	128Mx64	1.5V	Gold	
NT1GC64BH8A1PS-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				
NT2GC64B8HA1NS-BE	DDR3-1066	PC3-8500	533MHz (1.875ns @ CL = 7)	256Mx64			
NT2GC64B8HA1NS-CG	DDR3-1333	PC3-10600	667MHz (1.5ns @ CL = 9)				

Pin Description

Pin Name	Description	Pin Name	Description
CK0, CK1	Clock Inputs, positive line	DQ0-DQ63	Data input/output
$\overline{CK0}$, $\overline{CK1}$	Clock Inputs, negative line	DQS0-DQS7	Data strobes
CKE0, CKE1	Clock Enable	$\overline{DQS0}$ - $\overline{DQS7}$	Data strobes complement
\overline{RAS}	Row Address Strobe	DM0-DM7	Data Masks
\overline{CAS}	Column Address Strobe	\overline{EVENT}	Temperature event pin
\overline{WE}	Write Enable	\overline{RESET}	Reset pin
$\overline{S0}$, $\overline{S1}$	Chip Selects	V_{REFDQ} , V_{REFCA}	Input/Output Reference
A0-A9, A11, A13	Address Inputs	V_{DDSPD}	SPD and Temp sensor power
A10/AP	Address Input/Auto-Precharge	SA0, SA1	Serial Presence Detect Address Inputs
A12/ \overline{BC}	Address Input/Burst Chop	Vtt	Termination voltage
BA0-BA2	SDRAM Bank Address Inputs	V_{SS}	Ground
ODT0, ODT1	Active termination control lines	V_{DD}	Core and I/O power
SCL	Serial Presence Detect Clock Input	NC	No Connect
SDA	Serial Presence Detect Data input/output		

Note: A13 is for 2GB modules only.

DDR3 SDRAM Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REFDQ}	2	V _{SS}	53	DQ19	54	V _{SS}	105	V _{DD}	106	V _{DD}	155	V _{SS}	156	V _{SS}
3	V _{SS}	4	DQ4	55	V _{SS}	56	DQ28	107	A10/AP	108	BA1	157	DQ42	158	DQ46
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{\text{RAS}}$	159	DQ43	160	DQ47
7	DQ1	8	V _{SS}	59	DQ25	60	V _{SS}	111	V _{DD}	112	V _{DD}	161	V _{SS}	162	V _{SS}
9	V _{SS}	10	$\overline{\text{DQS0}}$	61	V _{SS}	62	$\overline{\text{DQS3}}$	113	$\overline{\text{WE}}$	114	$\overline{\text{S0}}$	163	DQ48	164	DQ52
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{\text{CAS}}$	116	ODT0	165	DQ49	166	DQ53
13	V _{SS}	14	V _{SS}	65	V _{SS}	66	V _{SS}	117	V _{DD}	118	V _{DD}	167	V _{SS}	168	V _{SS}
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13/NC	120	ODT1	169	$\overline{\text{DQS6}}$	170	DM6
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{\text{ST}}$	122	NC	171	DQS6	172	V _{SS}
19	V _{SS}	20	V _{SS}	71	V _{SS}	72	V _{SS}	123	V _{DD}	124	V _{DD}	173	V _{SS}	174	DQ54
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	NC	126	V _{REFCA}	175	DQ50	176	DQ55
23	DQ9	24	DQ13	75	V _{DD}	76	V _{DD}	127	V _{SS}	128	V _{SS}	177	DQ51	178	V _{SS}
25	V _{SS}	26	V _{SS}	77	NC	78	NC	129	DQ32	130	DQ36	179	V _{SS}	180	DQ60
27	$\overline{\text{DQS1}}$	28	DM1	79	BA2	80	NC	131	DQ33	132	DQ37	181	DQ56	182	DQ61
29	DQS1	30	$\overline{\text{RESET}}$	81	V _{DD}	82	V _{DD}	133	V _{SS}	134	V _{SS}	183	DQ57	184	V _{SS}
31	V _{SS}	32	V _{SS}	83	A12/BC	84	A11	135	$\overline{\text{DQS4}}$	136	DM4	185	V _{SS}	186	$\overline{\text{DQS7}}$
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V _{SS}	187	DM7	188	DQS7
35	DQ11	36	DQ15	87	V _{DD}	88	V _{DD}	139	V _{SS}	140	DQ38	189	V _{SS}	190	V _{SS}
37	V _{SS}	38	V _{SS}	89	A8	90	A6	141	DQ34	142	DQ39	191	DQ58	192	DQ62
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V _{SS}	193	DQ59	194	DQ63
41	DQ17	42	DQ21	93	V _{DD}	94	V _{DD}	145	V _{SS}	146	DQ44	195	V _{SS}	196	V _{SS}
43	V _{SS}	44	V _{SS}	95	A3	96	A2	147	DQ40	148	DQ45	197	SA0	198	$\overline{\text{EVENT}}$
45	$\overline{\text{DQS2}}$	46	DM2	97	A1	98	A0	149	DQ41	150	V _{SS}	199	V _{DDSPD}	200	SDA
47	DQS2	48	V _{SS}	99	V _{DD}	100	V _{DD}	151	V _{SS}	152	$\overline{\text{DQS5}}$	201	SA1	202	SCL
49	V _{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5	203	V _t	204	V _t
51	DQ18	52	DQ23	103	$\overline{\text{CK0}}$	104	$\overline{\text{CK1}}$								

Note: A13 is for 2GB modules only.

Input/Output Functional Description

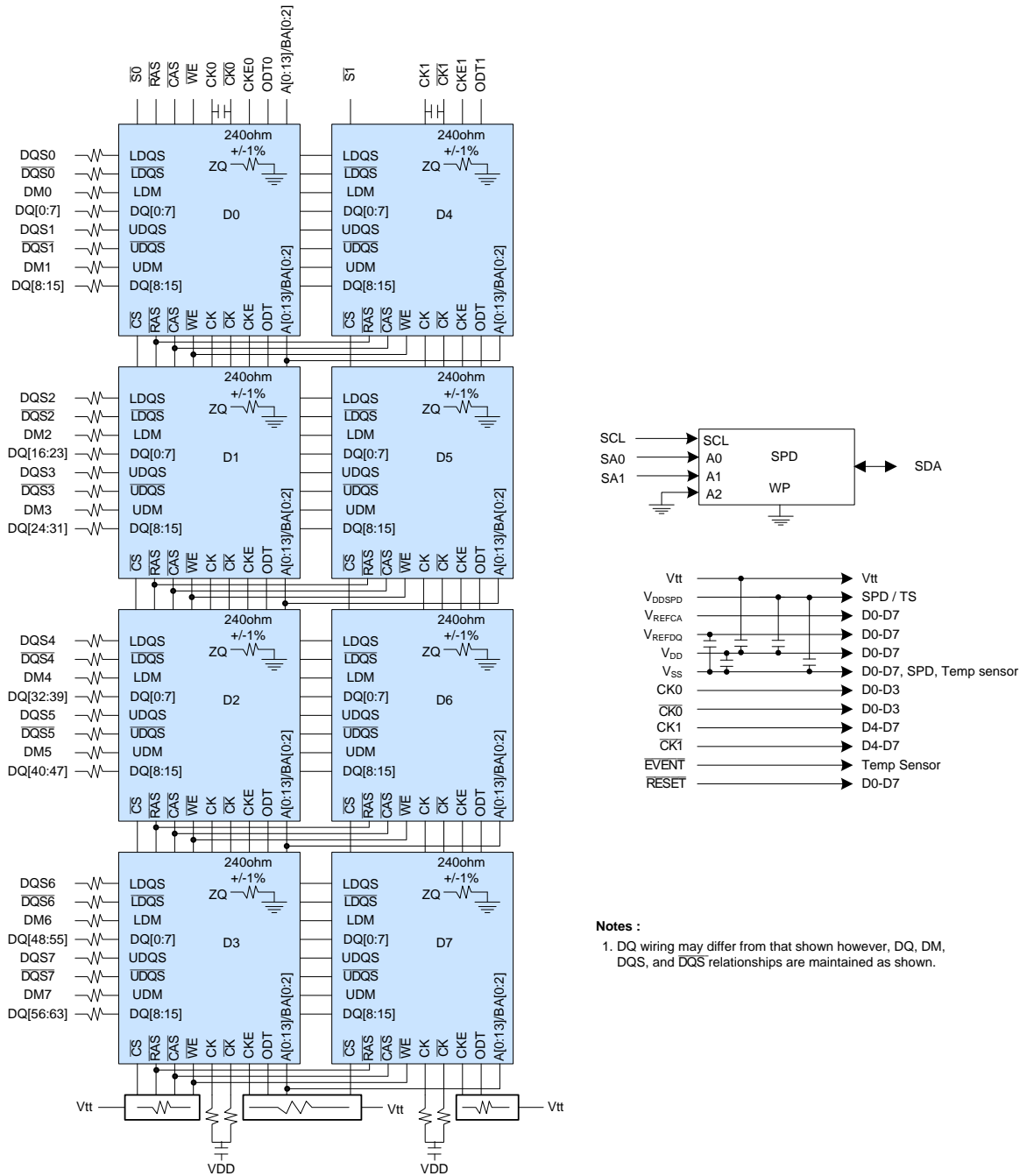
Symbol	Type	Polarity	Function
CK0, CK1 $\overline{\text{CK0}}, \overline{\text{CK1}}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S0}}, \overline{\text{S1}}$	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue, Rank 0 is selected by $\overline{\text{S0}}$; Rank 1 is selected by $\overline{\text{S1}}$.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	Input	Active Low	When sampled at the positive rising edge of CK and falling edge of $\overline{\text{CK}}$, signals $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$ define the operation to be executed by the SDRAM.
ODT0, ODT1	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR3 SDRAM mode register.
DM0 – DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0 – DQS7 $\overline{\text{DQS0}} – \overline{\text{DQS7}}$	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the cross point of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all $\overline{\text{DQS}}$ signals must be tied on the system board to V_{SS} and DDR3 SDRAM mode registers programmed appropriately.
BA0, BA1, BA2	Input	-	Selects which DDR3 SDRAM internal bank of four or eight is activated.
A0 – A9 A10/AP A11 A12/ $\overline{\text{BC}}$ A13	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0 – DQ63	Input	-	Data Input/Output pins.
$V_{DD}, V_{DDSPD}, V_{SS}$	Supply	-	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ}, V_{REFCA}	Supply	-	Reference voltage for SSTL15 inputs
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and temp sensor. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0 – SA2	Input	-	Address pins used to select the Serial Presence Detect and Temp sensor base address.
$\overline{\text{EVENT}}$	Output	-	The $\overline{\text{EVENT}}$ pin is reserved for use to flag critical module temperature.
$\overline{\text{RESET}}$	Input	-	This signal resets the DDR3 SDRAM

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Functional Block Diagram

[1GB – 2 Ranks, 64Mx16 DDR3 SDRAMs]

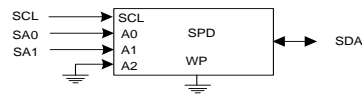
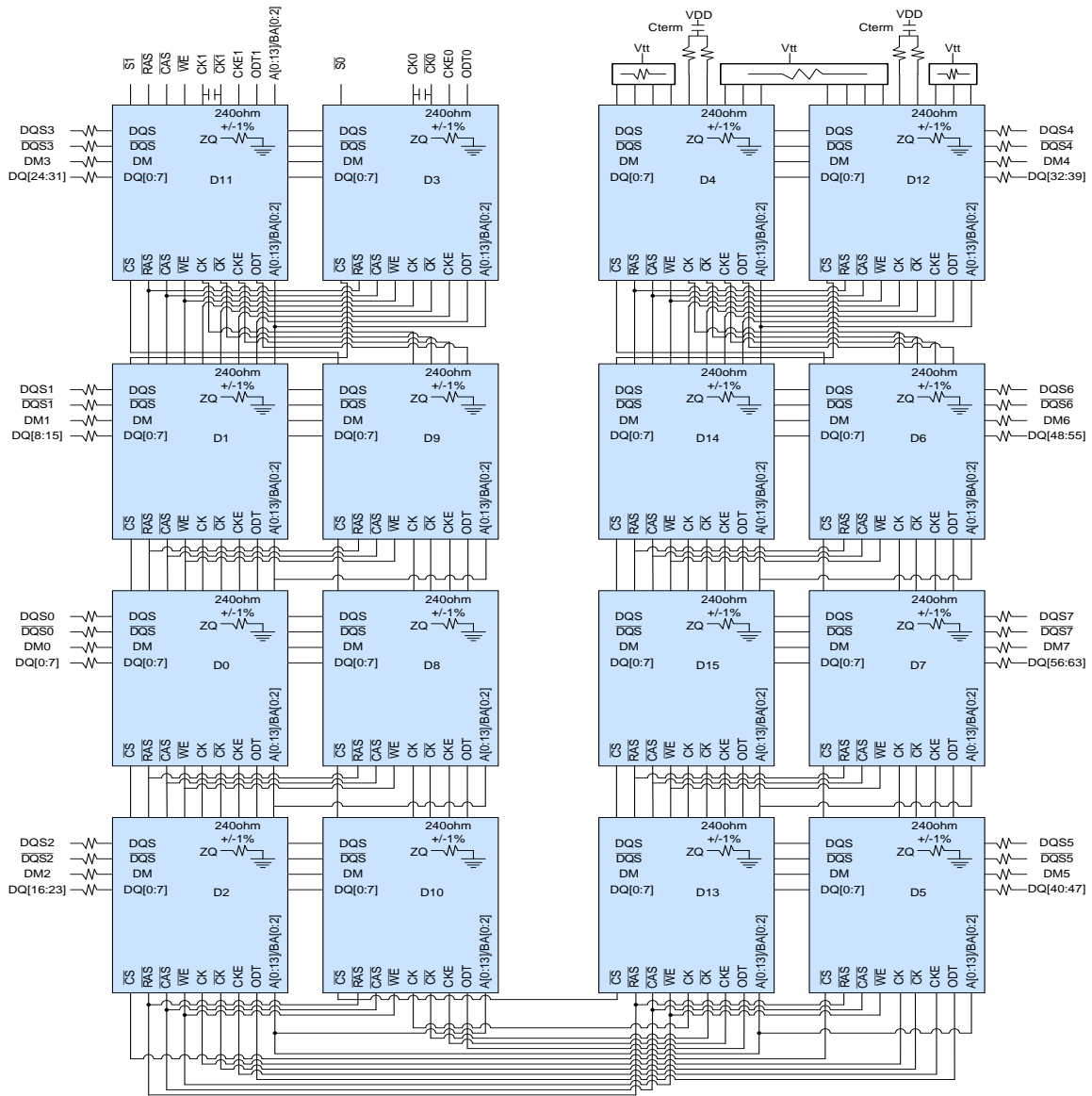


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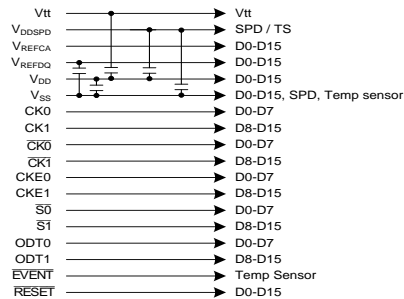


Functional Block Diagram

[2GB – 2 Ranks, 128Mx8 DDR3 SDRAMs]



Notes :
 1. DQ wiring may differ from that shown however, DQ, DM, DQS, and DQS3 relationships are maintained as shown.



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Serial Presence Detect (Part 1 of 2) [1GB – 2 Ranks, 64Mx16 DDR3 SDRAMs]

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-BE	-CG	-BE	-CG
0	CRC range, EEPROM bytes, bytes used	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,	92	92
1	SPD revision	Revision 1.0	Revision 1.0	10	10
2	DRAM device type	DDR3 SDRAM	DDR3 SDRAM	0B	0B
3	Module type (form factor)	SO-DIMM	SO-DIMM	03	03
4	SDRAM Device density and banks	8 banks, 1Gb	8 banks, 1Gb	02	02
5	SDRAM device row and column count	13 rows, 10 columns	13 rows, 10 columns	09	09
6	Reserved	1.5 V	1.5 V	00	00
7	Module ranks and device DQ count	2 ranks, 16 bits	2 ranks, 16 bits	0A	0A
8	ECC tag and module memory Bus width	Non ECC, 64bits	Non ECC, 64bits	03	03
9	Fine timebase dividend/divisor (in ps)	2.5ps	2.5ps	52	52
10	Medium timebase dividend	1ns	1ns	01	01
11	Medium timebase divisor	8ns	8ns	08	08
12	Minimum SDRAM cycle time (tCKmin)	1.875ns	1.5ns	0F	0C
13	Reserved	Undefined	Undefined	00	00
14	CAS latencies supported	6,7,8	6,7,8,9	1C	3C
15	CAS latencies supported	Undefined	Undefined	00	00
16	Minimum CAS latency time (tAmin)	13.125ns	13.125ns	69	69
17	Minimum write recovery time (tWRmin)	15ns	15ns	78	78
18	Minimum CAS-to-CAS delay (tRCDmin)	13.125ns	13.125ns	69	69
19	Minimum Row Active to Row Active delay (tRRDmin)	10ns	7.5ns	50	3C
20	Minimum row Precharge delay (tRPmin)	13.125ns	13.125ns	69	69
21	Upper nibble for tRAS and tRC	1,1	1,1	11	11
22	Minimum Active-to-Precharge delay (tRASmin)	37.5ns	36ns	2C	20
23	Minimum Active-to-Active/Refresh delay (tRCmin)	50.625ns	49.125ns	95	89
24	Minimum refresh recovery delay (tRFCmin) LSB	(Combo bytes 24,25)	(Combo bytes 24,25)	70	70
25	Minimum refresh recovery delay (tRFCmin) MSB	110ns	110ns	03	03
26	Minimum internal Write-to-Read command delay (tWTRmin)	7.5ns	7.5ns	3C	3C
27	Minimum internal Read-to-Precharge command delay (tRTPmin)	7.5ns	7.5ns	3C	3C
28	Minimum four active window delay (tFAWmin) LSB	(Combo byte 28, 29)	(Combo byte 28, 29)	01	01
29	Minimum four active window delay (tFAWmin) MSB	50ns	45ns	90	68
30	SDRAM device output drivers supported	RZQ / 6, RZQ / 7, DLL-Off Mode Support,	RZQ / 6, RZQ / 7, DLL-Off Mode Support,	83	83
31	SDRAM device thermal and refresh options	Extended Temperature Range, ASR, ODTS, PASR,	Extended Temperature Range, ASR, ODTS, PASR,	8D	8D
32	Module Thermal Sensor	Non Thermal Sensor Support	Non Thermal Sensor Support	00	00
33	SDRAM Device Type	Standard Monolithic Device	Standard Monolithic Device	00	00
34-59	Reserved	Undefined	Undefined	--	--
60	Module height (nominal)	29 < height ≤ 30 mm	29 < height ≤ 30 mm	0F	0F
61	Module thickness (Max)	Back: 1 < thickness ≤ 2 mm, Front: 1 < thickness ≤ 2 mm,	Back: 1 < thickness ≤ 2 mm, Front: 1 < thickness ≤ 2 mm,	11	11
62	Raw Card ID reference	Raw Card A	Raw Card A	00	00
63	DRAM address mapping edge connector	Undefined	Undefined	00	00
64-116	Reserved	Undefined	Undefined	--	--
117-118	Module manufacture ID	Nanya Technology	Nanya Technology	830B	830B
119-121	Module manufacturer Information	Undefined	Undefined	--	--
126-127	CRC	Calculated Value	Calculated Value	5309	2DD0

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Serial Presence Detect (Part 2 of 2) [1GB – 2 Ranks, 64Mx16 DDR3 SDRAMs]

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-BE	-CG	-BE	-CG
128-145	Module part number	ASCII values	ASCII values	--	--
146	Module die revision	Undefined	Undefined	00	00
147	Module PCB revision	Undefined	Undefined	00	00
148-149	DRAM device manufacturer ID	Nanya Technology	Nanya Technology	830B	830B
150-175	Manufacturer reserved	Undefined	Undefined	--	--
176-255	Customer reserved	Undefined	Undefined	--	--

Note1:
 NT1GC64BH8A1PS-BE -> 4E543147433634424838413150532D424520
 NT1GC64BH8A1PS-CG -> 4E543147433634424838413150532D434720

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Serial Presence Detect (Part 1 of 2) [2GB – 2 Ranks, 128Mx8 DDR3 SDRAMs]

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-BE	-CG	-BE	-CG
0	CRC range, EEPROM bytes, bytes used	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,	92	92
1	SPD revision	Revision 1.0	Revision 1.0	10	10
2	DRAM device type	DDR3 SDRAM	DDR3 SDRAM	0B	0B
3	Module type (form factor)	SO-DIMM	SO-DIMM	03	03
4	SDRAM Device density and banks	8 banks, 1Gb	8 banks, 1Gb	02	02
5	SDRAM device row and column count	14 rows, 10 columns	14 rows, 10 columns	11	11
6	Reserved	1.5 V	1.5 V	00	00
7	Module ranks and device DQ count	2 ranks, 8 bits	2 ranks, 8 bits	09	09
8	ECC tag and module memory Bus width	Non ECC, 64bits	Non ECC, 64bits	03	03
9	Fine timebase dividend/divisor (in ps)	2.5ps	2.5ps	52	52
10	Medium timebase dividend	1ns	1ns	01	01
11	Medium timebase divisor	8ns	8ns	08	08
12	Minimum SDRAM cycle time (tCKmin)	1.875ns	1.5ns	0F	0C
13	Reserved	Undefined	Undefined	00	00
14	CAS latencies supported	6,7,8	6,7,8,9	1C	3C
15	CAS latencies supported	Undefined	Undefined	00	00
16	Minimum CAS latency time (tAmin)	13.125ns	13.125ns	69	69
17	Minimum write recovery time (tWRmin)	15ns	15ns	78	78
18	Minimum CAS-to-CAS delay (tRCDmin)	13.125ns	13.125ns	69	69
19	Minimum Row Active to Row Active delay (tRRDmin)	7.5ns	6ns	3C	30
20	Minimum row Precharge delay (tRPmin)	13.125ns	13.125ns	69	69
21	Upper nibble for tRAS and tRC	1,1	1,1	11	11
22	Minimum Active-to-Precharge delay (tRASmin)	37.5ns	36ns	2C	20
23	Minimum Active-to-Active/Refresh delay (tRCmin)	50.625ns	49.125ns	95	89
24	Minimum refresh recovery delay (tRFCmin) LSB	(Combo bytes 24,25)	(Combo bytes 24,25)	70	70
25	Minimum refresh recovery delay (tRFCmin) MSB	110ns	110ns	03	03
26	Minimum internal Write-to-Read command delay (tWTRmin)	7.5ns	7.5ns	3C	3C
27	Minimum internal Read-to-Precharge command delay (tRTPmin)	7.5ns	7.5ns	3C	3C
28	Minimum four active window delay (tFAWmin) LSB	(Combo byte 28, 29)	(Combo byte 28, 29)	01	00
29	Minimum four active window delay (tFAWmin) MSB	37.5ns	30ns	2C	F0
30	SDRAM device output drivers supported	RZQ / 6, RZQ / 7, DLL-Off Mode Support,	RZQ / 6, RZQ / 7, DLL-Off Mode Support,	83	83
31	SDRAM device thermal and refresh options	Extended Temperature Range, ASR, ODTS, PASR,	Extended Temperature Range, ASR, ODTS, PASR,	8D	8D
32	Module Thermal Sensor	Non Thermal Sensor Support	Non Thermal Sensor Support	00	00
33	SDRAM Device Type	Standard Monolithic Device	Standard Monolithic Device	00	00
34-59	Reserved	Undefined	Undefined	--	--
60	Module height (nominal)	29 < height ≤ 30 mm	29 < height ≤ 30 mm	0F	0F
61	Module thickness (Max)	Back: 1 < thickness ≤ 2 mm, Front: 1 < thickness ≤ 2 mm,	Back: 1 < thickness ≤ 2 mm, Front: 1 < thickness ≤ 2 mm,	11	11
62	Raw Card ID reference	Raw Card F	Raw Card F	05	05
63	DRAM address mapping edge connector	Undefined	Undefined	00	00
64-116	Reserved	Undefined	Undefined	--	--
117-118	Module manufacture ID	Nanya Technology	Nanya Technology	830B	830B
119-121	Module manufacturer Information	Undefined	Undefined	--	--
126-127	CRC	Calculated Value	Calculated Value	84E6	C64F

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Serial Presence Detect (Part 2 of 2) [2GB – 2 Ranks, 128Mx8 DDR3 SDRAMs]

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hex.)	
		-BE	-CG	-BE	-CG
128-145	Module part number	ASCII values	ASCII values	--	--
146	Module die revision	Undefined	Undefined	00	00
147	Module PCB revision	Undefined	Undefined	00	00
148-149	DRAM device manufacturer ID	Nanya Technology	Nanya Technology	830B	830B
150-175	Manufacturer reserved	Undefined	Undefined	--	--
176-255	Customer reserved	Undefined	Undefined	--	--

Note1:
 NT2GC64B8HA1NS-BE -> 4E54324743363442384841314E532D424520
 NT2GC64B8HA1NS-CG -> 4E54324743363442384841314E532D434720



Environmental Requirements

Symbol	Parameter	Rating	Units
T _{OPR}	Operating Temperature (ambient)	0 to 65	°C
T _{STG}	Storage Temperature	-50 to 100	°C

Note: Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
V _{DD}	Voltage on VDD pins relative to V _{SS}	-0.4 V ~ 1.975 V	V	1, 3
V _{DDQ}	Voltage on VDDQ pins relative to V _{SS}	-0.4 V ~ 1.975 V	V	1, 3
V _{IN} , V _{OUT}	Voltage on I/O pins relative to V _{SS}	-0.4 V ~ 1.975 V	V	1
T _{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREF must be not greater

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T _{OPER}	Normal Operating Temperature Range	0 to 85	°C	1, 2
	Extended Temperature Range	85 to 95	°C	1, 3

Note:

- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JEDEC51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8 μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V _{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V _{DDQ}	Output Supply Voltage	1.425	1.5	1.575	V	1,2

Note:

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Units	Note
		Min.	Max.	Min.	Max.		
VIH.CA(DC)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.CA(DC)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.CA(AC)	AC Input Logic High	Vref + 0.175	Note 2	Vref + 0.175	Note 2	V	1, 2
VIL.CA(AC)	AC Input Logic Low	Note 2	Vref - 0.175	Note 2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC Input Logic High	-	-	Vref + 0.15	Note 2	V	1, 2
VIL.CA(AC150)	AC Input Logic Low	-	-	Note 2	Vref - 0.15	V	1, 2
V _{RefCA(DC)}	Reference Voltage for ADD, CMD Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:

1. For input only pins except RESET#. Vref = VrefCA(DC).
2. See "Overshoot and Undershoot Specifications" in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Units	Note
		Min.	Max.	Min.	Max.		
VIH.DQ(DC)	DC Input Logic High	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.DQ(DC)	DC Input Logic Low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.DQ(AC)	AC Input Logic High	Vref + 0.175	Note 2	Vref + 0.15	Note 2	V	1, 2, 5
VIL.DQ(AC)	AC Input Logic Low	Note 2	Vref - 0.175	Note 2	Vref - 0.15	V	1, 2, 5
V _{RefDQ(DC)}	Reference Voltage for DQ, DM Inputs	0.49 x VDD	0.51 x VDD	0.49 x VDD	0.51 x VDD	V	3, 4

Note:

1. For input only pins except RESET#. Vref = VrefDQ(DC).
2. See "Overshoot and Undershoot Specifications" in the device datasheet.
3. The ac peak noise on VRef may not allow VRef to deviate from VRefDQ(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.
5. Single-ended swing requirement for DQS, DQS# is 350 mV (peak to peak). Differential swing requirement for DQS - DQS# is 700 mV (peak to peak).

Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 1.5\text{V} \pm 0.075\text{V}$ [1GB – 2 Rank, 64Mx16 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-8500 (-BE)	PC3-10600 (-CG)	Unit
IDD0	Operating One Bank Active-Precharge Current	480	546	mA
IDD1	Operating One Bank Active-Read-Precharge Current	546	634	mA
IDD2P0	Precharge Power-Down Current Slow Exit	123	123	mA
IDD2P1	Precharge Power-Down Current Fast Exit	264	290	mA
IDD2Q	Precharge Quiet Standby Current	484	528	mA
IDD2N	Precharge Standby Current	396	440	mA
IDD3P	Active Power-Down Current	290	308	mA
IDD3N	Active Standby Current	484	572	mA
IDD4R	Operating Burst Read Current	1074	1294	mA
IDD4W	Operating Burst Write Current	942	1074	mA
IDD5B	Burst Refresh Current	854	1052	mA
IDD6	Self Refresh Current: Normal Temperature Range	106	106	mA
IDD7	Operating Bank Interleave Read Current	1206	1426	mA

Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 1.5\text{V} \pm 0.075\text{V}$ [2GB – 2 Ranks, 128Mx8 DDR3 SDRAMs]

Symbol	Parameter/Condition	PC3-8500 (-BE)	PC3-10600 (-CG)	Unit
IDD0	Operating One Bank Active-Precharge Current	783	871	mA
IDD1	Operating One Bank Active-Read-Precharge Current	915	1003	mA
IDD2P0	Precharge Power-Down Current Slow Exit	246	246	mA
IDD2P1	Precharge Power-Down Current Fast Exit	528	581	mA
IDD2Q	Precharge Quiet Standby Current	968	1056	mA
IDD2N	Precharge Standby Current	792	880	mA
IDD3P	Active Power-Down Current	581	616	mA
IDD3N	Active Standby Current	968	1144	mA
IDD4R	Operating Burst Read Current	1531	1883	mA
IDD4W	Operating Burst Write Current	1311	1619	mA
IDD5B	Burst Refresh Current	1707	2103	mA
IDD6	Self Refresh Current: Normal Temperature Range	211	211	mA
IDD7	Operating Bank Interleave Read Current	2059	2411	mA

Standard Speed Bins

Speed Bin		DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit	
CL – tRCD - tRP		7-7-7		9-9-9			
Parameter	Symbol	Min	Max	Min	Max		
Internal read command to first data	tAA	13.125	20	13.5	20	ns	
ACT to internal read or write delay time	tRCD	13.125	-	13.5	-	ns	
PRE command period	tRP	13.125	-	13.5	-	ns	
ACT to ACT or REF command period	tRC	50.625	-	49.5	-	ns	
ACT to PRE command period	tRAS	37.5	9*tREFI	36	9*tREFI	ns	
CL = 5	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6, 7	tCK(AVG)	Reserved		Reserved		
CL = 6	CWL=5	tCK(AVG)	2.5	3.3	2.5	3.3	ns
	CWL=6	tCK(AVG)	Reserved		Reserved		
	CWL=7	tCK(AVG)	Reserved		Reserved		
CL = 7	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	Reserved		
	CWL=7	tCK(AVG)	Reserved		Reserved		
CL = 8	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	1.875	<2.5	
	CWL=7	tCK(AVG)	Reserved		1.5	<1.875	
CL = 9	CWL=5, 6	tCK(AVG)	Reserved		Reserved		ns
	CWL=7	tCK(AVG)	Reserved		1.5	<1.875	
CL = 10	CWL=5, 6	tCK(AVG)	Reserved		Reserved		ns
	CWL=7	tCK(AVG)	Reserved		1.5	<1.875	
Supported CL settings		6, 7, 8		6, 8, 9		nCK	
Supported CWL Settings		5, 6		5, 6, 7		nCK	



AC Timing Specifications for DDR3 SDRAM Devices Used on Module

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit
		min	max	min	max	
Clock Timing						
tCK(DLL_OF)	Minimum Clock Cycle Time (DLL off mode)	8	-	8	-	ns
tCK(avg)	Average Clock Period(Refer to "Standard Speed)					
tCH(avg)	Average high pulse width	0.47	0.53	0.47	0.53	tCK(avg)
tCL(avg)	Average low pulse width	0.47	0.53	0.47	0.53	tCK(avg)
tCK(abs)	Absolute Clock Period	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps
tCH(abs)	Absolute high pulse width	0.43	-	0.43	-	tCK(avg)
tCL(abs)	Absolute low pulse width	0.43	-	0.43	-	tCK(avg)
JIT(per)	Clock Period Jitter	-90	90	-80	80	ps
tJIT(per,lck)	Clock Period Jitter during DLL locking period	-80	80	-70	70	ps
tJIT(cc)	Cycle to Clcyle Period Jitter	180		160		ps
tJIT(cc,lck)	Cycle to Cycle Period Jitter	160		140		ps
tERR(2per)	Cumulative error accross 2 cycles	-132	132	-118	118	ps
tERR(3per)	Cumulative error accross 3 cycles	-157	157	-140	140	ps
tERR(4per)	Cumulative error accross 4cycles	-175	175	-155	155	ps
tERR(5per)	Cumulative error accross 5cycles	-188	188	-168	168	ps
tERR(6per)	Cumulative error accross 6 cycles	-200	200	-177	177	ps
tERR(7per)	Cumulative error accross 7 cycles	-209	209	-186	186	ps
tERR(8per)	Cumulative error accross 8 cycles	-217	217	-193	193	ps
tERR(9per)	Cumulative error accross 9 cycles	-224	224	-200	200	ps
tERR(10per)	Cumulative error accross 10 cycles	-231	231	-205	205	ps
tERR(11per)	Cumulative error accross 11 cycles	-237	237	-210	210	ps
tERR(12per)	Cumulative error accross 12 cycles	-242	242	-215	215	ps
tERR(nper)	Cumulative error accross n=13,14,...,49,50 cycles	tERR(npr)min = (1+ 0.68ln(n)) * tJIT(per)min	tERR(npr)max = (1+ 0.68ln(n)) * tJIT(per)max	tERR(npr)min = (1+ 0.68ln(n)) * tJIT(per)min	tERR(npr)max = (1+ 0.68ln(n)) * tJIT(per)max	ps
Data Timing						
tDQSQ	DQS, DQS to DQ skew per group, per access	-	150	-	125	ps
tQH	DQ output hold time from DQS, DQS	0.38	-	0.38	-	tCK(avg)
tLZ(DQ)	DQ low-impedence time from CK / \overline{CK}	-600	300	-500	250	ps
tHZ(DQ)	DQ high-impedence time from CK / \overline{CK}	-	300	-	250	ps
tDS(base)	Data Setup time to DQS, DQS referenced to Vih(ac)/ Vil(ac) levels	25		TBD		ps
tDH(base)	Data Hold time to DQS, DQS referenced to Vih(dc)/ Vil(dc) levels	100		TBD		ps
Data Strobe Timing						
tRPRE	DQS, DQS differential READ Preamble	0.9	Note 19	0.9	Note 19	tCK(avg)
tRPST	DQS, DQS differential READ Postamble	0.3	Note 11	0.3	Note 11	tCK(avg)
tQSH	DQS, DQS differential output high time	0.38	-	0.4	-	tCK(avg)
tQSL	DQS, DQS differential output low time	0.38	-	0.4	-	tCK(avg)
tWPRE	DQS, DQS differential WRITE Preamble	0.9	-	0.9	-	tCK(avg)
tWPST	DQS, DQS differential WRITE Postamble	0.3	-	0.3	-	tCK(avg)
tDQSCK	DQS, DQS rising edge output access time from rising CK, \overline{CK}	-300	300	-255	255	ps
tLZ(DQS)	DQS, DQS low-impedance time (Referenced from	-600	300	-500	250	ps
tHZ(DQS)	DQS, DQS high-impedance time (Referenced from RL+BL/2)	-	300	-	250	ps
tDQSL	DQS, DQS differential input low pulse width	0.4	0.6	0.4	0.6	tCK(avg)
tDQSH	DQS, DQS differential input high pulse width	0.4	0.6	0.4	0.6	tCK(avg)
tDQSS	DQS, DQS rising edge to CK, CK rising edge	-0.25	0.25	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS falling edge setup time to CK, CK rising edge	0.2	-	0.2	-	tCK(avg)
tDSH	DQS, DQS falling edge hold time to CK, \overline{CK} rising	0.2	-	0.2	-	tCK(avg)

NT1GC64BH8A1PS / NT2GC64B8HA1NS
1GB: 128M x 64 / 2GB: 256M x 64
PC3-8500 / PC3-10600
Unbuffered DDR3 SO-DIMM



Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit
		min	max	min	max	
Command and Address Timing						
tDLLK	DLL Locking time	512	-	512	-	nCK
tRTP	Internal READ command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to internal read command	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	
tCCD	CAS to CAS command delay	4	-	4	-	nCK
tDAL	Auto Precharge write recovery + precharge time	WR + roundup (tRP/tCK(avg))		WR + roundup (tRP/tCK(avg))		nCK
tMPRR	End of MPR Read burst to MSR for MPR (exit)	1	-			nCK
tRAS	ACTIVE to PRECHARGE command period Refer to "Standard Speed Bins"					
tRRD	ACTIVE to ACTIVE command period (1k page size -x4/x8)	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period (2k page size -x16)	max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-	
tFAW	Four activate window (1k page size - x4/x8)	37.5	-	30	0	ns
tFAW	Four activate window (2k page size - x16)	50	-	45	0	ns
tIS(base)	Command and Address setup time to CK, CK referenced Vih(ac) / Vil(ac) levels	125	-	65	-	ps
tIH(base)	Command and Address hold time from CK, CK referenced Vih(ac) / Vil(ac) levels	200	-	140	-	ps
tIS(base) AC150	Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	-	-	65+125	-	ps
Calibration Timing						
tZQinit	Power-up and RESET calibration time	512	-	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	256	-	nCK
tZQCS	normal operation Short calibration time	64	-	64	-	nCK
Reset Timing						
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, tRFC(min) +10ns)	-	max(5nCK, tRFC(min) +10ns)	-	
Self Refresh Timings						
tXS	Exit Self Refresh to Commands not requiring a locked DLL	max(5nCK, tRFC(min) +10ns)	-	max(5nCK, tRFC(min) +10ns)	-	
tXSDLL	Exit Self Refresh to Commands requiring a locked	tDLLK(min)	-	tDLLK(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power Down Entry (PDE)	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit(SRX) or Power-Down Exit (PDX) or Reset Exit	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Power Down Timings						
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 7.5ns)	-	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	
tCPDED	Command Pass disable delay	1	-	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9tREFI	tCKE(min)	9tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down	1	-	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL + 4 + 1	-	RL + 4 + 1	-	nCK

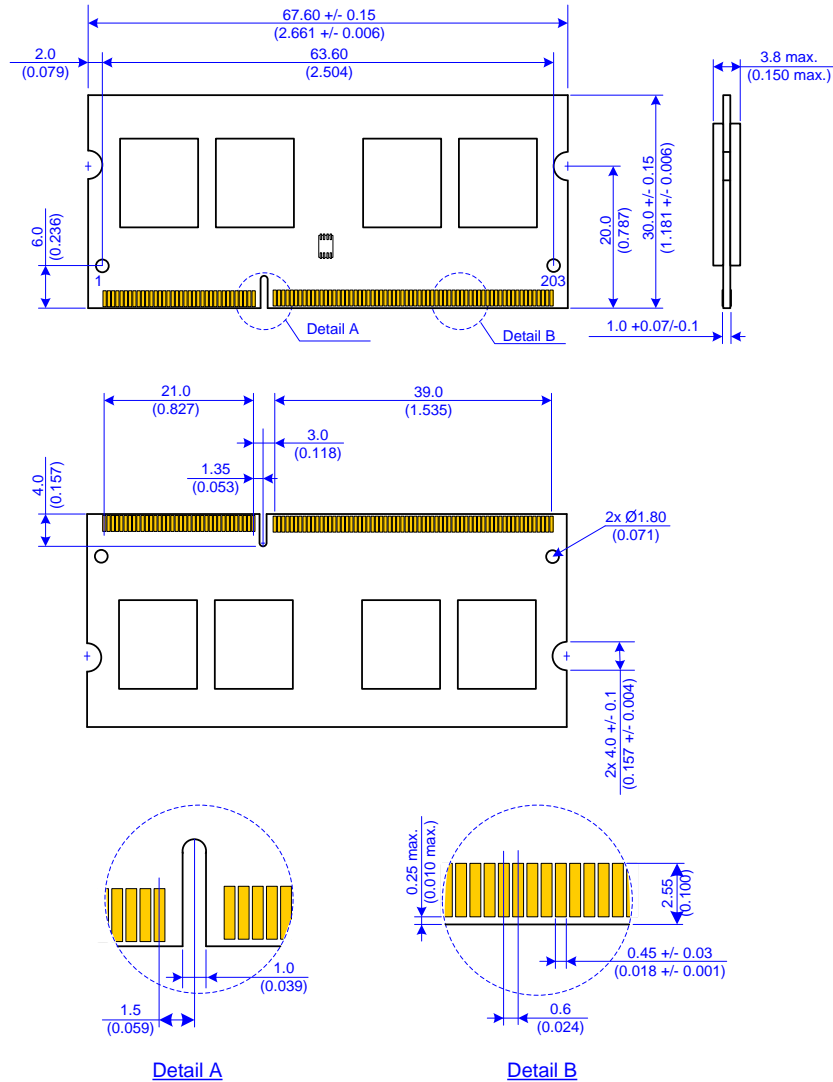
NT1GC64BH8A1PS / NT2GC64B8HA1NS
1GB: 128M x 64 / 2GB: 256M x 64
PC3-8500 / PC3-10600
Unbuffered DDR3 SO-DIMM



Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Unit
		min	max	min	max	
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR/tCK(avg))	-	WL + 4 + (tWR/tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR/tCK(avg))	-	WL + 2 + (tWR/tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	tMOD(min)	-	
ODT Timings						
tODTH4	ODT high time without write command or with write command and BC4	4	-	4	-	nCK
tODTH8	ODT high time without write command oand BL8	6	-	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	1	9	1	9	ns
tAOFPD	Asynchronous RTT turn-off delay (Power Down with DLL frozen)	1	9	1	9	ns
tAON	RTT turn-on	-300	300	-250	250	ps
tAOF	RTT_NOM and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timings						
tWLMRD	First DQS/DQS rising edge after write leveling mode is programmed	40	-	40	-	nCK
tWLDQSEN	DQS/DQS delay after write leveling mode is	25	-	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	245	-	195	-	ps
tWLH	Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	245	-	195	-	ps
tWLO	Write leveling output delay	0	9	0	9	ns
tWLOE	Write leveling output error	0	2	0	2	ns
tRFC	REF command to ACT or REF command time	110		110		ns
tREFI	Average period refresh interval (0°C ≤ tCASE ≤ 85°C)	7.8		7.8		us
tREFI	Average period refresh interval (85°C < tCASE ≤ 95°C)	3.9		3.9		us

Package Dimensions

[1GB – 2 Ranks, 64Mx16 DDR3 SDRAMs]

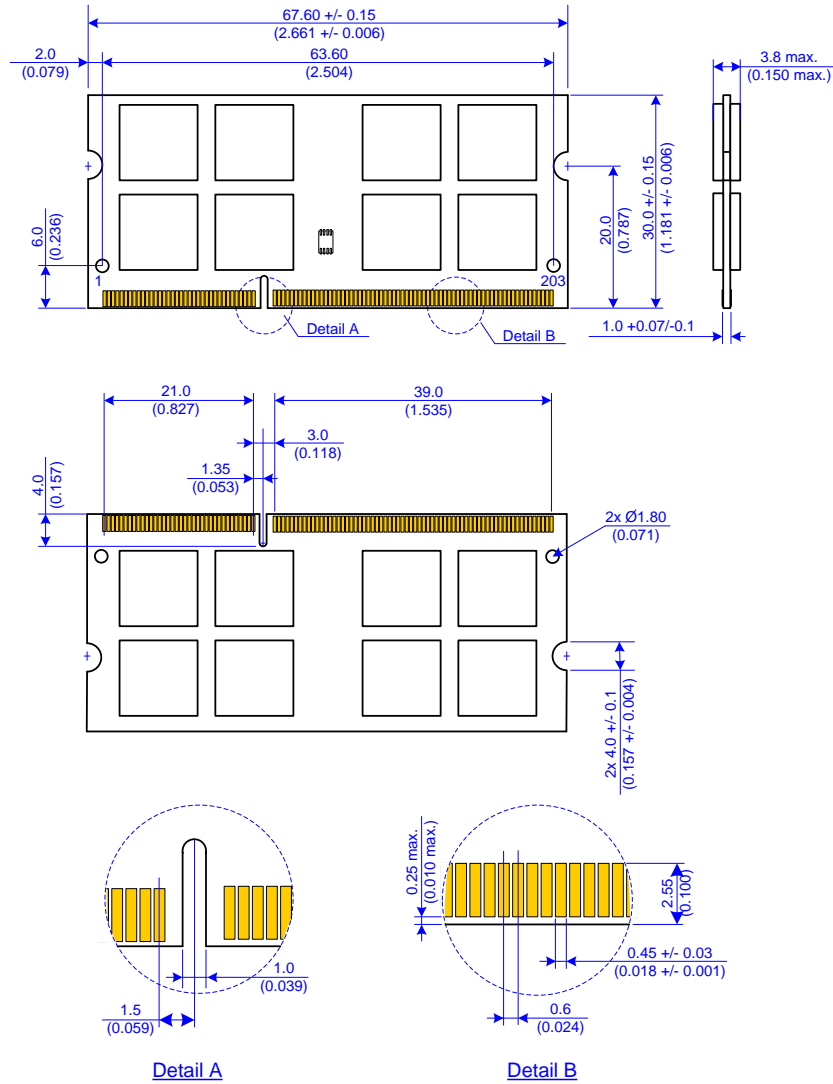


Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

Package Dimensions

[2GB – 2 Ranks, 128Mx8 DDR3 SDRAMs]



Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

NT1GC64BH8A1PS / NT2GC64B8HA1NS
1GB: 128M x 64 / 2GB: 256M x 64
PC3-8500 / PC3-10600
Unbuffered DDR3 SO-DIMM



Revision Log

Rev	Date	Modification
0.1	05/2008	Preliminary Release
1.0	07/2008	Official Release
1.1	09/2008	Revise SPD from Rev0.8 to Rev1.0
1.2	05/2009	Modify IDDX current 1GB & 2GB 1066/1333MHz
1.3	06/2009	IDD and SPD update

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