240pin DDR2 SDRAM Fully Buffered DIMM

Based on 128Mx8 (1GB/2GB), 256Mx4 (4GB), and 512Mx4 (8GB) DDR2 SDRAM

Features

- 1GB 128Mx72 and 2GB 256Mx72 DDR2 Fully Buffered DIMM based on 128Mx8 DDR2 SDRAM (NT5TB128M8DE-3C)
- 4GB 512Mx72 DDR2 Fully Buffered DIMM based on 256Mx4 DDR2 SDRAM (NT5TB256M4DE-3C)
- JEDEC Standard 240-pin Fully Buffered ECC Dual In-Line Memory Module.
- Performance:

Speed Sort		PC2-5300	Unit
		-3C	
DIMM $\overline{CAS}$ Latency		5	
f_{CK}	Clock Frequency	333	MHz
t_{CK}	Clock Cycle	3	ns
f_{DQ}	DQ Burst Frequency	667	Mbps

- Intended for 333MHz applications.
- Inputs and outputs are SSTL-18 compatible.
- **V_{DD} = 1.55V ± 0.075V, V_{DDQ} = 1.55V ± 0.075V**
- Host Interface and AMB component industry standard compliant.
- Support SMBus protocol interface for access to the AMB configuration registers.
- Detects errors on the channel and reports them to the host memory controller.
- Automatic DDR2 DRAM Bus Calibration.
- Full Host Control of the DDR2 DRAMs.
- Over-Temperature Detection and Alert.
- MBIST & IBIST Test Functions.
- Transparent Mode for DRAM Test Support.
- Serial Presence Detect (SPD)
- Gold contacts
- RoHS Compliant products
- SDRAMs in 60-ball BGA Package

Description

Fully Buffered 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Dual In-Line Memory Module (DIMM), organized as an eight bank 128Mx72 (1GB), 256Mx72 (2GB), or 512Mx72 (4GB) high-speed memory array. The module uses nine 128Mx8 (1GB), eighteen 128Mx8 (2GB), or thirty-six 256Mx4 (4GB) DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25” long space-saving footprint.

The DIMM is intended for use in applications operating up to 333MHz clock speeds and achieves high-speed data transfer rates of up to 667 Mbps. Prior to any access operation, the device $\overline{CAS}$ latency and burst type/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1, and BA2 using the mode register set cycle.

Ordering Information

Part Number	AMB	Speed			Organization	Leads	Power
NT1GT72B89D2BD-3C	IDTAMB+	333MHz (3ns @ CL = 5)	DDR2-667	PC2-5300	128Mx72		1.55V
NT2GT72B8PD2BD-3C	IDTAMB+				256Mx72		
NT4GT72B4ND2BD-3C	IDTAMB+				512Mx72		

Note:

FBDIMM module revision will change if AMB, PCB, or Heat spreader version changes.

Ex:

NT512T72U89A0BE-4B

Module Revision

DIMM Connector Pin Description

Pin Name	Pin Description	Note
SCK	System Clock Input, positive line	1
$\overline{SCK}$	System Clock Input, negative line	1
PN0-PN13	Primary Northbound Data, positive lines	
$\overline{PN0}$-$\overline{PN13}$	Primary Northbound Data, negative lines	
PS0-PS9	Primary Southbound Data, positive lines	
$\overline{PS0}$-$\overline{PS9}$	Primary Southbound Data, negative lines	
SN0-SN13	Secondary Northbound Data, positive lines	
$\overline{SN0}$-$\overline{SN13}$	Secondary Northbound Data, negative lines	
SS0-SS9	Secondary Southbound Data, positive lines	
$\overline{SS0}$-$\overline{SS9}$	Secondary Southbound Data, negative lines	
SCL	Serial Presence Detect (SPD) Clock Input	
SDA	SPD Data Input / Output	
S0-S1	SPD Address Inputs, also used to select the DIMM number in the AMB	
VID0-VID1	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID0 is V_{DD} value: OPEN=1.8V, GND=1.5V; VID1 is V_{CC} value: OPEN=1.5V, GND=1.2V	
$\overline{RESET}$	AMB reset signal	
RFU	Reserved for Future Use	2
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5V)	
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8V)	
V_{TT}	DRAM Address/Command/Clock Termination Power (V_{DD}/2)	
V_{DDSPD}	SPD Power (3.3V)	
V_{SS}	Ground	
DNU/M_TEST	It provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.	1

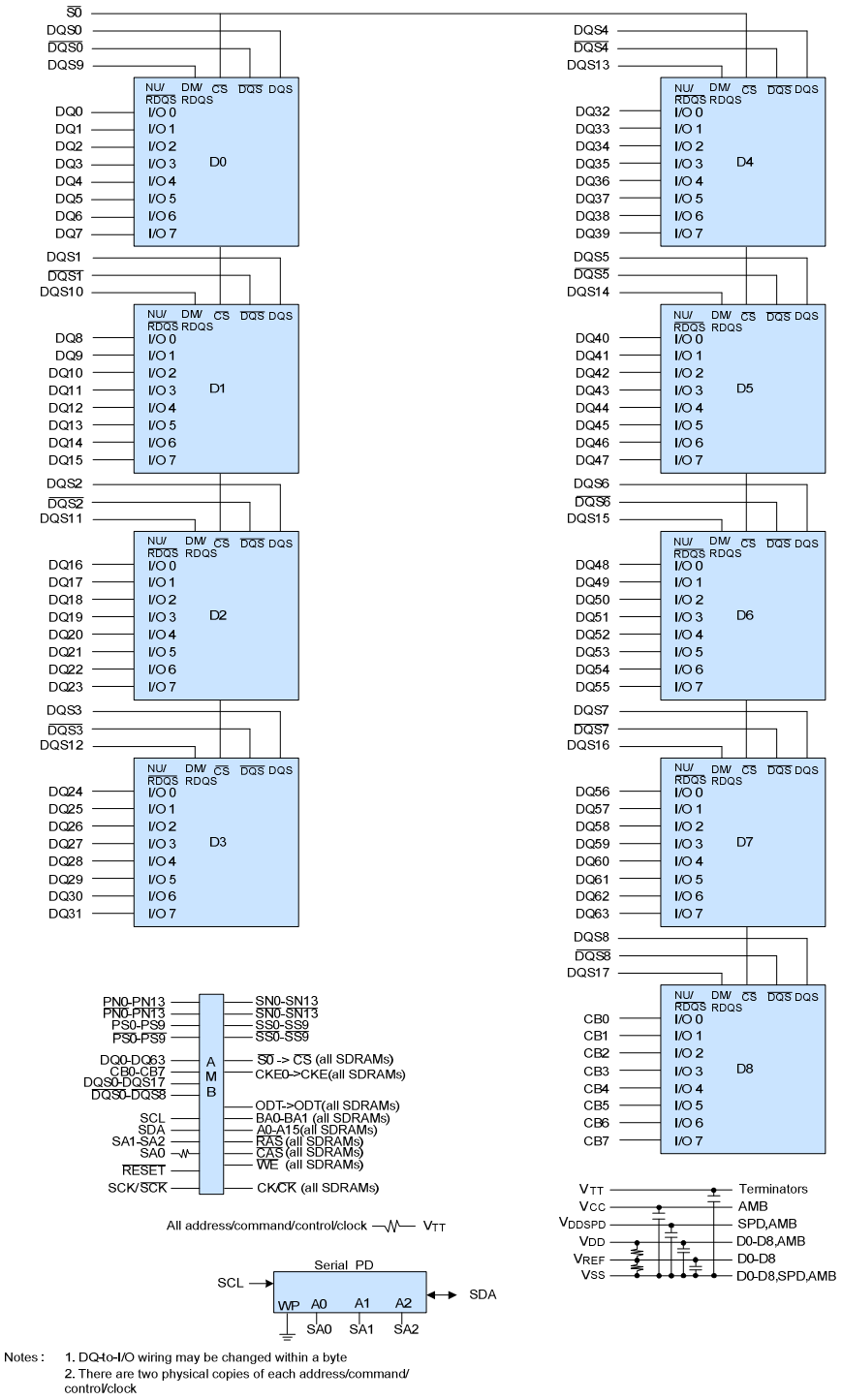
Note:
1. System Clock Signals SCK and SCK switch at one half the DRAM CK/$\overline{CK}$ frequency
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

DDR2 240-pin FBDIMM Pinout

Pin	Front Side	Pin	Front Side	Pin	Front Side	Pin	Back Side	Pin	Back Side	Pin	Back Side
1	V_{DD}	42	V_{SS}	82	PS4	121	V_{DD}	162	V_{SS}	202	SS4
2	V_{DD}	43	V_{SS}	83	$\overline{PS4}$	122	V_{DD}	163	V_{SS}	203	$\overline{SS4}$
3	V_{DD}	44	RFU*	84	V_{SS}	123	V_{DD}	164	RFU*	204	V_{SS}
4	V_{SS}	45	RFU*	85	V_{SS}	124	V_{SS}	165	RFU*	205	V_{SS}
5	V_{DD}	46	V_{SS}	86	RFU*	125	V_{DD}	166	V_{SS}	206	RFU*
6	V_{DD}	47	V_{SS}	87	RFU*	126	V_{DD}	167	V_{SS}	207	RFU*
7	V_{DD}	48	PN12	88	V_{SS}	127	V_{DD}	168	SN12	208	V_{SS}
8	V_{SS}	49	$\overline{PN12}$	89	V_{SS}	128	V_{SS}	169	$\overline{SN12}$	209	V_{SS}
9	V_{CC}	50	V_{SS}	90	PS9	129	V_{CC}	170	V_{SS}	210	SS9
10	V_{CC}	51	PN6	91	$\overline{PS9}$	130	V_{CC}	171	SN6	211	$\overline{SS9}$
11	V_{SS}	52	$\overline{PN6}$	92	V_{SS}	131	V_{SS}	172	$\overline{SN6}$	212	V_{SS}
12	V_{CC}	53	V_{SS}	93	PS5	132	V_{CC}	173	V_{SS}	213	SS5
13	V_{CC}	54	PN7	94	$\overline{PS5}$	133	V_{CC}	174	SN7	214	$\overline{SS5}$
14	V_{SS}	55	$\overline{PN7}$	95	V_{SS}	134	V_{SS}	175	$\overline{SN7}$	215	V_{SS}
15	V_{TT}	56	V_{SS}	96	PS6	135	V_{TT}	176	V_{SS}	216	SS6
16	VID1	57	PN8	97	$\overline{PS6}$	136	VID0	177	SN8	217	$\overline{SS6}$
17	$\overline{RESET}$	58	$\overline{PN8}$	98	V_{SS}	137	DNU/M_TEST	178	$\overline{SN8}$	218	V_{SS}
18	V_{SS}	59	V_{SS}	99	PS7	138	V_{SS}	179	V_{SS}	219	SS7
19	RFU**	60	PN9	100	$\overline{PS7}$	139	RFU**	180	SN9	220	$\overline{SS7}$
20	RFU**	61	$\overline{PN9}$	101	V_{SS}	140	RFU**	181	$\overline{SN9}$	221	V_{SS}
21	V_{SS}	62	V_{SS}	102	PS8	141	V_{SS}	182	V_{SS}	222	SS8
22	PN0	63	PN10	103	$\overline{PS8}$	142	SN0	183	SN10	223	$\overline{SS8}$
23	$\overline{PN0}$	64	$\overline{PN10}$	104	V_{SS}	143	$\overline{SN0}$	184	$\overline{SN10}$	224	V_{SS}
24	V_{SS}	65	V_{SS}	105	RFU**	144	V_{SS}	185	V_{SS}	225	RFU**
25	PN1	66	PN11	106	RFU**	145	SN1	186	SN11	226	RFU**
26	$\overline{PN1}$	67	$\overline{PN11}$	107	V_{SS}	146	$\overline{SN1}$	187	$\overline{SN11}$	227	V_{SS}
27	V_{SS}	68	V_{SS}	108	V_{DD}	147	V_{SS}	188	V_{SS}	228	SCK
28	PN2	KEY		109	V_{DD}	148	SN2	KEY		229	$\overline{SCK}$
29	$\overline{PN2}$	69	V_{SS}	110	V_{SS}	149	$\overline{SN2}$	189	V_{SS}	230	V_{SS}
30	V_{SS}	70	PS0	111	V_{DD}	150	V_{SS}	190	SS0	231	V_{DD}
31	PN3	71	$\overline{PS0}$	112	V_{DD}	151	SN3	191	$\overline{SS0}$	232	V_{DD}
32	$\overline{PN3}$	72	V_{SS}	113	V_{DD}	152	$\overline{SN3}$	192	V_{SS}	233	V_{DD}
33	V_{SS}	73	PS1	114	V_{SS}	153	V_{SS}	193	SS1	234	V_{SS}
34	PN4	74	$\overline{PS1}$	115	V_{DD}	154	SN4	194	$\overline{SS1}$	235	V_{DD}
35	$\overline{PN4}$	75	V_{SS}	116	V_{DD}	155	$\overline{SN4}$	195	V_{SS}	236	V_{DD}
36	V_{SS}	76	PS2	117	V_{TT}	156	V_{SS}	196	SS2	237	V_{TT}
37	PN5	77	$\overline{PS2}$	118	SA2	157	SN5	197	$\overline{SS2}$	238	V_{DDSPD}
38	$\overline{PN5}$	78	V_{SS}	119	SDA	158	$\overline{SN5}$	198	V_{SS}	239	SA0
39	V_{SS}	79	PS3	120	SCL	159	V_{SS}	199	SS3	240	SA1
40	PN13	80	$\overline{PS3}$			160	SN13	200	$\overline{SS3}$		
41	$\overline{PN13}$	81	V_{SS}			161	$\overline{SN13}$	201	V_{SS}		

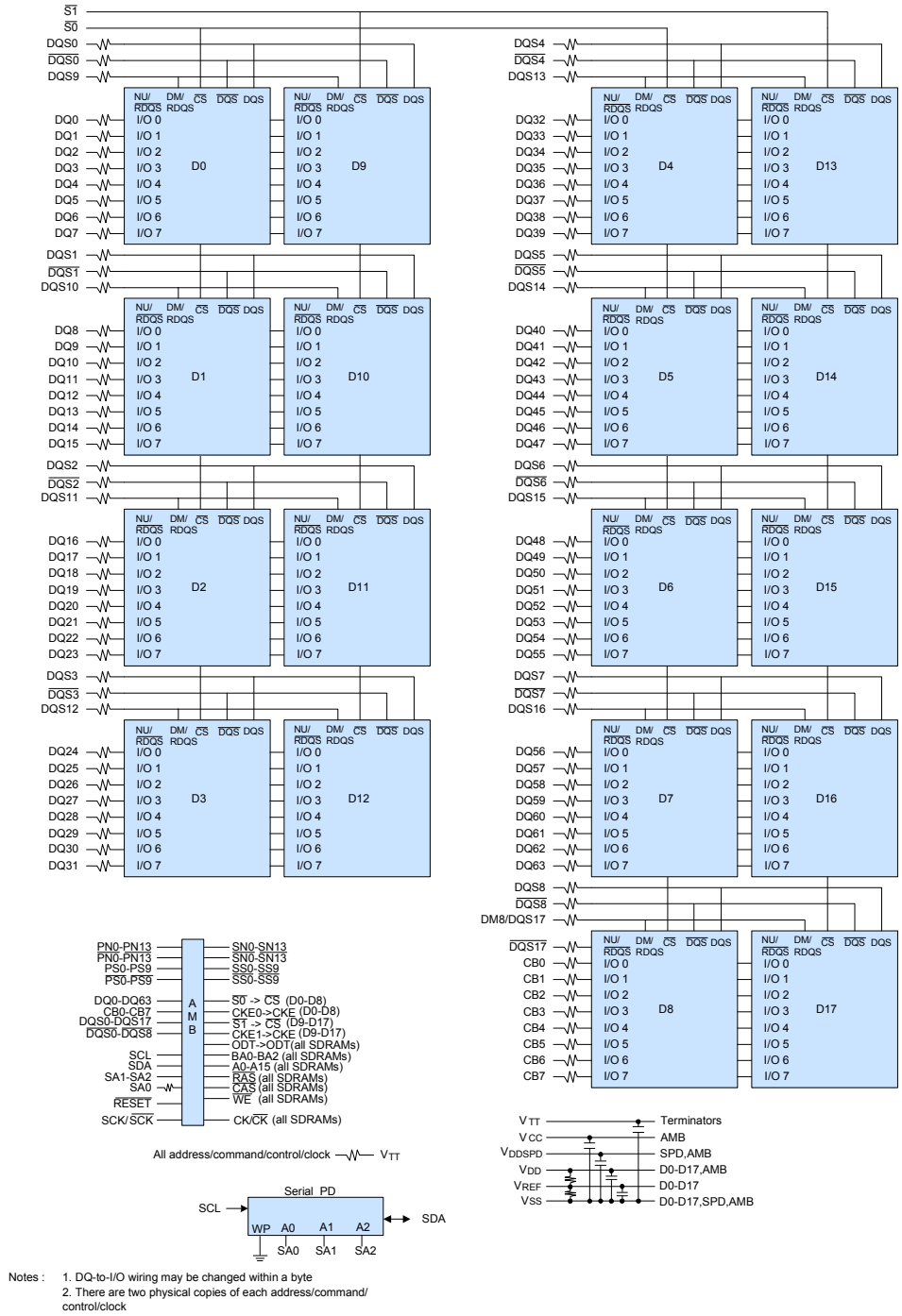
Note:
RFU = Reserved Future Use
* These pin positions are reserved for forwarded clocks to be used in future module implementation
** These pin positions are reserved for future architecture flexibility
The following signals are CRC bits and thus appear out of the normal sequence: PN12/$\overline{PN12}$, SN12/$\overline{SN12}$, PN13/$\overline{PN13}$, SN13/$\overline{SN13}$, PS9/$\overline{PS9}$, SS9/$\overline{SS9}$

Functional Block Diagram (1GB, 1Rank, 128Mx8 DDR2 SDRAMs)



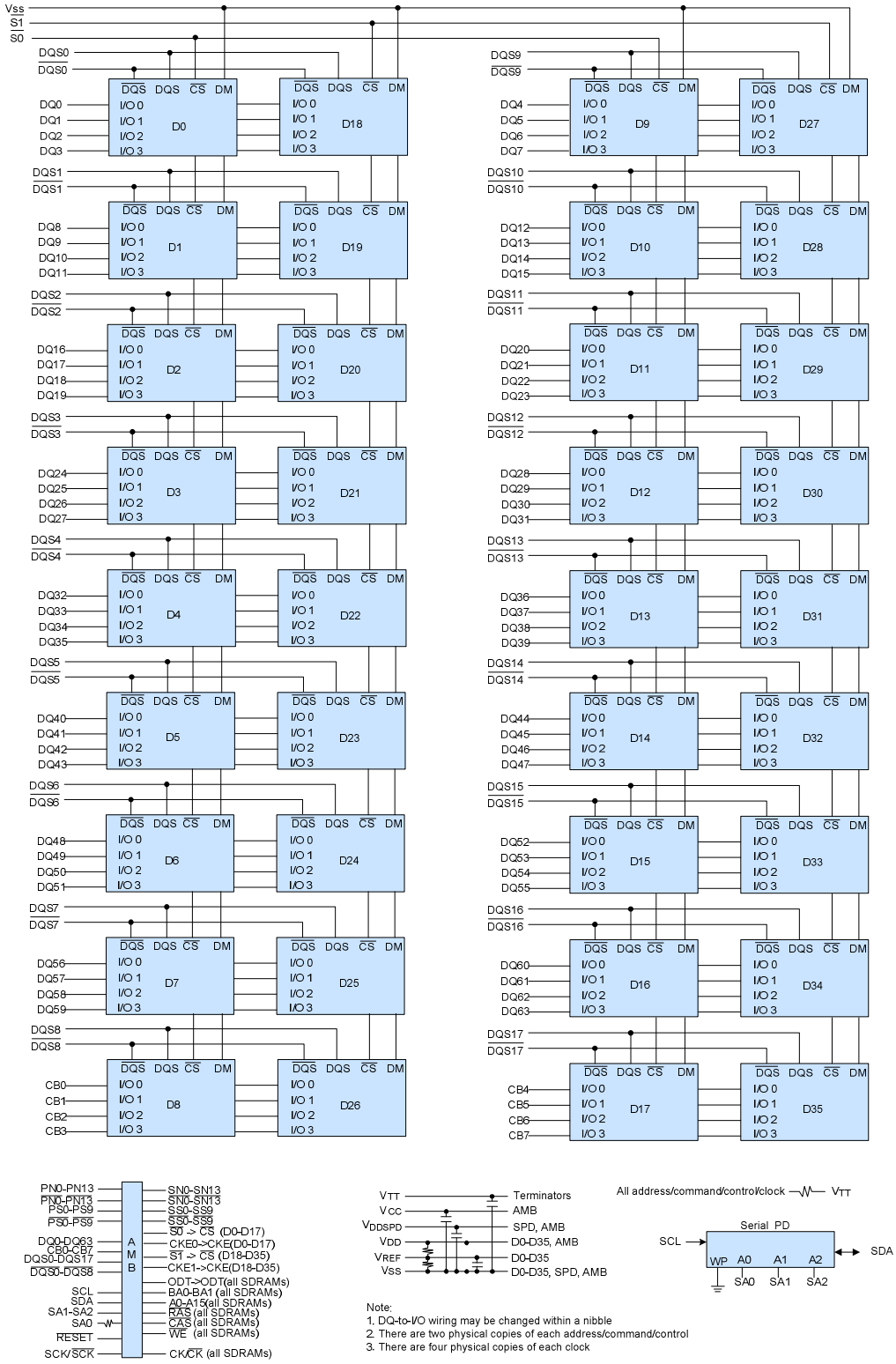
Notes : 1. DQ-to-I/O wiring may be changed within a byte
2. There are two physical copies of each address/command/control/clock

Functional Block Diagram (2GB, 2Ranks, 128Mx8 DDR2 SDRAMs)



Notes : 1. DQ-to-I/O wiring may be changed within a byte
2. There are two physical copies of each address/command/control/clock

Functional Block Diagram (4GB, 2Ranks, 256Mx4 DDR2 SDRAMs)



Note:
1. DQ-to-I/O wiring may be changed within a nibble
2. There are two physical copies of each address/command/control
3. There are four physical copies of each clock

Absolute Maximum DC Ratings

Symbol	Min	Typical	Max	Units	Notes
DRAM V_{DD} / V_{DDQ}, AMB V_{DDQ}	1.475	1.55	1.625	V	
AMB V_{CC} / V_{CCFBD}	1.46	1.5	1.54	V	1
DRAM Interface V_{TT}	0.48 x V_{DD}	0.5 x V_{DD}	0.52 x V_{DD}	V	
V_{DDSPD}	3.0	3.3	3.6	V	
Note 1: Estimate					

Operating Temperature Range

Symbol	Parameter	Min	Max	Units	Notes
Tcase	DRAM Component Operating Temperature (Ambient)	0	+95	℃	1
Tcase	AMB Component Operating Temperature (Ambient)	0	+110	℃	
Note 1: Within the DRAM Temperature range all DRAM will be support.					

Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
VDD, VDDQ	Supply Voltage, I/O Supply Voltage	1.475	1.625	V	1
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.125	VDDQ	V	1
VIL (DC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.125	V	1
VIH (AC)	Input High (Logic1) Voltage	VREF + 0.2	VDDQ	V	
VIL (AC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.2	V	
VID (AC)	AC differential input voltage	0.5	VDDQ + 0.6	V	
VIX (AC)	AC Differential cross point input Voltage	0.5* VDDQ - 0.175	0.5* VDDQ + 0.175	V	
VOX (AC)	AC Differential cross point output Voltage	0.5* VDDQ - 0.125	0.5* VDDQ + 0.125	V	
VSS, VSSQ	Supply Voltage, I/O Supply Voltage	0	0	V	
VREF	I/O Reference Voltage	0.49 x VDDQ	0.51 x VDDQ	V	1, 2
VTT	I/O Termination Voltage (System)	VREF - 0.04	VREF + 0.04	V	1, 3

Note:
1. Inputs are not recognized as valid until VREF stabilizes.
2. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
3. VTT is not applied directly to the DIMM. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.

Serial Presence Detect -- Part 1 of 2

Byte	Description	Serial PD Data Entry (Hexadecimal)			Note
		1GB	2GB	4GB	
0	Number of Serial PD Bytes in CRC	92	92	92	
1	SPD Revision	11	11	11	
2	Key Byte / DRAM Device Type	09	09	09	
3	Voltage Levels of this Assembly	42	42	42	
4	SDRAM Addressing	45	45	49	
5	Module Physical Attributes	24	24	24	
6	Modules Type	07	07	07	
7	Module Organization	09	11	10	
8	Fine Timebase Dividend and Divisor	52	52	52	
9	Medium Timebase Dividend	01	01	01	
10	Medium Timebase Divisor	04	04	04	
11	SDRAM Minimum Cycle Time (tCKmin)	0C	0C	0C	
12	SDRAM Maximum Cycle Time (tCKmax)	20	20	20	
13	SDRAM $\overline{CAS}$ Latencies Supported	43	43	43	
14	SDRAM Minimum CAS Latency Time (tAA)	3C	3C	3C	
15	SDRAM Write Recovery Times Supported	42	42	42	
16	SDRAM Write Recovery Time (tWR)	3C	3C	3C	
17	SDRAM Write Latencies Supported	42	42	42	
18	SDRAM Additive Latencies Supported	60	60	60	
19	SDRAM Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (tRCD)	3C	3C	3C	
20	SDRAM Minimum Row Active to Row Active Delay (tRRD)	1E	1E	1E	
21	SDRAM Minimum Row Precharge Time (tRP)	3C	3C	3C	
22	SDRAM Upper Nibbles for tRAS and tRC	00	00	00	
23	SDRAM Minimum Active to Precharge Time (tRAS)	B4	B4	B4	
24	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC)	F0	F0	F0	
25~26	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	FE01	FE01	FE01	
27	SDRAM Internal Write to Read Command Delay (tWTR)	1E	1E	1E	
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	1E	1E	1E	
29	SDRAM Burst Lengths Supported	03	03	03	
30	SDRAM Terminations Supported	07	07	07	
31	SDRAM Drivers Supported	01	01	01	
32	SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication	C2	C2	C2	
33	Tcasemax	00	00	00	
34	Thermal resistance of SDRAM device package from top (case0 to ambient (Psi T-A SDRAM)	00	00	00	

Serial Presence Detect -- Part 2 of 2

Byte	Description	Serial PD Data Entry (Hexadecimal)			Note
		1GB	2GB	4GB	
35-41	Delta Temperature	--	--	--	
42-80	Reserved	--	--	--	
81~82	FB-DIMM Channel Protocols Supported	0200	0200	0200	
83	Additional Back to Back Access Turnaround Time	10	10	10	
84	AMB Read Access Time for DDR2-800	36	36	36	
85	AMB Read Access Time for DDR2-667	34	34	34	
86	AMB Read Access Time for DDR2-533	32	32	32	
87	Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition.	2A	2A	2A	
88	AMB DT Idle_0	56	56	5E	
89	AMB DT Idle_1	6B	6B	73	
90	AMB DT Idle_2	5C	5C	5C	
91	AMB DT Active_1	91	91	9B	
92	AMB DT Active _2	76	76	80	
93	AMB DT L0s	00	00	00	
94~114	Reserved	--	--	--	
115~116	AMB Manufacturer ID Code	7FB3	7FB3	7FB3	
117-118	Module ID: Module Manufacture's JEDEC ID Code	830B	830B	830B	
119-125	Reserved for Module ID	--	--	--	
126-127	Cyclical Redundancy Code	--	--	--	
128-145	Module Part Number	--	--	--	
146-147	Module Revision Code	--	--	--	
148-149	SDRAM Manufacture's JEDEC ID Code	830B	830B	830B	
150-255	Reserved	--	--	--	

Environmental Requirements

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Operating temperature	-		1
H_{OPR}	Operating humidity (relative)	10 to 90	%	2
T_{STG}	Storage temperature	-50 to +100	ºC	2
H_{STG}	Storage humidity (without condensation)	5 to 95	%	2
P_{BAR}	Barometric pressure (operating & Storage)	105 to 69	K pascal	2

Note:
1. The designer must meet the case temperature specifications for individual module components.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating, Standby, and Refresh Currents

Definition table

Symbol	Parameter/Condition
Idd_Idle_0 **Icc_Idle_0**	**Idle Current, single or last DIMM.** L0 state, idle (0BW). Primary channel enabled; Secondary Channel disabled. CKE high. Command and address line stable. DRAM clock active.
Idd_Idle_1 **Icc_Idle_1**	**Idle Current, first DIMM.** L0 stage, idle (0BW). Primary and Secondary channels enabled. CKE high. Command and address line stable. DRAM clock active.
Idd_Idle_2 **Icc_Idle_2**	**Idle Current, DRAM power down.** L0 stage, idle (0BW). Primary and Secondary channels enabled CKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low.
Idd_Active_1 **Icc_Active_1** **(Write)**	**Active Power.** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.
Idd_Active_1 **Icc_Active_1** **(Read)**	**Active Power.** L0 state. 50% DRAM BW to downstream DIMM, 100% read. Primary and Secondary channels enabled. DRAM clock active, CKE high.
Idd_Active_2 **Icc_Active_2**	**Active Power, data pass through.** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. CKE high. Command and address lines stable. DRAM clock active.
Idd_Training **Icc_Training**	Primary and Secondary channels enabled. 100% toggle on all channel lanes. DRAMs idle. 0BW. CKE high, Command and address line stable. DRAM clock active.

Part Number	Idle_0		Idle_1		Idle_2		Active_1 (W)		Active_1 (R)		Active_2		Training		Unit
	Idd	Icc	Idd	Icc	Idd	Icc	Idd	Icc	Idd	Icc	Idd	Icc	Idd	Icc	
NT1GT72B89D2BD-3C	0.825	1.87	0.825	2.31	0.847	2.31	0.836	2.31	0.825	2.299	0.836	2.31	0.825	2.266	A
NT2GT72B8PD2BD-3C	1.155	1.925	1.155	2.42	1.21	2.431	1.21	2.442	1.21	2.431	1.155	2.431	1.155	2.398	A
NT4GT72B4ND2BD-3C	1.969	1.98	1.969	2.475	2.046	2.486	2.035	2.486	2.057	2.497	1.958	2.497	1.958	2.464	A

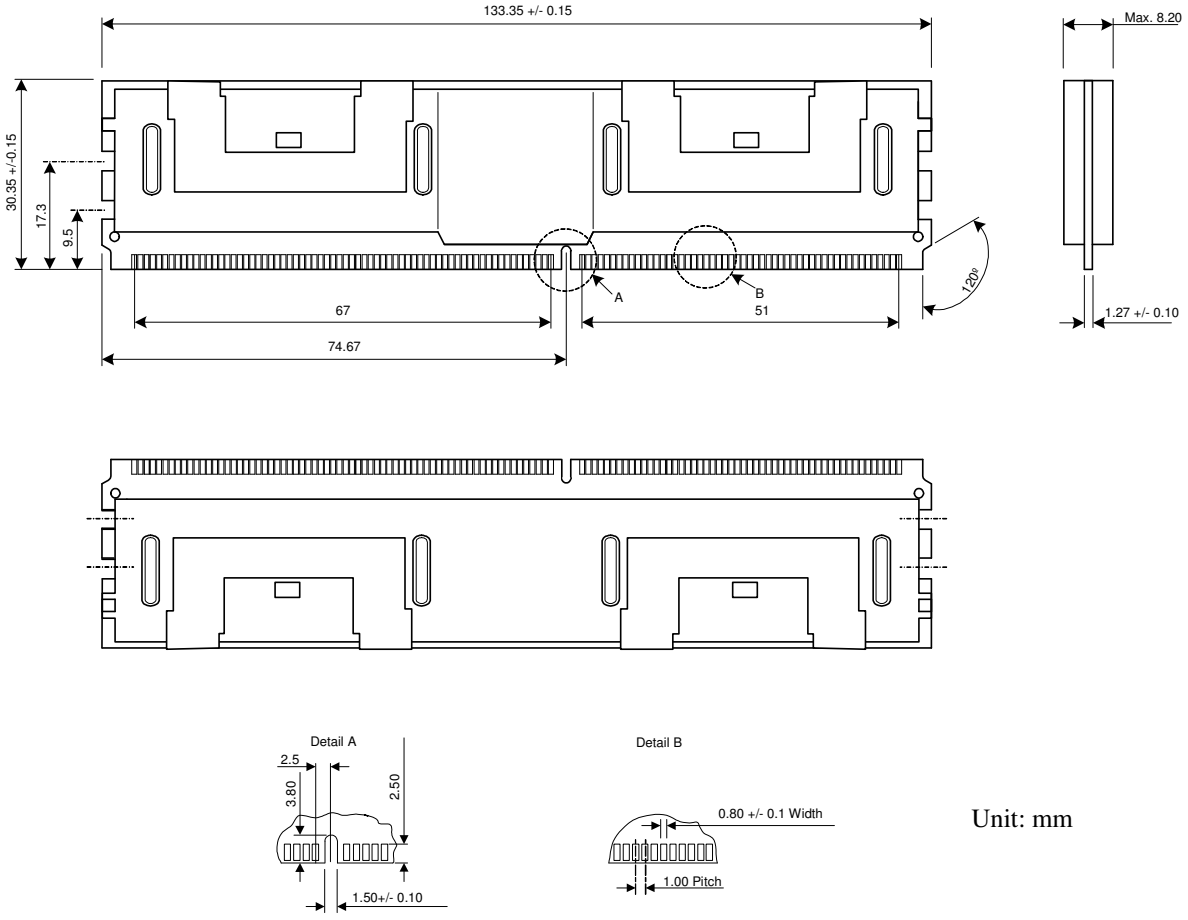
AC Timing Specifications for DDR2 SDRAM Devices Used on Module (Part 1 of 2)

Symbol	Parameter	-3C		Unit	Notes
		Min.	Max.		
t_{AC}	DQ output access time from CK/$\overline{CK}$	-0.45	+0.45	ns	
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$	-0.4	+0.4	ns	
t_{CH}	CK high-level width	0.48	0.52	t_{CK}	
t_{CL}	CK low-level width	0.48	0.52	t_{CK}	
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	Min (t_{CH}, t_{CL})	-	t_{CK}	
t_{CK}	Clock Cycle Time	3	8	ns	
t_{DH}	DQ and DM input hold time	175	-	ps	
t_{DS}	DQ and DM input setup time	100	-	ps	
t_{IPW}	Input pulse width	0.6	-	t_{CK}	
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	t_{CK}	
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$	-	$t_{AC\ max}$	ns	
$t_{LZ(DQ)}$	Data-out low-impedance time from CK/$\overline{CK}$	$2t_{AC\ min}$	$t_{AC\ max}$	ns	
$t_{LZ(DQS)}$	DQS/$\overline{DQS}$ low-impedance time from CK/$\overline{CK}$	$t_{AC\ min}$	$t_{AC\ max}$	ns	
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.24	ns	
t_{QHS}	Data hold Skew Factor	-	0.34	ns	
t_{QH}	Data output hold time from DQS	t_{HP} - t_{QHS}	-	ns	
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	0.25	t_{CK}	
$t_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)	0.35	-	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	t_{CK}	
t_{MRD}	Mode register set command cycle time	2	-	t_{CK}	
t_{WPST}	Write postamble	0.40	0.60	t_{CK}	
t_{WPRE}	Write preamble	0.35	-	t_{CK}	
t_{IH}	Address and control input hold time	0.275	-	ps	
t_{IS}	Address and control input setup time	0.2	-	ps	
t_{RPRE}	Read preamble	0.9	1.1	t_{CK}	
t_{RPST}	Read postamble	0.4	0.6	t_{CK}	
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	t_{IS} + t_{CK} + t_{IH}		ns	
t_{RFC}	Refresh to active/Refresh command time	127.5		ns	
t_{REFI}	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	3.9		µs	
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	7.8		µs	
t_{RRD}	Active bank A to Active bank B command	7.5	-	ns	

AC Timing Specifications for DDR2 SDRAM Devices Used on Module (Part 2 of 2)

Symbol	Parameter	-3C		Unit	Notes
		Min.	Max.		
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$	2	-	t_{CK}	
t_{WR}	Write recovery time	15	-	ns	
WR	Write recovery time with Auto-Precharge	t_{WR}/t_{CK}		ns	
t_{DAL}	Auto precharge write recovery + precharge time	WR +t_{RP}	-	t_{CK}	
t_{WTR}	Internal write to read command delay	7.5	-	ns	
t_{RTP}	Internal read to precharge command delay	7.5		ns	
t_{XSNR}	Exit self refresh to a Non-read command	t_{RFC} +10		ns	
t_{XSRD}	Exit self refresh to a Read command	200		t_{CK}	
t_{XP}	Exit precharge power down to any Non- read command	2	-	t_{CK}	
t_{XARD}	Exit active power down to read command	2	-	t_{CK}	
t_{XARDS}	Exit active power down to read command	7-AL		t_{CK}	
t_{CKE}	CKE minimum pulse width	3		t_{CK}	
t_{OIT}	OCD drive mode output delay	0	12	ns	
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	t_{AC} (min)	t_{AC} (max) +1	ns	
t_{AONPD}	ODT turn-on (Power down mode)	$t_{AC(min)}$ +2	2t_{CK} + $t_{AC(max)}$ +1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	ns	
t_{AOFPD}	ODT turn-off (Power down mode)	$t_{AC(min)}$ +2	2.5t_{CK} + $t_{AC(max)}$ +1	ns	
t_{ANPD}	ODT to power down entry latency	3		t_{CK}	
t_{AXPD}	ODT power down exit latency	8		t_{CK}	
t_{RAS}	Row Active Time	45	70000	ns	
t_{RCD}	RAS to CAS delay	15	-	ns	
t_{RC}	Row Cycle Time	60	-	ns	
t_{RP}	Row Precharge Time	15	-	ns	

Package Dimensions



Unit: mm

Revision Log

Rev	Date	Modification
0.1	05/2008	Preliminary Release
1.0	06/2008	Official release