240pin DDR2 SDRAM Fully Buffered DIMM Based on 64Mx8 & 128Mx4 DDR2 SDRAM - B die

Features

- 512MB 64Mx72 DDR2 Fully Buffered DIMM based on 64Mx8 DDR2 SDRAM (NT5TU64M8BE-25C).
- 1GB 128Mx72 DDR2 Fully Buffered DIMM based on 64Mx8 DDR2 SDRAM (NT5TU64M8BE-25C).
- 2GB 256Mx72 DDR2 Fully Buffered DIMM based on 128Mx4 DDR2 SDRAM (NT5TU128M4BE-25C).
- JEDEC Standard 240-pin Fully Buffered ECC Dual In-Line Memory Module.
- Performance:

FBDIMM	PC2-6400	Unit
Speed Sort	-2C	
DRAM	DDR2-800	
DIMM $\overline{CAS}$ Latency	5	t CK
Channel Clock	200	MHz
DRAM Clock	400	MHz

- Inputs and outputs are SSTL-18 compatible.
- V_{DD} = 1.8Volt ± 0.1, V_{DDQ} = 1.8Volt ± 0.1.
- Host Interface and AMB component industry standard compliant.
- Support SMBus protocol interface for access to the AMB configuration registers.
- Detects errors on the channel and reports them to the host memory controller.
- Automatic DDR2 DRAM Bus Calibration.
- Full Host Control of the DDR2 DRAMs.
- Over-Temperature Detection and Alert.
- MBIST & IBIST Test Functions.
- Transparent Mode for DRAM Test Support.
- Serial Presence Detect (SPD)
- Gold contacts
- RoHS Compliance
- SDRAM in 60-ball BGA Package

Description

NT512T72U89B1BD-2C, NT1GT72U8PB1BD-2C, and NT2GT72U4NB1BD-2C are Fully Buffered 240-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Dual In-Line Memory Module (DIMM) with **Intel designed Heat Spreader**, organized as one rank on 64Mx72; two ranks of 128Mx72, and 256Mx72 high-speed memory array. The module uses nine 64Mx8 (512MB), eighteen 64Mx8 (1GB), and thirty-six 128Mx4 (2GB) DDR2 SDRAMs in BGA packages. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint. The DIMM is intended for use in applications operating up to 400MHz clock speeds and achieves high-speed data transfer rates of up to 800 MHz.

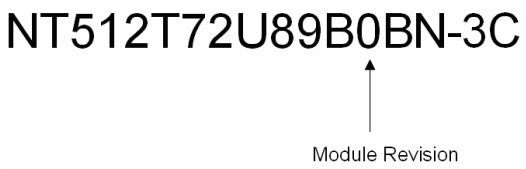
Ordering Information

Part Number	AMB	Speed			Organization	Leads	Note
NT2GT72U4NB1BD-2C	IDT C1-800	400MHz (2.5ns @ CL = 5)	DDR2-800	PC2-6400	256Mx72	Gold	Intel Designed Heat Spreader
NT1GT72U8PB1BD-2C					128Mx72		
NT512T72U89B1BD-2C					64Mx72		

Note:

Module revision will change if AMB, PCB, or Heat spreader version changes.

Example:



DIMM Connector Pin Description

Pin Name	Pin Description
SCK	System Clock Input, positive line
$\overline{SCK}$	System Clock Input, negative line
PN0-PN13	Primary Northbound Data, positive lines
$\overline{PN0}$-$\overline{PN13}$	Primary Northbound Data, negative lines
PS0-PS9	Primary Southbound Data, positive lines
$\overline{PS0}$-$\overline{PS9}$	Primary Southbound Data, negative lines
SN0-SN13	Secondary Northbound Data, positive lines
$\overline{SN0}$-$\overline{SN13}$	Secondary Northbound Data, negative lines
SS0-SS9	Secondary Southbound Data, positive lines
$\overline{SS0}$-$\overline{SS9}$	Secondary Southbound Data, negative lines
SCL	Serial Presence Detect (SPD) Clock Input
SDA	SPD Data Input / Output
SA0-SA2	SPD Address Inputs, also used to select the DIMM number in the AMB
VID0-VID1	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID0 is V_{DD} value: OPEN=1.8V, GND=1.5V; VID1 is V_{CC} value: OPEN=1.5V, GND=1.2V
$\overline{RESET}$	AMB reset signal
RFU	Reserved for Future Use
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5V)
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8V)
V_{TT}	DRAM Address/Command/Clock Termination Power (V_{DD}/2)
V_{DDSPD}	SPD Power (3.3V)
V_{SS}	Ground
DNU/M_TEST	It provides an external connection on 512MB/1GB for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.

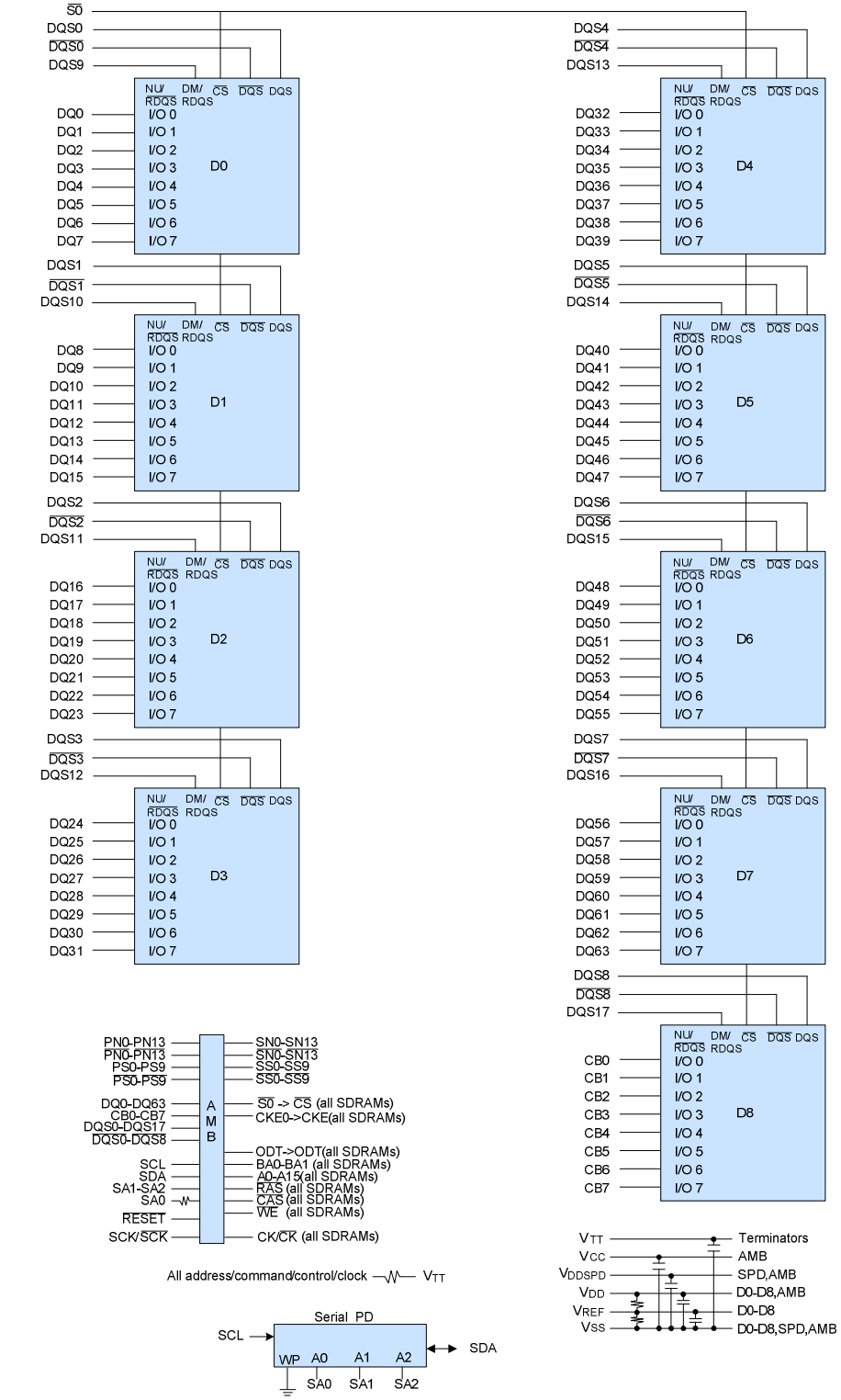
Note:
1. System Clock Signals SCK and SCK switch at one half the DRAM CK/$\overline{CK}$ frequency
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

DDR2 240-pin FBDIMM Pinout

Pin	Front Side	Pin	Front Side	Pin	Front Side	Pin	Back Side	Pin	Back Side	Pin	Back Side
1	V_{DD}	42	V_{SS}	82	PS4	121	V_{DD}	162	V_{SS}	202	SS4
2	V_{DD}	43	V_{SS}	83	$\overline{PS4}$	122	V_{DD}	163	V_{SS}	203	$\overline{SS4}$
3	V_{DD}	44	RFU*	84	V_{SS}	123	V_{DD}	164	RFU*	204	V_{SS}
4	V_{SS}	45	RFU*	85	V_{SS}	124	V_{SS}	165	RFU*	205	V_{SS}
5	V_{DD}	46	V_{SS}	86	RFU*	125	V_{DD}	166	V_{SS}	206	RFU*
6	V_{DD}	47	V_{SS}	87	RFU*	126	V_{DD}	167	V_{SS}	207	RFU*
7	V_{DD}	48	PN12	88	V_{SS}	127	V_{DD}	168	SN12	208	V_{SS}
8	V_{SS}	49	$\overline{PN12}$	89	V_{SS}	128	V_{SS}	169	$\overline{SN12}$	209	V_{SS}
9	V_{CC}	50	V_{SS}	90	PS9	129	V_{CC}	170	V_{SS}	210	SS9
10	V_{CC}	51	PN6	91	$\overline{PS9}$	130	V_{CC}	171	SN6	211	$\overline{SS9}$
11	V_{SS}	52	$\overline{PN6}$	92	V_{SS}	131	V_{SS}	172	$\overline{SN6}$	212	V_{SS}
12	V_{CC}	53	V_{SS}	93	PS5	132	V_{CC}	173	V_{SS}	213	SS5
13	V_{CC}	54	PN7	94	$\overline{PS5}$	133	V_{CC}	174	SN7	214	$\overline{SS5}$
14	V_{SS}	55	$\overline{PN7}$	95	V_{SS}	134	V_{SS}	175	$\overline{SN7}$	215	V_{SS}
15	V_{TT}	56	V_{SS}	96	PS6	135	V_{TT}	176	V_{SS}	216	SS6
16	VID1	57	PN8	97	$\overline{PS6}$	136	VID0	177	SN8	217	$\overline{SS6}$
17	$\overline{RESET}$	58	$\overline{PN8}$	98	V_{SS}	137	DNU/M_TEST	178	$\overline{SN8}$	218	V_{SS}
18	V_{SS}	59	V_{SS}	99	PS7	138	V_{SS}	179	V_{SS}	219	SS7
19	RFU**	60	PN9	100	$\overline{PS7}$	139	RFU**	180	SN9	220	$\overline{SS7}$
20	RFU**	61	$\overline{PN9}$	101	V_{SS}	140	RFU**	181	$\overline{SN9}$	221	V_{SS}
21	V_{SS}	62	V_{SS}	102	PS8	141	V_{SS}	182	V_{SS}	222	SS8
22	PN0	63	PN10	103	$\overline{PS8}$	142	SN0	183	SN10	223	$\overline{SS8}$
23	$\overline{PN0}$	64	$\overline{PN10}$	104	V_{SS}	143	$\overline{SN0}$	184	$\overline{SN10}$	224	V_{SS}
24	V_{SS}	65	V_{SS}	105	RFU**	144	V_{SS}	185	V_{SS}	225	RFU**
25	PN1	66	PN11	106	RFU**	145	SN1	186	SN11	226	RFU**
26	$\overline{PN1}$	67	$\overline{PN11}$	107	V_{SS}	146	$\overline{SN1}$	187	$\overline{SN11}$	227	V_{SS}
27	V_{SS}	68	V_{SS}	108	V_{DD}	147	V_{SS}	188	V_{SS}	228	SCK
28	PN2	**KEY**		109	V_{DD}	148	SN2	**KEY**		229	$\overline{SCK}$
29	$\overline{PN2}$	69	V_{SS}	110	V_{SS}	149	$\overline{SN2}$	189	V_{SS}	230	V_{SS}
30	V_{SS}	70	PS0	111	V_{DD}	150	V_{SS}	190	SS0	231	V_{DD}
31	PN3	71	$\overline{PS0}$	112	V_{DD}	151	SN3	191	$\overline{SS0}$	232	V_{DD}
32	$\overline{PN3}$	72	V_{SS}	113	V_{DD}	152	$\overline{SN3}$	192	V_{SS}	233	V_{DD}
33	V_{SS}	73	PS1	114	V_{SS}	153	V_{SS}	193	SS1	234	V_{SS}
34	PN4	74	$\overline{PS1}$	115	V_{DD}	154	SN4	194	$\overline{SS1}$	235	V_{DD}
35	$\overline{PN4}$	75	V_{SS}	116	V_{DD}	155	$\overline{SN4}$	195	V_{SS}	236	V_{DD}
36	V_{SS}	76	PS2	117	V_{TT}	156	V_{SS}	196	SS2	237	V_{TT}
37	PN5	77	$\overline{PS2}$	118	SA2	157	SN5	197	$\overline{SS2}$	238	V_{DDSPD}
38	$\overline{PN5}$	78	V_{SS}	119	SDA	158	$\overline{SN5}$	198	V_{SS}	239	SA0
39	V_{SS}	79	PS3	120	SCL	159	V_{SS}	199	SS3	240	SA1
40	PN13	80	$\overline{PS3}$			160	SN13	200	$\overline{SS3}$		
41	$\overline{PN13}$	81	V_{SS}			161	$\overline{SN13}$	201	V_{SS}		

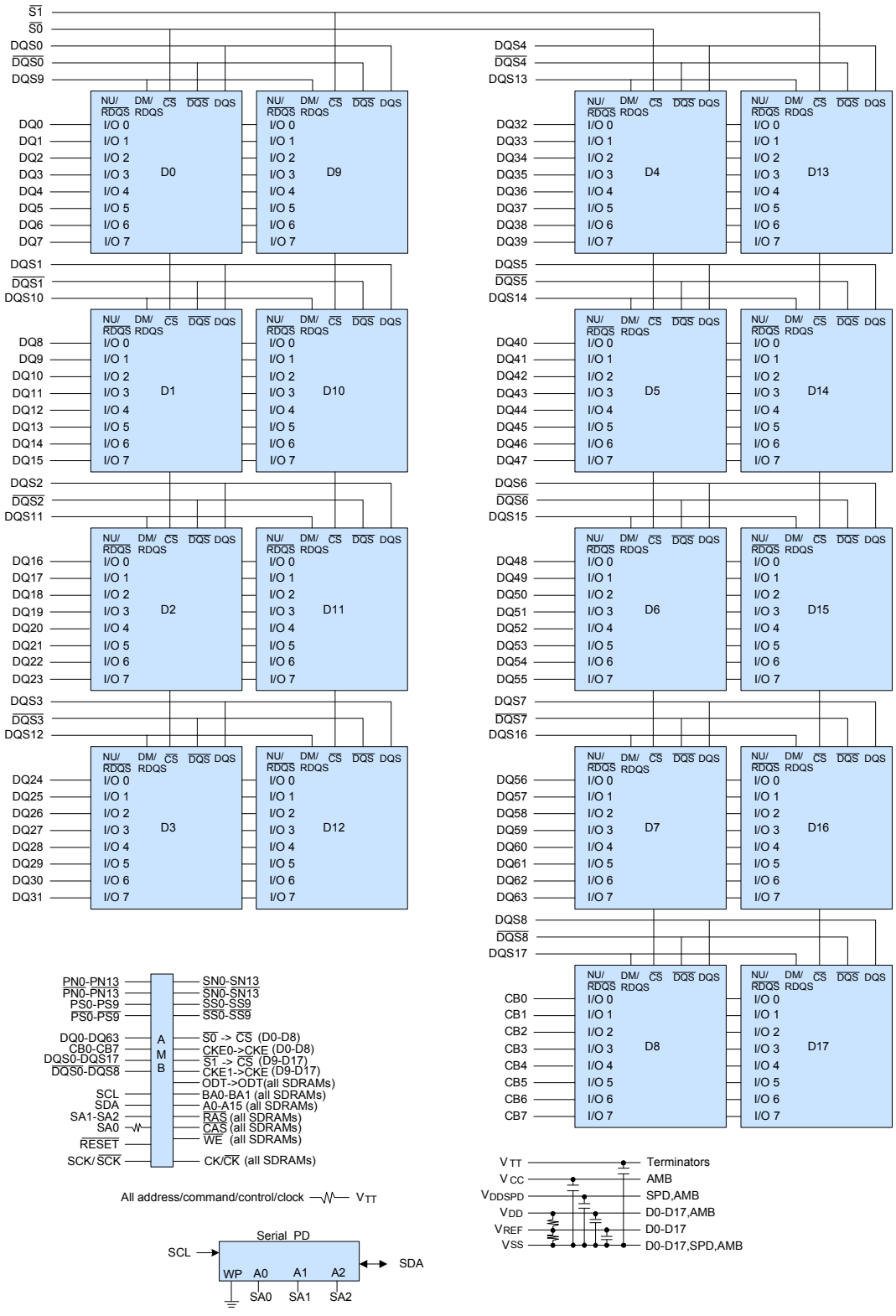
Note:
RFU = Reserved Future Use
* These pin positions are reserved for forwarded clocks to be used in future module implementation
** These pin positions are reserved for future architecture flexibility
The following signals are CRC bits and thus appear out of the normal sequence: PN12/$\overline{PN12}$, SN12/$\overline{SN12}$, PN13/$\overline{PN13}$, SN13/$\overline{SN13}$, PS9/$\overline{PS9}$, SS9/$\overline{SS9}$

Functional Block Diagram (512MB, 1Rank, 64Mx8 DDR2 SDRAMs)



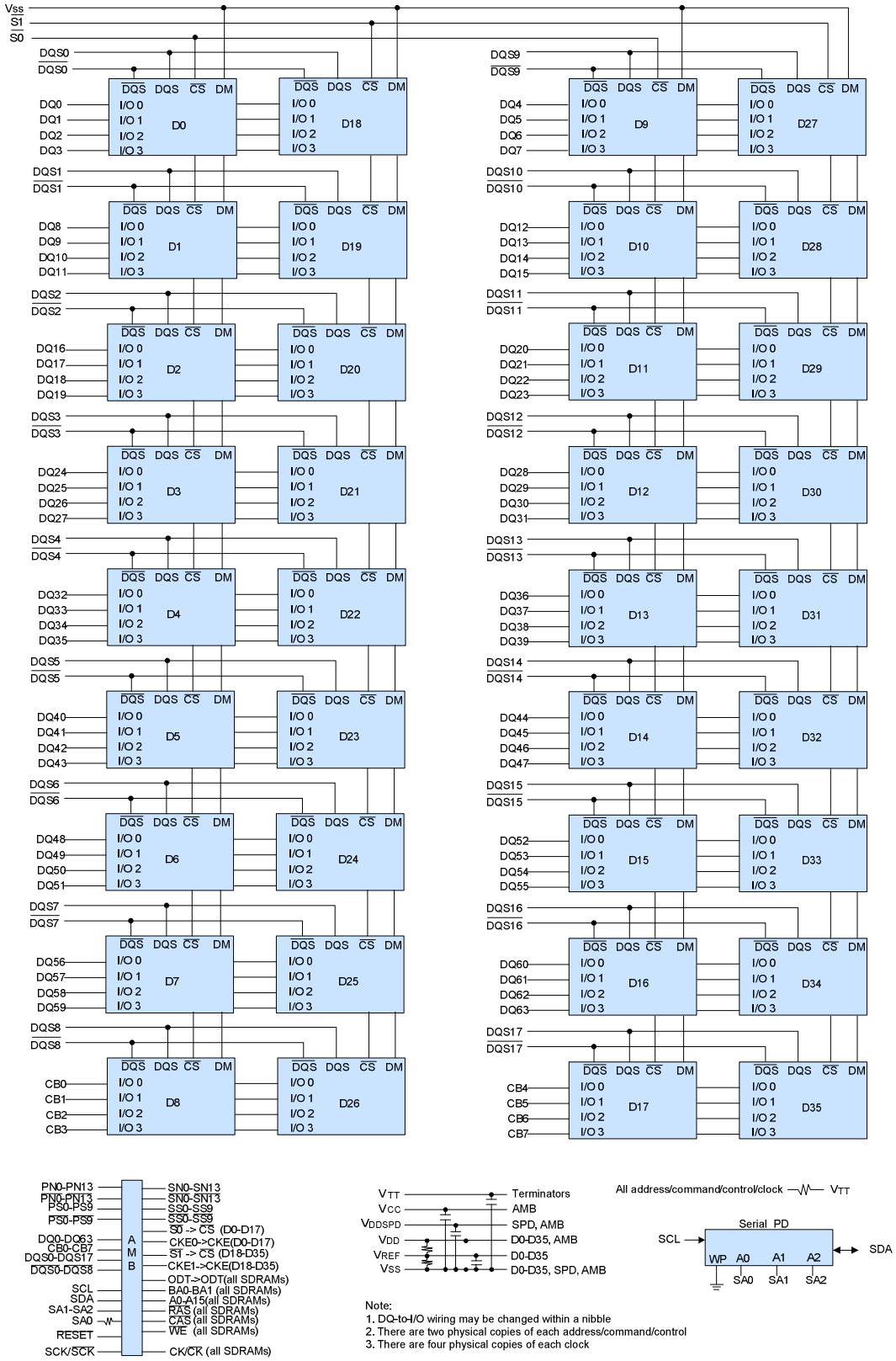
Notes : 1. DQ-to-I/O wiring may be changed within a byte
2. There are two physical copies of each address/command/control/clock

Functional Block Diagram (1GB, 2Ranks, 64Mx8 DDR2 SDRAMs)



Notes : 1. DQ-to-I/O wiring may be changed within a byte
2. There are two physical copies of each address/command/ control/clock

Functional Block Diagram (2GB, 2Ranks, 128Mx4 DDR2 SDRAMs)



Note:
1. DQ-to-I/O wiring may be changed within a nibble
2. There are two physical copies of each address/command/control
3. There are four physical copies of each clock

DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See Device AC Characteristics)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{CC}	AMB supply Voltage	1.46	1.5	1.54	V	
VDD	Supply Voltage	1.7	1.8	1.9	V	1
V_{DDSPD}	EEPROM supply Voltage	3.0	3.3	3.6	V	
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1,5
VREF	I/O Reference Voltage	0.48 x VDDQ	0.50xVDDQ	0.52 x VDDQ	V	2,3
VTT	I/O Termination Voltage (System)	VREF - 0.04	VREF	VREF + 0.04	V	4

Note:
1. There is no specific device VDD supply requirement for SSTL_18 compliance. However, under all conditions VDDQ must be less than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5VDDQ of the transmitting device and VREF is expected to track variations is VDDQ.
3. Peak to peak AC noise on VREF may not exceed ±0.2% VREF(dc).
4. VTT of transmitting device must track VREF of receiving device.
5. VDDQ tracks with VDD, VDDL tracks with VDD.

Input DC Logic Level

Symbol	Parameter/Condition	Min	Max	Unit
VIH (AC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.3	V
VIL (AC)	Input Low (Logic 0) Voltage	-0.3	VREF - 0.125	V

Input AC Logic Level

Symbol	Parameter/Condition	Min	Max	Unit
VIH (AC)	Input High (Logic 1) Voltage	V REF + 0.20	-	V
VIL (AC)	Input Low (Logic 0) Voltage	-	V REF - 0.20	V

Environmental Requirements

Symbol	Parameter	Rating	Units	Note
T_{OPR}	Operating temperature	-		1
H_{OPR}	Operating humidity (relative)	10 to 90	%	2
T_{STG}	Storage temperature	-50 to +100	ºC	2
H_{STG}	Storage humidity (without condensation)	5 to 95	%	2
P_{BAR}	Barometric pressure (operating & Storage)	105 to 69	K pascal	2

Note:
1. The designer must meet the case temperature specifications for individual module components. Please refer to device spec.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Serial Presence Detect -- Part 1 of 2

Byte	Description	PC2-6400 (-2C) Serial PD Data Entry (Hexadecimal)		
		512MB	1GB	2GB
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	92	92	92
1	SPD Revision	11	11	11
2	Key Byte / DRAM Device Type	09	09	09
3	Voltage Levels of this Assembly	12	12	12
4	SDRAM Addressing	44	44	48
5	Module Physical Attributes	23	23	23
6	Modules Type / Thickness	07	07	07
7	Module Organization	09	11	10
8	Fine Timebase Dividend and Divisor	52	52	52
9	Medium Timebase Dividend	01	01	01
10	Medium Timebase Divisor	04	04	04
11	SDRAM Minimum Cycle Time (tCKmin)	0A	0A	0A
12	SDRAM Maximum Cycle Time (tCKmax)	20	20	20
13	SDRAM $\overline{CAS}$ Latencies Supported	43	43	43
14	SDRAM Minimum CAS Latency Time (tCAS)	32	32	32
15	SDRAM Write Recovery Times Supported	42	42	42
16	SDRAM Write Recovery Time (tWR)	3C	3C	3C
17	SDRAM Write Latencies Supported	42	42	42
18	SDRAM Additive Latencies Supported	40	40	40
19	SDRAM Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (tRCD)	32	32	32
20	SDRAM Minimum Row Active to Row Active Delay (tRRD)	1E	1E	1E
21	SDRAM Minimum Row Precharge Time (tRP)	32	32	32
22	SDRAM Upper Nibbles for tRAS and tRC	00	00	00
23	SDRAM Minimum Active to Precharge Time (tRAS)	B4	B4	B4
24	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC)	F0	F0	F0
25~26	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	A401	A401	A401
27	SDRAM Internal Write to Read Command Delay (tWTR)	1E	1E	1E
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	1E	1E	1E
29	SDRAM Burst Lengths Supported	03	03	03
30	SDRAM Terminations Supported	07	07	07
31	SDRAM Drivers Supported	01	01	01
32	SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication	C2	C2	C2
33	Tcasemax / DT4R4W	53	51	51
34	Thermal resistance of SDRAM device package from top (case0 to ambient (Psi T-A SDRAM)	7A	7A	7A
35	DT0: Case temperature rise from ambient due to IDD2N/precharge operation minus 2.8°C offset temperature	50	60	60
36	DT2N/DT2Q: Case temperature rise from ambient due to IDD2Q/precharge quiet standby operation for FBDIMM	2F	35	35
37	DT2P: Case temperature rise from ambient due to IDD2P/precharge power-down operation	37	37	37
38	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation	27	2F	2F
39	DT4R: Case temperature rise from ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W)	4C	56	56

Serial Presence Detect – Part 2 of 2

Byte	Description	PC2-6400 (-2C) Serial PD Data Entry (Hexadecimal)		
		512MB	1GB	2GB
40	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation	26	29	29
41	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation	28	28	28
42-78	Reserved	--	--	--
79	ODT termination	01	21	21
80	Reserved	00	00	00
81-82	FB-DIMM Channel Protocols Supported	0200	0200	0200
83	Back to back access turn around time	10	10	10
84	AMB Read Access Time for DDR2-800	36	36	36
85	AMB Read Access Time for DDR2-667	34	34	34
86	AMB Read Access Time for DDR2-533	32	32	32
87	Thermal resistance of AMB package from top(junction) to ambient(Psi T-A SDRAM) at still air condition	2A	2A	2A
88	AMB DT Idle_0	5D	5D	64
89	AMB DT Idle_1	71	71	7B
90	AMB DT Idle_2	65	65	65
91	AMB DT Active_1	9B	9B	A3
92	AMB DT Active_2	7F	7F	87
93	AMB DT L0s	00	00	00
94-97	Reserved	--	--	--
98	AMB junction temp. Max. (Tjmax)	1F	1F	1F
99	Reserved	0A	0A	0A
100	Reserved	00	00	00
101	AMB personality Bytes: Pre-initialization(1)	00	00	00
102	AMB personality Bytes: Pre-initialization(2)	E2	E2	E2
103	AMB personality Bytes: Pre-initialization(3)	62	62	62
104	AMB personality Bytes: Pre-initialization(4)	20	20	20
105	AMB personality Bytes: Pre-initialization(5)	80	80	80
106	AMB personality Bytes: Pre-initialization(6)	9C	9C	9C
107	AMB personality Bytes: Post-initialization(1)	00	00	00
108	AMB personality Bytes: Post-initialization(2)	00	00	00
109	AMB personality Bytes: Post-initialization(3)	F0	F0	F0
110	AMB personality Bytes: Post-initialization(4)	70	70	70
111	AMB personality Bytes: Post-initialization(5)	60	60	60
112	AMB personality Bytes: Post-initialization(6)	60	60	60
113	AMB personality Bytes: Post-initialization(7)	60	60	60
114	AMB personality Bytes: Post-initialization(8)	60	60	60
115-116	AMB manufacture's JEDEC ID code	7FB3	7FB3	7FB3
117-118	Module ID: Module Manufacture's JEDEC ID code	830B	830B	830B
119-255	Reserved	--	--	--

Operating, Standby, and Refresh Currents

(Test condition: Vdd=1.8V, Vcc=1.5V, Room temperature)

Symbol	Parameter/Condition	512MB	1GB	2GB	Unit
Idd_Idle_0	**Idle Current, single or last DIMM.** L0 state, idle (0BW). Primary channel enabled; Secondary Channel disabled. Command and address lines stable, DRAM clock active. CKE high.	968	1364	2431	mA
Icc_Idle_0		2871	2871	2871	mA
Idd_Idle_1	**Idle Current, first DIMM.** L0 stage, idle (0BW). Primary and Secondary channels enabled. CKE high. Command and address line stable. DRAM clock active.	968	1364	2431	mA
Icc_Idle_1		4301	4301	4301	mA
Idd_Idle_2	**Idle Current, DRAM power down.** L0stage, idle (0BW). Primary and Secondary channels enabled CKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low.	209	231	297	mA
Icc_Idle_2		4312	4312	4312	mA
Idd_Active_1 (Read)	**Active Power.** L0 state. 50% DRAM BW to downstream DIMM, 100% read. Primary and Secondary channels enabled, DRAM clock active, CKE high.	2640	3498	5412	mA
Icc_Active_1 (Read)		4851	4851	4851	mA
Idd_Active_1 (Write)	**Active Power.** L0 state. 50% DRAM BW to downstream DIMM, 100% write. Primary and Secondary channels enabled, DRAM clock active, CKE high.	2728	3498	5412	mA
Icc_Active_1 (Write)		4653	4653	4653	mA
Idd_Active_2	**Active Power, data pass through.** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. CKE high. Command and address lines stable. DRAM clock active.	979	1386	2464	mA
Icc_Active_2		4554	4554	4554	mA
Idd_Training	Primary and Secondary channels enabled. 100% toggle on all channel lanes. DRAMs idle. 0BW. CKE high, Command and address line stable. DRAM clock active. CKE high.	979	1386	2453	mA
Icc_Training		4224	4224	4224	mA

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 1 of 2)

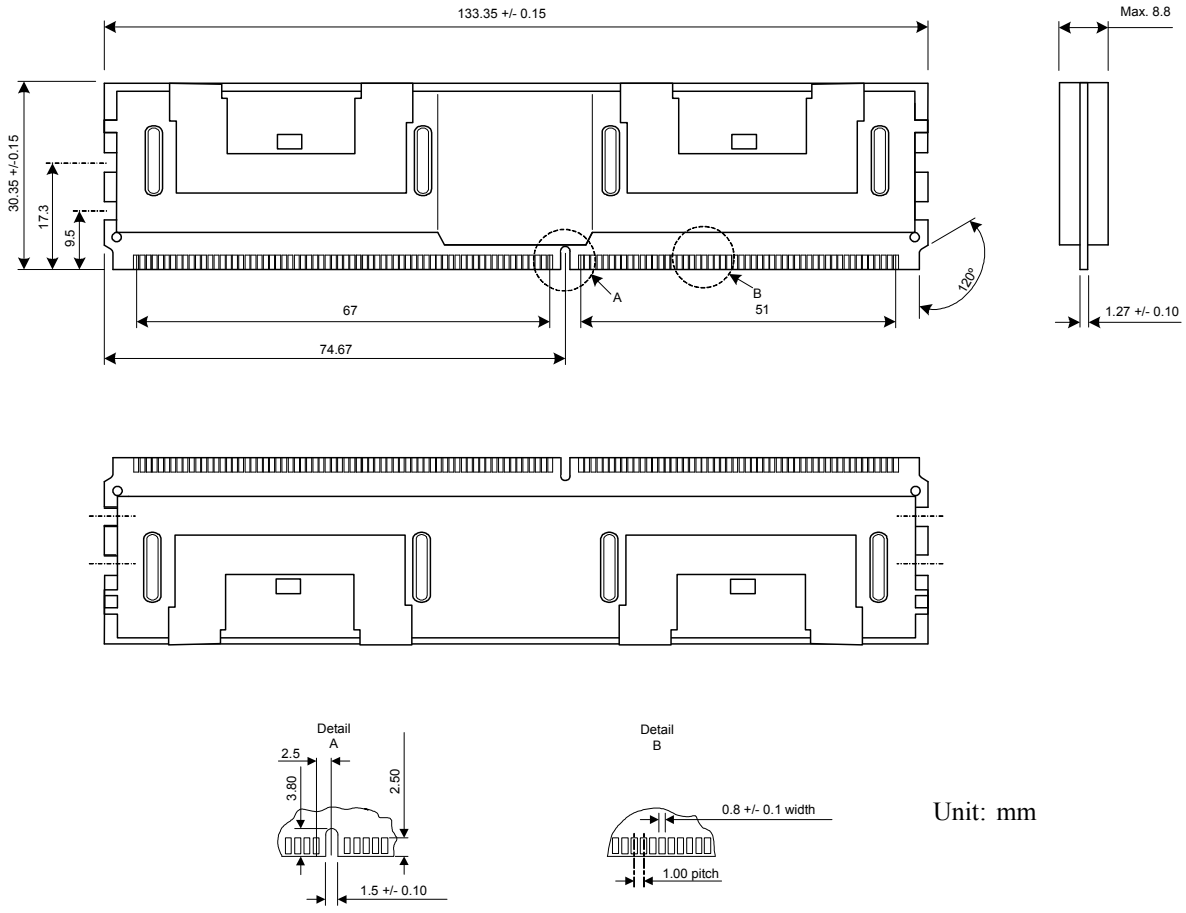
Symbol	Parameter	-2C		Unit	Notes
		Min.	Max.		
t_{CK}	Average clock period	2500	8000	ps	
t_{CH}	Average clock high-level width	0.48	0.52	t_{CK}	
t_{CL}	Average clock low-level width	0.48	0.52	t_{CK}	
WL	Average command to DQS associated clock edge	RL-1		nCK	
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	0.25	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	t_{CK}	
$t_{DQSL,(H)}$	DQS input low (high) pulse width (write cycle)	0.35	-	t_{CK}	
t_{WPRE}	Write preamble	0.35	-	t_{CK}	
t_{WPST}	Write postamble	0.40	0.60	t_{CK}	
t_{IS}	Address and control input setup time	175	-	ps	
t_{IH}	Address and control input hold time	250	-	ps	
t_{IPW}	Input pulse width	0.6	-	t_{CK}	
t_{DS}	DQ and DM input setup time	50	-	ps	
t_{DH}	DQ and DM input hold time	125	-	ps	
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	t_{CK}	
t_{AC}	DQ output access time from CK/$\overline{CK}$	-400	+400	ps	
t_{DQSCK}	DQS output access time from CK/$\overline{CK}$	-350	+350	ps	
t_{HZ}	Data-out high-impedance time from CK/$\overline{CK}$	-	$t_{AC\ max}$	ps	
$t_{LZ(DQS)}$	DQS/$\overline{DQS}$ low-impedance time from CK/$\overline{CK}$	$t_{AC\ min}$	$t_{AC\ max}$	ps	
$t_{LZ(DQ)}$	Data-out low-impedance time from CK/$\overline{CK}$	$2t_{AC\ min}$	$t_{AC\ max}$	ps	
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	200	ps	
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	$t_{CH(abs)}$ or $t_{CL(abs)}$	-	ps	
t_{QHS}	Data hold Skew Factor	-	300	ps	
t_{QH}	Data output hold time from DQS	t_{HP} - t_{QHS}	-	ps	
t_{RPRE}	Read preamble	0.9	1.1	t_{CK}	
t_{RPST}	Read postamble	0.4	0.6	t_{CK}	
t_{RRD}	Active bank A to Active bank B command	7.5	-	ns	
t_{FAW}	Four Activate Window	35	-	ns	
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ command delay	2	-	nCK	
t_{WR}	Write recovery time	15	-	ns	
t_{DAL}	Auto precharge write recovery + precharge time	WR +t_{nRP}	-	nCK	
t_{WTR}	Internal write to read command delay	7.5	-	ns	
t_{RTP}	Internal read to precharge command delay	7.5	-	ns	
t_{CKE}	CKE minimum pulse width	3	-	nCK	

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T_{CASE} = 0 ℃ ~ 85 ℃; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-2C		Unit	Notes
		Min.	Max.		
t_{XSNR}	Exit self refresh to a Non-read command	t_{RFC} +10	-	ns	
t_{XSRD}	Exit self refresh to a Read command	200	-	nCK	
t_{XP}	Exit precharge power down to any Non- read command	2	-	nCK	
t_{XARD}	Exit active power down to read command	2	-	nCK	
t_{XARDS}	Exit active power down to read command	8-AL	-	nCK	
t_{AOND}	ODT turn-on delay	2	2	nCK	
t_{AON}	ODT turn-on	$t_{AC(min)}$	$t_{AC(max)}$ +0.7	ns	
t_{AONPD}	ODT turn-on (Power down mode)	$t_{AC(min)}$ +2	$2t_{CK}$ + $t_{AC(max)}$ +1	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	nCK	
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ +0.6	ns	
t_{AOFPD}	ODT turn-off (Power down mode)	$t_{AC(min)}$ +2	$2.5t_{CK}$ + $t_{AC(max)}$ +1	ns	
t_{ANPD}	ODT to power down entry latency	3	-	nCK	
t_{AXPD}	ODT power down exit latency	8		nCK	
t_{MRD}	Mode register set command cycle time	2	-	nCK	
t_{MOD}	MRS command to ODT update delay	0	12	ns	
t_{OIT}	OCD drive mode output delay	0	12	ns	
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	t_{IS} + t_{CK} + t_{IH}	-	ns	
WR	Write recovery time with Auto-Precharge	t_{WR}/t_{CK}		ns	
Refresh parameters					
t_{RFC}	Refresh to active/Refresh command time	105		ns	
t_{REFI}	Average Periodic Refresh Interval (85ºC < T_{CASE} ≤ 95ºC)	3.9		µs	
	Average Periodic Refresh Interval (0ºC ≤ T_{CASE} ≤ 85ºC)	7.8		µs	
Speed Grade Definition					
t_{RAS}	ACT to PRE delay	45	70000	ns	
t_{RCD}	ACT to RD(A) or WT(A) delay	12.5	-	ns	
t_{RP}	PRE to ACT delay	12.5	-	ns	
t_{RC}	ACT to ACT delay	57.5	-	ns	

Package Dimensions



Unit: mm

Revision Log

Rev	Date	Modification
0.1	09/2007	Preliminary Release.
1.0	09/2007	Official Release.