



200 pin Unbuffered DDR2 SO-DIMM

Based on DDR2-533/667/800 32Mx16/64Mx8 SDRAM B-Die

Features

• Performance:

	PC2-4200	PC2-5300	PC2-6400	PC2-6400	Unit
Speed Sort	-37B	-3C	-25D	-25C	
DIMM CAS Latency	4	5	6	5	
fck – Clock Frequency	266	333	400	400	MHz
tck – Clock Cycle	3.75	3	2.5	2.5	ns
fDQ – DQ Burst Frequency	533	667	800	800	MHz

- 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- 32Mx64 and 64Mx64 Unbuffered DDR2 SO-DIMM based on 32Mx16 DDR2 SDRAM B-Die devices.
- 128Mx64 Unbuffered DDR2 SO-DIMM based on 64Mx8 DDR2 SDRAM B-Die devices.
- Intended for 266MHz, 333MHz, and 400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
- SDRAMs have 4 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Programmable Operation:
 - DIMM CAS Latency: 3, 4, 5 (-37B/-3C/-25C)
 - DIMM CAS Latency: 4, 5, 6 (-25D)
- Burst Type: Sequential or Interleave
- Burst Length: 4, 8
- Operation: Burst Read and Write
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- 13/10/1 Addressing (256MB)
- 13/10/2 Addressing (512MB)
- 14/10/2 Addressing (1GB)
- 7.8 μ s Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- SDRAMs in 84-ball BGA Package (256MB & 512MB)
- SDRAMs in 60-ball BGA Package (1GB)
- RoHS compliance
- Halogen free (p/n list in page 2)

Description

NT256T64UH4B0FN, NT512T64UH8B0FN, NT1GT64U8HB0BN, NT256T64UH4B0CN, NT512T64UH8B0CN, and NT1GT64U8HB0AN are unbuffered 200-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as one rank of 32x64 (256MB), two ranks of 64x64 (512MB), and two ranks of 128x64(1GB) high-speed memory array. Modules use four 32Mx16 (256MB) and eight 32Mx16 (512MB) 84-ball BGA packaged devices. Modules use sixteen 64Mx8 (1GB) 60-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 266MHz/333MHz/400MHz clock speeds and achieves high-speed data transfer rates of 533MHz/667MHz/800MHz. Prior to any access operation, the device \overline{CAS} latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Power	Leads
NT256T64UH4B0FN-25D	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)	32Mx64	1.8V	Gold
NT256T64UH4B0FN-3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)			
NT256T64UH4B0CN-3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)			
NT256T64UH4B0FN-37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)			
NT512T64UH8B0FN-25D	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)	64Mx64		
NT512T64UH8B0FN-3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)			
NT512T64UH8B0CN-3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)			
NT512T64UH8B0FN-37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)			
NT1GT64U8HB0BN-25C	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)	128Mx64		
NT1GT64U8HB0AN-25C	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)			
NT1GT64U8HB0BN-25D	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)			
NT1GT64U8HB0BN-3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)			
NT1GT64U8HB0AN-3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)			
NT1GT64U8HB0BN-37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)			

Note:

NT256T64UH4B0CN-3C, NT512T64UH8B0CN-3C, NT1GT64U8HB0AN-3C, and NT1GT64U8HB0AN-25C are Halogen free products.

Pin Description

CK0, CK1, CK0, CK1	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
RAS	Row Address Strobe	$\overline{DQS0}$ - $\overline{DQS7}$	Differential data strobes
CAS	Column Address Strobe	DM0-DM7	Input Data Masks
\overline{WE}	Write Enable	V _{DD}	Power (1.8V)
$\overline{CS0}$, CS1	Chip Selects	V _{REF}	Ref. Voltage for SSTL_18 inputs
A0-A13	Row Address Inputs	V _{DDSPD}	Serial EEPROM positive power supply
A0-A9	Column Address Inputs	V _{SS}	Ground
A10/AP	Column Address Input/Auto-precharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	Active termination control lines	SA0, SA1	Serial Presence Detect Address Inputs
NC	No Connect		

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REF}	2	V _{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V _{SS}	4	DQ4	53	V _{SS}	54	V _{SS}	103	V _{DD}	104	V _{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V _{SS}	156	V _{SS}
7	DQ1	8	V _{SS}	57	DQ19	58	DQ23	107	BA0	108	\overline{RAS}	157	DQ48	158	DQ52
9	V _{SS}	10	DM0	59	V _{SS}	60	V _{SS}	109	\overline{WE}	110	$\overline{CS0}$	159	DQ49	160	DQ53
11	$\overline{DQS0}$	12	V _{SS}	61	DQ24	62	DQ28	111	V _{DD}	112	V _{DD}	161	V _{SS}	162	V _{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	\overline{CAS}	114	ODT0	163	NC	164	CK1
15	V _{SS}	16	DQ7	65	V _{SS}	66	V _{SS}	115	$\overline{CS1}$	116	A13	165	V _{SS}	166	$\overline{CK1}$
17	DQ2	18	V _{SS}	67	DM3	68	$\overline{DQS3}$	117	V _{DD}	118	V _{DD}	167	$\overline{DQS6}$	168	V _{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1	120	NC	169	DQS6	170	DM6
21	V _{SS}	22	DQ13	71	V _{SS}	72	V _{SS}	121	V _{SS}	122	V _{SS}	171	V _{SS}	172	V _{SS}
23	DQ8	24	V _{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V _{SS}	28	V _{SS}	77	V _{SS}	78	V _{SS}	127	V _{SS}	128	V _{SS}	177	V _{SS}	178	V _{SS}
29	$\overline{DQS1}$	30	CK0	79	CKE0	80	CKE1	129	$\overline{DQS4}$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK0}$	81	V _{DD}	82	V _{DD}	131	DQS4	132	V _{SS}	181	DQ57	182	DQ61
33	V _{SS}	34	V _{SS}	83	NC	84	NC	133	V _{SS}	134	DQ38	183	V _{SS}	184	V _{SS}
35	DQ10	36	DQ14	85	NC	86	NC	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS7}$
37	DQ11	38	DQ15	87	V _{DD}	88	V _{DD}	137	DQ35	138	V _{SS}	187	V _{SS}	188	DQS7
39	V _{SS}	40	V _{SS}	89	A12	90	A11	139	V _{SS}	140	DQ44	189	DQ58	190	V _{SS}
41	V _{SS}	42	V _{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V _{SS}	193	V _{SS}	194	DQ63
45	DQ17	46	DQ21	95	V _{DD}	96	V _{DD}	145	V _{SS}	146	$\overline{DQS5}$	195	SDA	196	V _{SS}
47	V _{SS}	48	V _{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS2}$	50	NC	99	A3	100	A2	149	V _{SS}	150	V _{SS}	199	V _{DDSPD}	200	SA1

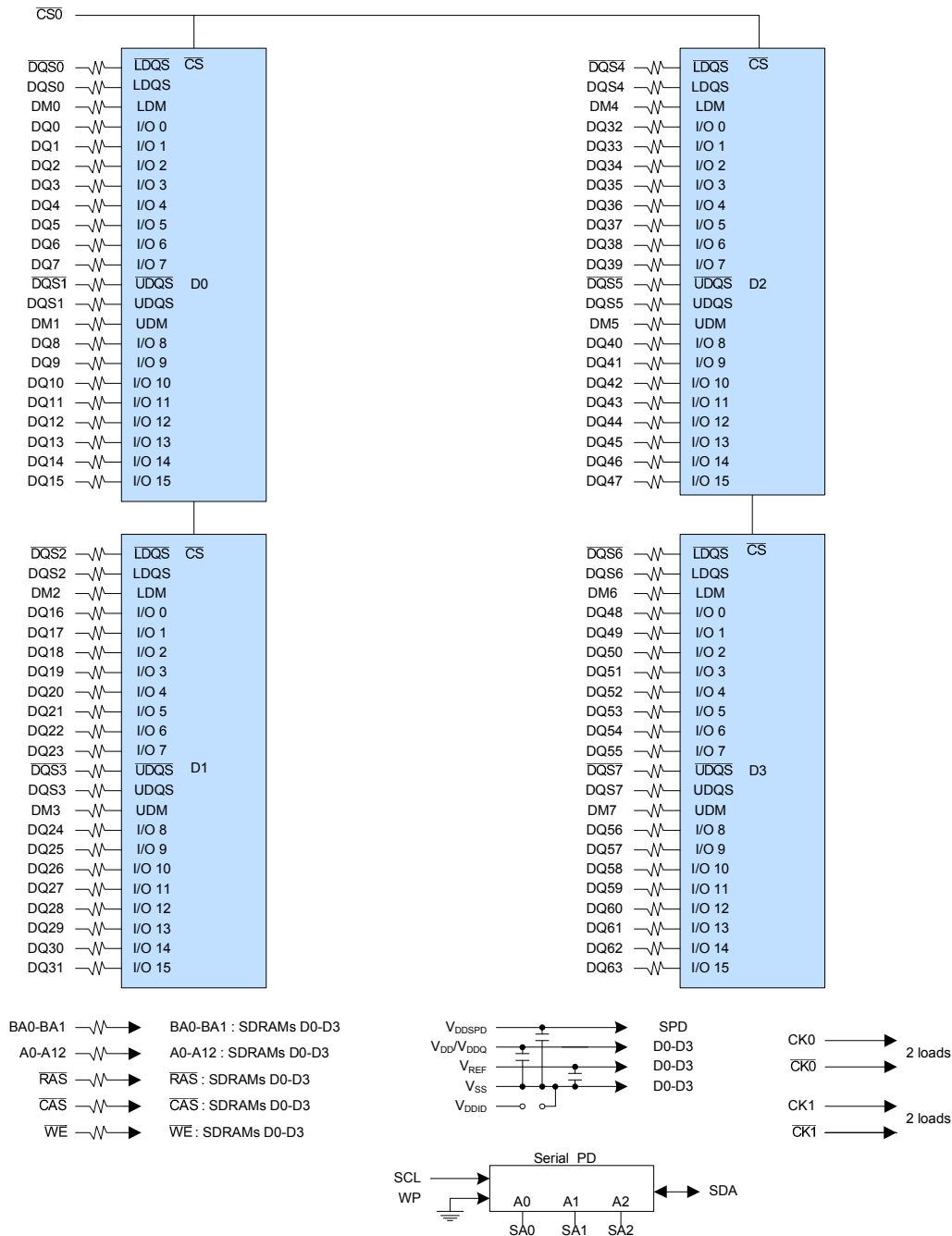
Note: All pin assignments are consistent for all 8-byte unbuffered versions.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{CK0}$, $\overline{CK1}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$, $\overline{CS1}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
\overline{RAS} , \overline{CAS} , \overline{WE}	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, \overline{RAS} , \overline{CAS} , \overline{WE} define the operation to be executed by the SDRAM.
V _{REF}	Supply		Reference voltage for SSTL-18 inputs
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11, A13	(SSTL)	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA10) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
V _{DD} , V _{SS}	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS7 $\overline{DQS0}$ – $\overline{DQS7}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA2		-	Address inputs. Connected to either V _{DD} or V _{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V _{DD} to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V _{DD} to act as a pull-up.
V _{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram

(256MB – 1 Rank, 32Mx16 DDR2 SDRAMs)

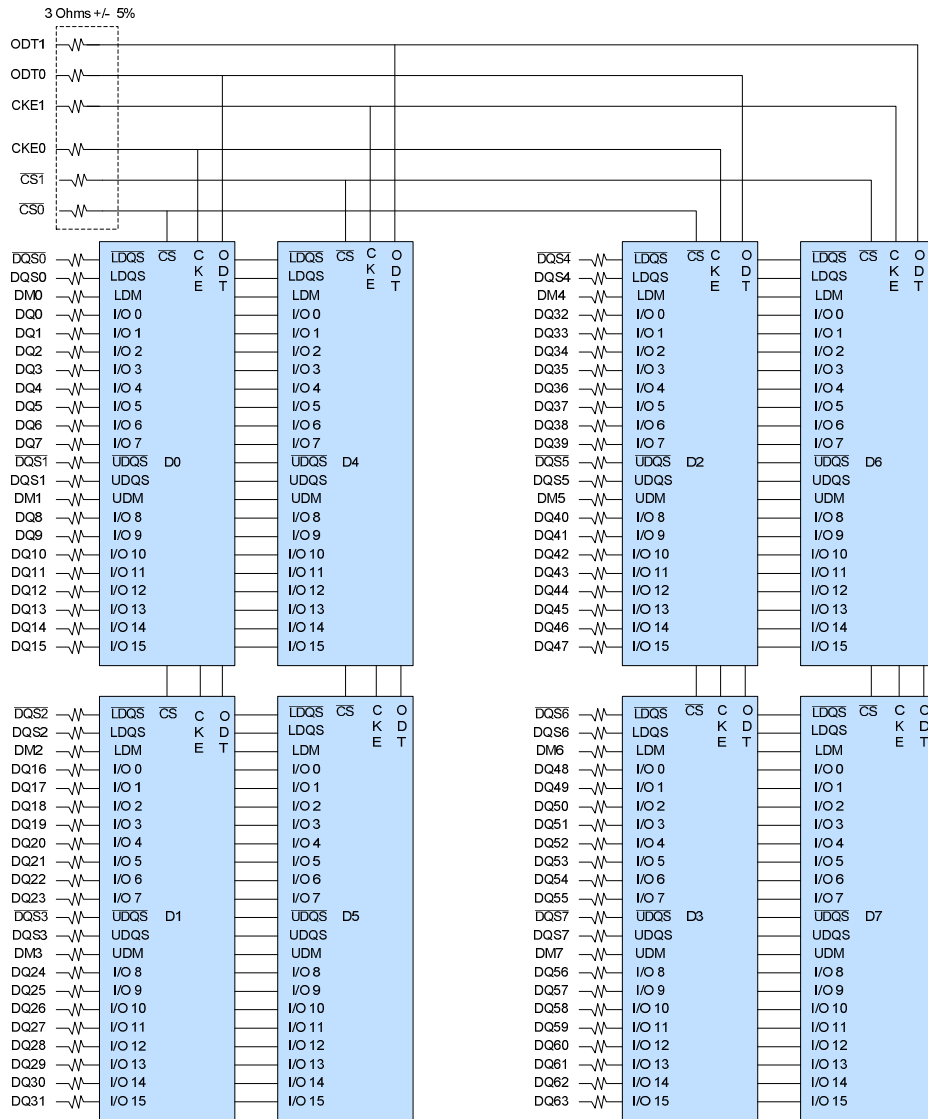


Notes :

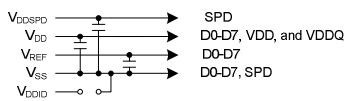
1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22+/- 5% Ohms.
4. V_{DDID} Strap connections (for memory device V_{DD}, V_{DDQ}):
 STRAP OUT (OPEN): V_{DD} = V_{DDQ}
 STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Functional Block Diagram

(512MB – 2 Ranks, 32Mx16 DDR2 SDRAMs)



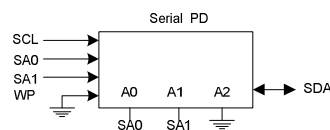
BA0-BA1 → SDRAMs D0-D7
 A0-A12 → SDRAMs D0-D7
 RAS → SDRAMs D0-D7
 CAS → SDRAMs D0-D7
 WE → SDRAMs D0-D7



CK0 → 4 loads
 CK0 → 4 loads
 CK1 → 4 loads
 CK1 → 4 loads

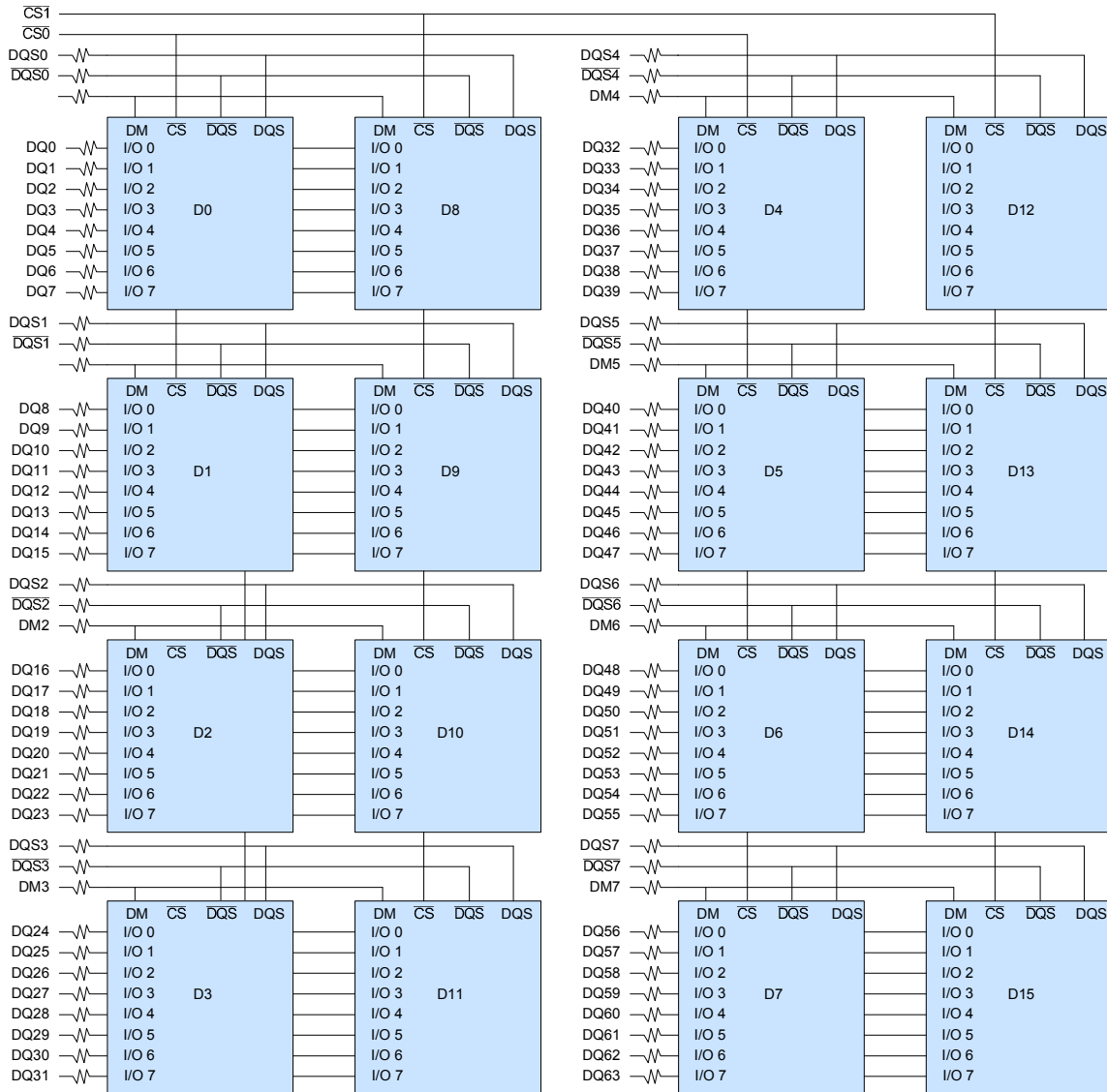
Notes:

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22+/- 5% Ohms.
4. V_{DDIO} strap connections (for memory device V_{DD}, V_{DDQ}):
 STRAP OUT (OPEN): V_{DDIO} = V_{DDQ}
 STRAP IN (V_{SS}): V_{DDIO} is not equal to V_{DDQ}.



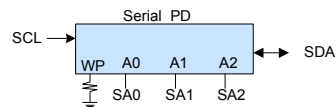
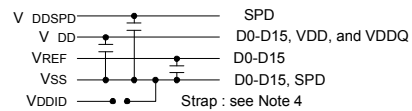
Functional Block Diagram

(1GB – 2 Ranks, 64Mx8 DDR2 SDRAMs)



BA0-BA1 — BA0-BA1 : SDRAMs D0-D15
 A0-A13 — A0-A13 : SDRAMs D0-D15
 RAS — RAS : SDRAMs D0-D15
 CAS — CAS : SDRAMs D0-D15
 WE — WE : SDRAMs D0-D15
 CKE0 — CKE : SDRAMs D0-D7
 CKE1 — CKE : SDRAMs D8-D15
 ODT0 — ODT : SDRAMs D0-D7
 ODT1 — ODT : SDRAMs D8-D15

- Notes :
1. DQ-to-I/O wiring may be changed within a byte.
 2. DQ/DQS/DM/CKE/CS relationships are maintained as shown.
 3. DQ/DQS/DQS resistors are 22 Ohms +/- 5%
 4. BAx, Ax, RAS, CAS, WE resistors are 5.1 Ohms +/- 5%
 5. Address and control resistors are 22 Ohms +/- 5%



Serial Presence Detect (256MB – 1 Rank, 32Mx16 DDR2 SDRAMs) (Part 1 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hex.)			Note
		-37B	-3C	-25D	-37B	-3C	-25D	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	13			0D			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Ranks, Package, and Height	1 rank, Height=30mm			60			
6	Data Width of Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at CL=5	3.75ns	3ns	2.5ns	3D	30	25	
10	DDR2 SDRAM Device Access Time (t _{ac}) from Clock at CL=5	0.5ns	0.45ns	0.40ns	50	45	40	
11	DIMM Configuration Type	Non-Parity			00			
12	Refresh Rate/Type	7.8µs/self			82			
13	Primary DDR2 SDRAM Width	X16			10			
14	Error Checking DDR2 SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3,4,5		4,5,6	38	70		
19	DIMM Mechanical Characteristics	<3.80mm			01			
20	DDR2 SDRAM DIMM Type Information	SODIMM (67.6mm)			04			
21	DDR2 SDRAM Module Attributes	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR			07			
23	Minimum Clock Cycle at CL=4	3.75ns		3ns	3D	30		
24	Maximum Data Access Time from Clock at CL=4	0.5ns		0.45ns	50	45		
25	Minimum Clock Cycle Time at CL=3	5ns		3.75ns	50	3D		
26	Maximum Data Access Time from Clock at CL=3	0.6ns		0.5ns	60	50		
27	Minimum Row Precharge Time (t _{RP})	15ns			3C			
28	Minimum Row Active to Row Active delay (t _{RRD})	10ns			28			
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t _{RCD})	15ns			3C			
30	Minimum Active to Precharge Time (t _{RAS})	45ns			2D			
31	Module Rank Density	256MB			40			
32	Address and Command Setup Time Before Clock (t _{IS})	0.25ns	0.2ns	0.17ns	25	20	17	
33	Address and Command Hold Time After Clock (t _{IH})	0.37ns	0.27ns	0.25ns	37	27	25	
34	Data Input Setup Time Before Clock (t _{DS})	0.10ns		0.05ns	10		05	
35	Data Input Hold Time After Clock (t _{DH})	0.22ns	0.17ns	0.12ns	22	17	12	
36	Write Recovery Time (t _{WR})	15ns			3C			
37	Internal Write to Read Command delay (t _{WTR})	7.5ns			1E			
38	Internal Read to Precharge delay (t _{RTP})	7.5ns			1E			
39	Reserved	Undefined			00			
40	Extension of Byte 41 t _{RC} and Byte 42 t _{RFC}	00: The number below a decimal point of t _{RC} and t _{RFC} are 0, t _{RFC} is less than 256ns.			00			

Serial Presence Detect (256MB – 1 Rank, 32Mx16 DDR2 SDRAMs) (Part 2 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hex.)			Note
		-37B	-3C	-25D	-37B	-3C	-25D	
41	Minimum Core Cycle Time (t_{RC})	60ns			3C			
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	105ns			69			
43	Maximum Clock Cycle Time (t_{CK})	8.0ns			80			
44	Max. DQS-DQ Skew Factor (tQHS)	0.30ns	0.24ns	0.20ns	1E	18	14	
45	Read Data Hold Skew Factor (tQHS)	0.40ns	0.34ns	0.30ns	28	22	1E	
46	PLL Relock Time	N/A			00			
47	Tcasemax DT4R4W Delta	95°C 0°C	95°C 1.2°C	95°C 0°C	50	53	50	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	59°C/W			76			
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	7.85°C	8.41°C	9.42°C	47	4F	5F	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	4.48°C	5.61°C	5.72°C	2D	39	3A	
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	0.795°C			35			
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	4.82°C	5.61°C	6.73°C	21	26	2D	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	3.14°C	3.7°C	4.37°C	3F	4A	58	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	1.01°C			29			
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	12.33°C	14.57°C	17.38°C	3E	4A	58	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	16.82°C	17.94°C	19.62°C	22	24	28	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	17.94°C	19.06°C		24	27		
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00			00			
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00			00			
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00			00			
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00			00			
62	SPD Reversion	1.2			12			
63	Checksum for Byte 0-62	Checksum Data			08	FC	FB	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-91	Module Part number	Module Part Number in ASCII			--			1
92-255	Reserved	undefined			--			

Note:

- Module part number:
 NT256T64UH4B0FN-37B → 4E543235365436345548344230464E2D333742
 NT256T64UH4B0FN-3C → 4E543235365436345548344230464E2D334320
 NT256T64UH4B0FN-25D → 4E543235365436345548344230464E2D323544

Serial Presence Detect (512MB – 2 Ranks, 32Mx16 DDR2 SDRAMs) (Part 1 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hex.)			Note
		-37B	-3C	-25D	-37B	-3C	-25D	
0	Number of Serial PD Bytes Written during Production	128			80			
1	Total Number of Bytes in Serial PD device	256			08			
2	Fundamental Memory Type	DDR2-SDRAM			08			
3	Number of Row Addresses on Assembly	13			0D			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of DIMM Ranks, Package, and Height	2 ranks, Height=30mm			61			
6	Data Width of Assembly	X64			40			
7	Reserved	Undefined			00			
8	Voltage Interface Level of this Assembly	SSTL_1.8V			05			
9	DDR2 SDRAM Device Cycle Time at CL=5	3.75ns	3ns	2.5ns	3D	30	25	
10	DDR2 SDRAM Device Access Time (t _{ac}) from Clock at CL=5	0.5ns	0.45ns	0.40ns	50	45	40	
11	DIMM Configuration Type	Non-Parity			00			
12	Refresh Rate/Type	7.8μs/self			82			
13	Primary DDR2 SDRAM Width	X16			10			
14	Error Checking DDR2 SDRAM Device Width	N/A			00			
15	Reserved	Undefined			00			
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8			0C			
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4			04			
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3,4,5	4,5,6		38	70		
19	DIMM Mechanical Characteristics	<3.80mm			01			
20	DDR2 SDRAM DIMM Type Information	SODIMM (67.6mm)			04			
21	DDR2 SDRAM Module Attributes	Normal DIMM			00			
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR			07			
23	Minimum Clock Cycle at CL=4	3.75ns		3ns	3D	30		
24	Maximum Data Access Time from Clock at CL=4	0.5ns		0.45ns	50	45		
25	Minimum Clock Cycle Time at CL=3	5ns		3.75ns	50	3D		
26	Maximum Data Access Time from Clock at CL=3	0.6ns		0.5ns	60	50		
27	Minimum Row Precharge Time (t _{RP})	15ns			3C			
28	Minimum Row Active to Row Active delay (t _{RRD})	10ns			28			
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t _{RCD})	15ns			3C			
30	Minimum Active to Precharge Time (t _{RAS})	45ns			2D			
31	Module Rank Density	256MB			40			
32	Address and Command Setup Time Before Clock (t _{IS})	0.25ns	0.2ns	0.17ns	25	20	17	
33	Address and Command Hold Time After Clock (t _{IH})	0.37ns	0.27ns	0.25ns	37	27	25	
34	Data Input Setup Time Before Clock (t _{DS})	0.10ns		0.05ns	10		05	
35	Data Input Hold Time After Clock (t _{DH})	0.22ns	0.17ns	0.12ns	22	17	12	
36	Write Recovery Time (t _{WR})	15ns			3C			
37	Internal Write to Read Command delay (t _{WTR})	7.5ns			1E			
38	Internal Read to Precharge delay (t _{RTP})	7.5ns			1E			
39	Reserved	Undefined			00			
40	Extension of Byte 41 t _{RC} and Byte 42 t _{RFC}	00: The number below a decimal point of t _{RC} and t _{RFC} are 0, t _{RFC} is less than 256ns.			00			

Serial Presence Detect (512MB – 2 Ranks, 32Mx16 DDR2 SDRAMs) (Part 2 of 2)

Byte	Description	SPD Entry Value			Serial PD Data Entry (Hex.)			Note
		-37B	-3C	-25D	-37B	-3C	-25D	
41	Minimum Core Cycle Time (t_{RC})	60ns			3C			
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	105ns			69			
43	Maximum Clock Cycle Time (t_{CK})	8.0ns			80			
44	Max. DQS-DQ Skew Factor (tQHS)	0.30ns	0.24ns	0.20ns	1E	18	14	
45	Read Data Hold Skew Factor (tQHS)	0.40ns	0.34ns	0.30ns	28	22	1E	
46	PLL Relock Time	N/A			00			
47	Tcasemax DT4R4W Delta	95°C 0°C	95°C 1.2°C	95°C 0°C	50	53	50	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	59°C/W			76			
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	7.85°C	8.41°C	9.42°C	47	4F	5F	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	4.48°C	5.61°C	5.72°C	2D	39	3A	
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	0.795°C			35			
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	4.82°C	5.61°C	6.73°C	21	26	2D	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	3.14°C	3.7°C	4.37°C	3F	4A	58	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	1.01°C			29			
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	12.33°C	14.57°C	17.38°C	3E	4A	58	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	16.82°C	17.94°C	19.62°C	22	24	28	
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	17.94°C	19.06°C		24	27		
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00			00			
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00			00			
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00			00			
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00			00			
62	SPD Reversion	1.2			12			
63	Checksum for Byte 0-62	Checksum Data			09	FD	FC	
64-71	Manufacturer's JEDEC ID Code	NANYA			7F7F7F0B00000000			
72	Module Manufacturing Location	Manufacturing code			--			
73-91	Module Part number	Module Part Number in ASCII			--			1
92-255	Reserved	undefined			--			

Note:

- Module part number:
 NT512T64UH8B0FN-37B → 4E543531325436345548384230464E2D333742
 NT512T64UH8B0FN-3C → 4E543531325436345548384230464E2D334320
 NT512T64UH8B0FN-25D → 4E543531325436345548384230464E2D323544

Serial Presence Detect (1GB – 2 Ranks, 64Mx8 DDR2 SDRAMs) (Part 1 of 2)

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note
		-37B	-3C	-25D	-25C	-37B	-3C	-25D	-25C	
0	Number of Serial PD Bytes Written during Production	128				80				
1	Total Number of Bytes in Serial PD device	256				08				
2	Fundamental Memory Type	DDR2-SDRAM				08				
3	Number of Row Addresses on Assembly	14				0E				
4	Number of Column Addresses on Assembly	10				0A				
5	Number of DIMM Ranks, Package, and Height	2 ranks, Height=30mm				61				
6	Data Width of Assembly	X64				40				
7	Reserved	Undefined				00				
8	Voltage Interface Level of this Assembly	SSTL_1.8V				05				
9	DDR2 SDRAM Device Cycle Time at CL=5	3.75ns	3ns	2.5ns		3D	30	25		
10	DDR2 SDRAM Device Access Time (t _{ac}) from Clock at CL=5	0.5ns	0.45ns	0.40ns		50	45	40		
11	DIMM Configuration Type	Non-Parity				00				
12	Refresh Rate/Type	7.8μs/self				82				
13	Primary DDR2 SDRAM Width	X8				08				
14	Error Checking DDR2 SDRAM Device Width	N/A				00				
15	Reserved	Undefined				00				
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8				0C				
17	DDR2 SDRAM Device Attributes: Number of Device Banks	4				04				
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3,4,5		4,5,6	3,4,5	38	70	38		
19	DIMM Mechanical Characteristics	<3.80mm				01				
20	DDR2 SDRAM DIMM Type Information	SODIMM (67.6mm)				04				
21	DDR2 SDRAM Module Attributes	Normal DIMM				00				
22	DDR2 SDRAM Device Attributes: General	Support weak driver, 50Ω ODT, and PASR				07				
23	Minimum Clock Cycle at CL=4	3.75ns		3ns	3.75ns	3D	30	3D		
24	Maximum Data Access Time from Clock at CL=4	0.5ns		0.45ns	0.5ns	50	45	50		
25	Minimum Clock Cycle Time at CL=3	5ns		3.75ns	5ns	50	3D	50		
26	Maximum Data Access Time from Clock at CL=3	0.6ns		0.5ns	0.6ns	60	50	60		
27	Minimum Row Precharge Time (t _{RP})	15ns			12.5ns	3C			32	
28	Minimum Row Active to Row Active delay (t _{R RD})	7.5ns				1E				
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t _{R CD})	15ns			12.5ns	3C			32	
30	Minimum Active to Precharge Time (t _{R AS})	45ns				2D				
31	Module Rank Density	512MB				80				
32	Address and Command Setup Time Before Clock (t _{IS})	0.25ns	0.2ns	0.17ns		25	20	17		
33	Address and Command Hold Time After Clock (t _{IH})	0.37ns	0.27ns	0.25ns		37	27	25		
34	Data Input Setup Time Before Clock (t _{DS})	0.10ns	0.10ns	0.05ns		10	10	05		
35	Data Input Hold Time After Clock (t _{DH})	0.22ns	0.17ns	0.12ns		22	17	12		
36	Write Recovery Time (t _{WR})	15ns				3C				
37	Internal Write to Read Command delay (t _{WTR})	7.5ns				1E				
38	Internal Read to Precharge delay (t _{RTP})	7.5ns				1E				
39	Reserved	Undefined				00				
40	Extension of Byte 41 t _{RC} and Byte 42 t _{RFC}	00: The number below a decimal point of t _{RC} and t _{RFC} are 0, t _{RFC} is less than 256ns. 30: The number below a decimal point of t _{RC} is 5, t _{RFC} is less than 256ns.				00			30	

Serial Presence Detect (1GBB – 2 Ranks, 64Mx8 DDR2 SDRAMs) (Part 2 of 2)

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note	
		-37B	-3C	-25D	-25C	-37B	-3C	-25D	-25C		
41	Minimum Core Cycle Time (t_{RC})	60ns		57.5ns		3C		39			
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	105ns				69					
43	Maximum Clock Cycle Time (t_{CK})	8.0ns				80					
44	Max. DQS-DQ Skew Factor (tQHS)	0.30ns	0.24ns	0.20ns		1E	18	14			
45	Read Data Hold Skew Factor (tQHS)	0.40ns	0.34ns	0.30ns		28	22	1E			
46	PLL Relock Time	N/A				00					
47	Tcasemax DT4R4W Delta	95°C 0°C	95°C 1.2°C	95°C 0°C		50	53	50			
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM)	61°C/W				7A					
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	8.11°C	8.69°C	9.74°C		4B	53	63			
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	4.64°C	5.8°C	5.91°C		2F	3A	3C			
51	DRAM Case Temperature Rise from Ambient due to precharge Power-Down (DT2P)	0.81°C				37					
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	4.98°C	5.8°C	6.95°C		22	27	2F			
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3P fast)	3.25°C	3.82°C	4.52°C		41	4D	5B			
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3P slow)	1.04°C				2A					
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	12.75°C	15.07°C	17.96°C		40	4C	5C			
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	17.39°C	18.54°C	20.28°C		23	26	29			
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	18.54°C	19.7°C		26	28					
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00				00					
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00				00					
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00				00					
61	Resister Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00				00					
62	SPD Reversion	1.2				12					
63	Checksum for Byte 0-62	Checksum Data				4D	41	43	5F		
64-71	Manufacturer's JEDEC ID Code	NANYA				7F7F7F0B00000000					
72	Module Manufacturing Location	Manufacturing code				--					
73-91	Module Part number	Module Part Number in ASCII				--				1	
92-255	Reserved	undefined				--					

Note:

- Module part number:
 NT1GT64U8HB0BN-37B → 4E5431475436345538484230424E2D33374220
 NT1GT64U8HB0BN-3C → 4E5431475436345538484230424E2D33432020
 NT1GT64U8HB0BN-25D → 4E5431475436345538484230424E2D32354420
 NT1GT64U8HB0BN-25C → 4E5431475436345538484230424E2D32354320

Environmental Requirements

Symbol	Parameter	Rating	Units
T _{OPR}	Operating Temperature (ambient)	0 to 65	°C
H _{OPR}	Operating Humidity (relative)	10 to 90	%
T _{STG}	Storage Temperature	-50 to 100	°C
H _{STG}	Storage Humidity (without condensation)	5 to 95	%
	Barometric pressure (operating & storage) up to 9850ft.	105 to 69	kPa

Note: Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
V _{DD}	Voltage on VDD pins relative to V _{SS}	-1.0 to +2.3	V
V _{DDQ}	Voltage on VDDQ pins relative to V _{SS}	-0.5 to +2.3	V
V _{DDL}	Voltage on VDDL pins relative to V _{SS}	-0.5 to +2.3	V
V _{IN} , V _{OUT}	Voltage on I/O pins relative to V _{SS}	-0.5 to +2.3	V
T _{STG}	Storage Temperature (Plastic)	-55 to +100	°C

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Storage temperature is the case surface temperature on the center/top side of the DRAM.

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T _{CASE}	Operating Temperature (Ambient)	0 to 95	°C	1

Note:

- Case temperature is measured at top and center side of any DRAMs.
- t_{CASE} > 85 °C → t_{REFI} = 3.9 μs

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V _{DD}	Supply Voltage	1.7	1.9	V	1
V _{DDL}	DLL Supply Voltage	1.7	1.9	V	1
V _{DDQ}	Output Supply Voltage	1.7	1.9	V	1
V _{SS} , V _{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V _{REF}	Input Reference Voltage	0.49V _{DDQ}	0.51V _{DDQ}	V	1, 2
V _{TT}	Termination Voltage	V _{REF} - 0.04	V _{REF} + 0.04	V	3

Note:

- There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However, VDDQ must be less than or equal to VDD under all conditions.
- VREF is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
- VTT of transmitting device must track VREF of receiving device.

ODT DC Electrical Characteristics

Parameter/Condition	Symbol	Min.	Nom.	Max.	Units	Note
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75ohm	Rtt1(eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150ohm	Rtt2(eff)	120	150	180	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50ohm	Rtt3(eff)	40	50	60	ohm	1
Deviation of V_M with respect to $V_{DDQ}/2$	Delta VM	-6		+6	%	1

Note1: Test condition for Rtt measurements.

Input AC/DC logic level

Symbol	Parameter	PC2-4300		PC2-5300		PC2-6400		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V _{IH} (AC)	Input High (Logic1) Voltage	V _{REF} + 0.250	-	V _{REF} + 0.200	-	V _{REF} + 0.200	-	V
V _{IL} (AC)	Input Low (Logic0) Voltage	-	V _{REF} - 0.250	-	V _{REF} - 0.200	-	V _{REF} - 0.200	V
V _{IH} (DC)	Input High (Logic1) Voltage	V _{REF} + 0.125	V _{DDQ} + 0.3	V _{REF} + 0.125	V _{DDQ} + 0.3	V _{REF} + 0.125	V _{DDQ} + 0.3	V
V _{IL} (DC)	Input Low (Logic0) Voltage	-0.3	V _{REF} - 0.125	-0.3	V _{REF} - 0.125	-0.3	V _{REF} - 0.125	V

Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ (256MB, 1 Rank, 32Mx16 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-4300 (-37B)	PC2-5300 (-3C)	PC2-6400 (-25D)	Unit
IDD0	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	374	396	440	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC} = t_{RC(MIN)}$; CL= 4; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$; address and control inputs changing once per clock cycle	418	440	506	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$	31	31	31	mA
IDD2Q	Precharge quiet standby current	154	176	198	mA
IDD2N	Idle Standby Current: $CS \geq V_{IH(MIN)}$; all banks idle; $CKE \geq V_{IH(MIN)}$; $t_{CK} = t_{CK(MIN)}$; address and control inputs changing once per clock cycle	176	202	224	mA
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$; MRS(12)=0	123	145	172	mA
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$; MRS(12)=1	40	40	40	mA
IDD3N	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH(MIN)}$; $CKE \geq V_{IH(MIN)}$; $t_{RC} = t_{RAS(MAX)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	189	220	264	mA
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 4; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$	594	682	792	mA
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL= 4; $t_{CK} = t_{CK(MIN)}$	638	748	880	mA
IDD5B	Burst Refresh Current: $t_{RFC} = t_{RFC(MIN)}$	660	748	836	mA
IDD5D	Distributed Refresh Current: $t_{RFC} = t_{REF}$	40	40	40	mA
IDD6	Self-Refresh Current: $CKE \leq 0.2\text{V}$	31	31	31	mA
IDD7	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC(min)}$; $I_{OUT} = 0\text{mA}$.	1144	1166	1210	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ (512MB, 2 Ranks, 32Mx16 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-4300 (-37B)	PC2-5300 (-3C)	PC2-6400 (-25D)	Unit
IDD0	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	563	616	704	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC} = t_{RC(MIN)}$; $CL = 4$; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$; address and control inputs changing once per clock cycle	607	660	770	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$	62	62	62	mA
IDD2Q	Precharge quiet standby current	308	352	396	mA
IDD2N	Idle Standby Current: $CS \geq V_{IH(MIN)}$; all banks idle; $CKE \geq V_{IH(MIN)}$; $t_{CK} = t_{CK(MIN)}$; address and control inputs changing once per clock cycle	352	405	449	mA
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$; $MRS(12)=0$	246	290	343	mA
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$; $MRS(12)=1$	79	79	79	mA
IDD3N	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH(MIN)}$; $CKE \geq V_{IH(MIN)}$; $t_{RC} = t_{RAS(MAX)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	378	440	528	mA
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 4$; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$	783	902	1056	mA
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL = 4$; $t_{CK} = t_{CK(MIN)}$	827	968	1144	mA
IDD5B	Burst Refresh Current: $t_{RC} = t_{RFC(MIN)}$	849	968	1100	mA
IDD5D	Distributed Refresh Current: $t_{RFC} = t_{REF}$	79	79	79	mA
IDD6	Self-Refresh Current: $CKE \leq 0.2\text{V}$	56	56	56	mA
IDD7	Operating Current: four bank; four bank interleaving with $BL = 4$, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC(min)}$; $I_{OUT} = 0\text{mA}$.	1333	1386	1474	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ (1GB, 2 Banks, 64Mx8 DDR2 SDRAMs)

Symbol	Parameter/Condition	PC2-4300 (-37B)	PC2-5300 (-3C)	PC2-6400 (-25D)	PC2-6400 (-25C)	Unit
IDD0	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC(MIN)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	994	1100	1250	1276	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC} = t_{RC(MIN)}$; $CL = 4$; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$; address and control inputs changing once per clock cycle	1082	1232	1408	1452	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$	123	123	123	123	mA
IDD2Q	Precharge quiet standby current	616	704	792	792	mA
IDD2N	Idle Standby Current: $CS \geq V_{IH(MIN)}$; all banks idle; $CKE \geq V_{IH(MIN)}$; $t_{CK} = t_{CK(MIN)}$; address and control inputs changing once per clock cycle	704	810	898	898	mA
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$; $MRS(12)=0$	493	581	686	686	mA
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$; $t_{CK} = t_{CK(MIN)}$; $MRS(12)=1$	158	158	158	158	mA
IDD3N	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH(MIN)}$; $CKE \geq V_{IH(MIN)}$; $t_{RC} = t_{RAS(MAX)}$; $t_{CK} = t_{CK(MIN)}$; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	757	880	1056	1056	mA
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 4$; $t_{CK} = t_{CK(MIN)}$; $I_{OUT} = 0\text{mA}$	1346	1628	1892	1892	mA
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL = 4$; $t_{CK} = t_{CK(MIN)}$	1346	1584	1892	1892	mA
IDD5B	Burst Refresh Current: $t_{RC} = t_{RFC(MIN)}$	1698	1936	2200	2200	mA
IDD5D	Distributed Refresh Current: $t_{RFC} = t_{REF}$	158	158	158	158	mA
IDD6	Self-Refresh Current: $CKE \leq 0.2\text{V}$	123	123	123	123	mA
IDD7	Operating Current: four bank; four bank interleaving with $BL = 4$, address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC(MIN)}$; $I_{OUT} = 0\text{mA}$.	1786	1892	2024	2024	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

($T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$; $V_{DDQ} = 1.8\text{V} \pm 0.1\text{V}$; $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	-37B		-3C		-25C/-25D		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AC}	DQ output access time from CK/ $\overline{\text{CK}}$	-0.5	+0.5	-0.48	+0.52	-0.40	+0.40	ns	
$t_{DQ\text{SCK}}$	DQS output access time from CK/ $\overline{\text{CK}}$	-0.45	+0.45	-0.4	+0.4	-0.35	+0.35	ns	
t_{CH}	CK high-level width	0.45	0.55	0.48	0.52	0.48	0.52	t_{CK}	
t_{CL}	CK low-level width	0.45	0.55	0.48	0.52	0.48	0.52	t_{CK}	
t_{HP}	Minimum half clk period for any given cycle; defined by clk high (t_{CH}) or clk low (t_{CL}) time	t_{CH} or t_{CL}	-	t_{CH} or t_{CL}	-	t_{CH} or t_{CL}	-	t_{CK}	
t_{CK}	Clock Cycle Time	3.75	8	3	8	2.5	8	ns	
t_{DH}	DQ and DM input hold time	225	-	175	-	125	-	ps	
t_{DS}	DQ and DM input setup time	100	-	100	-	50	-	ps	
t_{IPW}	Input pulse width	0.6	-	0.6	-	0.6	-	t_{CK}	
t_{DIPW}	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	t_{CK}	
t_{HZ}	Data-out high-impedance time from CK/ $\overline{\text{CK}}$	-	$t_{AC\text{ max}}$	-	$t_{AC\text{ max}}$	-	$t_{AC\text{ max}}$	ns	
$t_{LZ(DQ)}$	Data-out low-impedance time from CK/ $\overline{\text{CK}}$	$2t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$2t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$2t_{AC\text{ min}}$	$t_{AC\text{ max}}$	ns	
$t_{LZ(DQS)}$	DQS low-impedance time from CK/ $\overline{\text{CK}}$	$t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$t_{AC\text{ min}}$	$t_{AC\text{ max}}$	ns	
t_{DQSQ}	DQS-DQ skew (DQS & associated DQ signals)	-	0.30	-	0.24	-	0.20	ns	
t_{QHS}	Data hold Skew Factor	-	0.4	-	0.34	-	0.30	ns	
t_{QH}	Data output hold time from DQS	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	ns	
t_{DQSS}	Write command to 1st DQS latching transition	-0.25	0.25	-0.25	0.25	-0.25	0.25	t_{CK}	
t_{DQSH}	DQS input high pulse width	0.35	-	0.35	-	0.35	-	t_{CK}	
t_{DQSL}	DQS input low pulse width	0.35	-	0.35	-	0.35	-	t_{CK}	
t_{DSS}	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	t_{CK}	
t_{DSH}	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	t_{CK}	
t_{MRD}	Mode register set command cycle time	2	-	2	-	2	-	t_{CK}	
t_{WPST}	Write postamble	0.40	0.60	0.40	0.60	0.40	0.60	t_{CK}	
t_{WPRE}	Write preamble	0.35	-	0.35	-	0.35	-	t_{CK}	
t_{IH}	Address and control input hold time	0.375	-	0.275	-	0.250	-	ns	
t_{IS}	Address and control input setup time	0.25	-	0.2	-	0.175	-	ns	
t_{RPRE}	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
t_{RPST}	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
t_{Delay}	Minimum time clocks remains ON after CKE asynchronously drops Low	$t_{IS} + t_{CK} + t_{IH}$	-	$t_{IS} + t_{CK} + t_{IH}$	-	$t_{IS} + t_{CK} + t_{IH}$	-	ns	
t_{RFC}	Refresh to active/Refresh command time	105		105		105		ns	
t_{REFI}	Average Periodic Refresh Interval (85°C < $T_{CASE} \leq 95^{\circ}\text{C}$)	3.9		3.9		3.9		μs	
	Average Periodic Refresh Interval (0°C $\leq T_{CASE} \leq 85^{\circ}\text{C}$)	7.8		7.8		7.8		μs	

AC Timing Specifications for DDR2 SDRAM Devices Used on Module

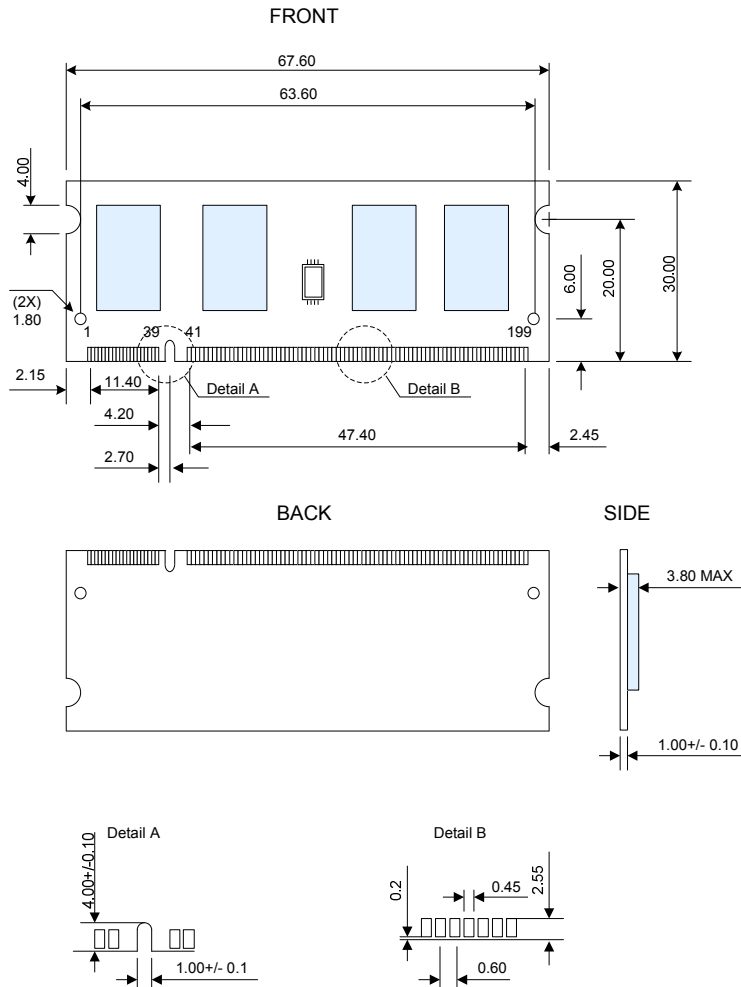
(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-37B		-3C		-25C/-25D		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{RRD}	Active bank A to Active bank B command	7.5	-	7.5	-	7.5	-	ns	
t _{CCD}	CAS to CAS	2	-	2	-	2	-	t _{CK}	
t _{WR}	Write recovery time	15	-	15	-	15	-	ns	
WR	Write recovery time with Auto-Precharge	t _{WR} /t _{CK}		t _{WR} /t _{CK}		t _{WR} /t _{CK}		ns	
t _{DAL}	Auto precharge write recovery + precharge time	WR + t _{RP}	-	WR + t _{RP}	-	WR + t _{RP}	-	t _{CK}	
t _{WTR}	Internal write to read command delay	7.5	-	7.5	-	7.5	-	ns	
t _{RTP}	Internal read to precharge command delay	7.5	-	7.5	-	7.5	-	ns	
t _{XSNR}	Exit self refresh to a Non-read command	t _{RFC} + 10	-	t _{RFC} + 10	-	t _{RFC} + 10	-	ns	
t _{XSRD}	Exit self refresh to a Read command	200	-	200	-	200	-	t _{CK}	
t _{XP}	Exit precharge power down to any Non- read command	2	-	2	-	2	-	t _{CK}	
t _{XARD}	Exit active power down to read command	2	-	2	-	2	-	t _{CK}	
t _{XARDS}	Exit active power down to read command	6-AL	-	7-AL	-	8-AL	-	t _{CK}	
t _{CKE}	CKE minimum pulse width	3	-	3	-	3	-	t _{CK}	
t _{OIT}	OCD drive mode output delay	0	12	0	12	0	12	ns	
ODT									
t _{AOND}	ODT turn-on delay	2	2	2	2	2	2	t _{CK}	
t _{AON}	ODT turn-on	t _{AC} (min)	t _{AC} (max) + 1	t _{AC} (min)	t _{AC} (max) + 0.7	t _{AC} (min)	t _{AC} (max) + 0.7	ns	
t _{AONPD}	ODT turn-on (Power down mode)	t _{AC} (min) + 2	2t _{CK} + t _{AC} (max) + 1	t _{AC} (min) + 2	2t _{CK} + t _{AC} (max) + 1	t _{AC} (min) + 2	2t _{CK} + t _{AC} (max) + 1	ns	
t _{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	t _{CK}	
t _{AOF}	ODT turn-off	t _{AC} (min)	t _{AC} (max) + 0.6	t _{AC} (min)	t _{AC} (max) + 0.6	t _{AC} (min)	t _{AC} (max) + 0.6	ns	
t _{AOFPD}	ODT turn-off (Power down mode)	t _{AC} (min) + 2	2.5t _{CK} + t _{AC} (max) + 1	t _{AC} (min) + 2	2.5t _{CK} + t _{AC} (max) + 1	t _{AC} (min) + 2	2.5t _{CK} + t _{AC} (max) + 1	ns	
t _{ANPD}	ODT to power down entry latency	3	-	3	-	3	-	t _{CK}	
t _{AXPD}	ODT power down exit latency	8	-	8	-	8	-	t _{CK}	

Speed Grade Definition										
Symbol	Parameter	-37B		-3C		-25D		-25C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RAS}	Row Active Time	45	70000	45	70000	45	70000	45	70000	ns
t _{RCD}	RAS to CAS delay	15	-	15	-	15	-	12.5	-	ns
t _{RC}	Row Cycle Time	60	-	60	-	60	-	57.5	-	ns
t _{RP}	Row Precharge Time	15	-	15	-	15	-	12.5	-	ns

Package Dimensions

(256MB, 1 Rank, 32Mx16 DDR2 SDRAMs)



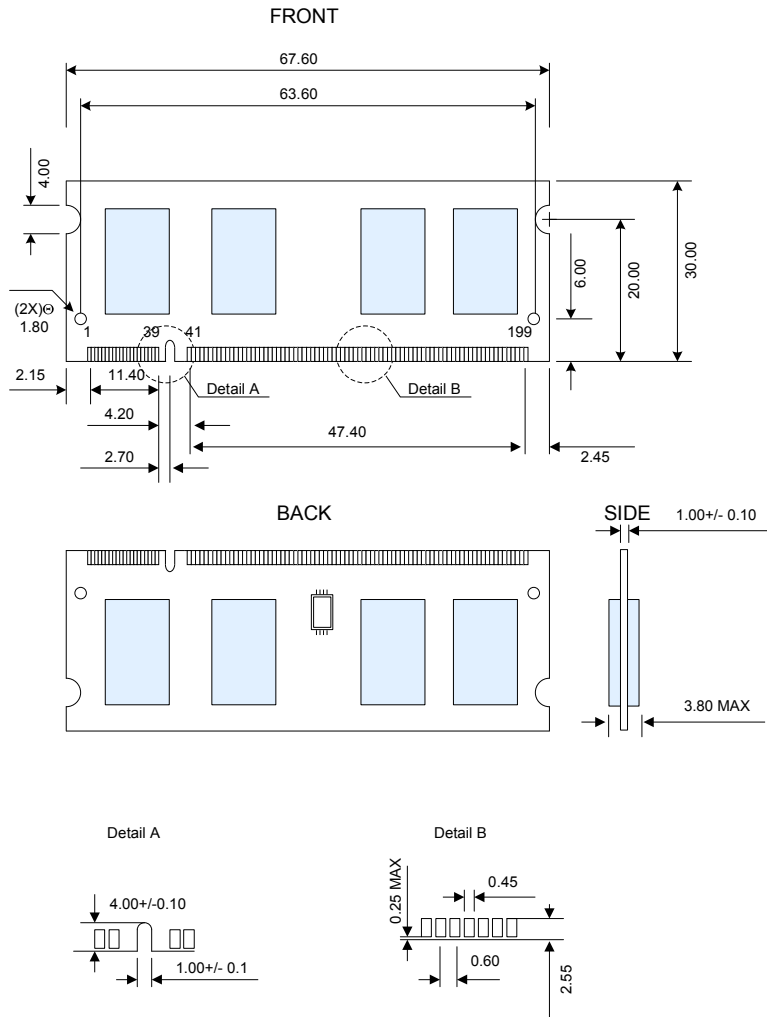
Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

Package Dimensions

(512MB – 2 Ranks, 32Mx16 DDR2 SDRAMs)



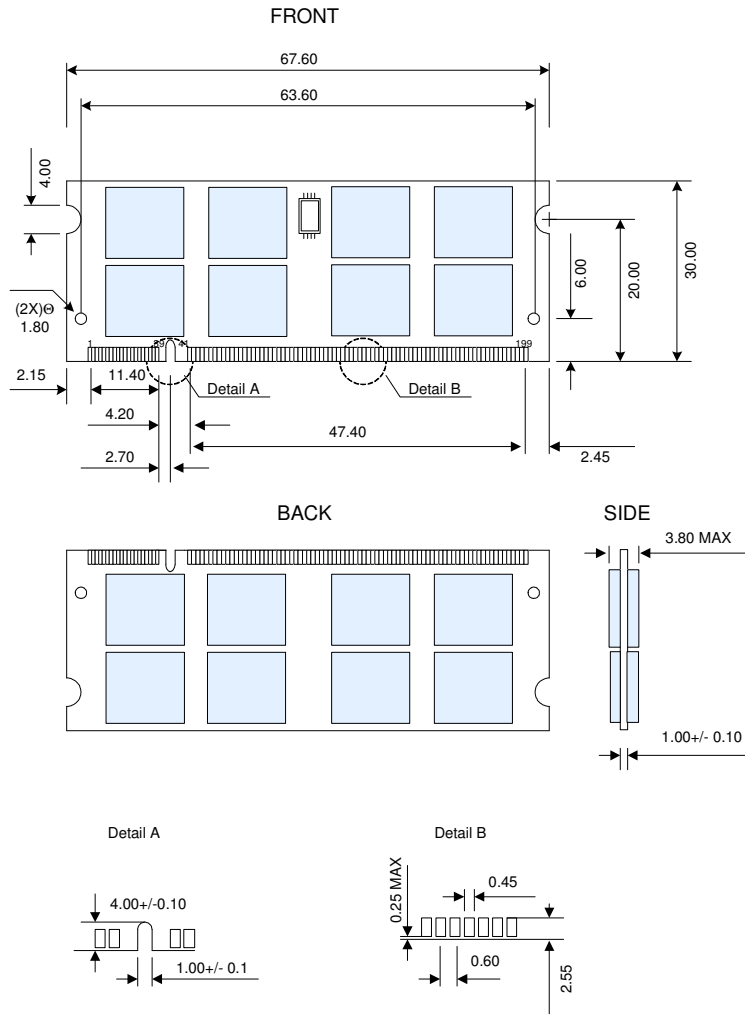
Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

Package Dimensions

(1GB – 2 Ranks, 32Mx8 DDR2 SDRAMs)



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Note: Device position and scale are only for reference.

Revision Log

Rev	Date	Modification
0.1	01/2006	Preliminary Release
0.2	03/2006	Add PC2-6400 (DDR2-800MHz)
1.0	06/2006	Official Release
1.1	07/2007	Modified 256MB/512MB DDR2-800 item
1.2	08/2007	Add Halogen free P/N

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