

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN  
 NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS  
 512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64  
 PC2-4200 / PC2-5300 / PC2-6400  
 Unbuffered DDR2 SO-DIMM**



Based on DDR2-533/667/800 64Mx16 (512MB)/64Mx16 (1GB)/128Mx8 (2GB) SDRAM D-Die

## Features

• Performance:

Speed Sort	PC2-4200	PC2-5300	PC2-6400	PC2-6400	Unit
	-37B	-3C	-AD	-AC	
DIMM CAS Latency	4	5	6	5	
fck – Clock Frequency	266	333	400	400	MHz
tck – Clock Cycle	3.75	3	2.5	2.5	ns
fDQ – DQ Burst Frequency	533	667	800	800	Mbps

- 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
- 512MB: 64Mx64 Unbuffered DDR2 SO-DIMM based on 64Mx16 DDR2 SDRAM D Die devices.
- 1GB: 128Mx64 Unbuffered DDR2 SO-DIMM based on 64Mx16 DDR2 SDRAM D Die devices.
- 2GB: 256Mx64 Unbuffered DDR2 SO-DIMM based on 128Mx8 DDR2 SDRAM D Die devices.
- Intended for 266MHz, 333MHz, and 400MHz applications
- Inputs and outputs are SSTL-18 compatible
- $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- DRAM DLL aligns DQ and DQS transitions with clock transitions.
- Address and control signals are fully synchronous to positive clock edge
- Auto Refresh (CBR) and Self Refresh Modes
- Automatic and controlled precharge commands
- Programmable Operation:
  - DIMM CAS Latency: 3, 4, 5 (-37B/-3C/-AC)
  - DIMM CAS Latency: 4, 5, 6 (-AD)
  - Burst Type: Sequential or Interleave
  - Burst Length: 4, 8
  - Operation: Burst Read and Write
- 13/10/1 Addressing (512MB)
- 13/10/2 Addressing (1GB)
- 14/10/2 Addressing (2GB)
- 7.8  $\mu$ s Max. Average Periodic Refresh Interval
- Serial Presence Detect
- Gold contacts
- 512MB/1GB module's SDRAMs are 84-ball BGA Package
- 2GB module's SDRAMs are 60-ball BGA Package
- RoHS compliance
- Halogen free product:
  - NT512T64UH4D0FS
  - NT1GT64UH8D0FS
  - NT2GT64U8HD0BS

## Description

NT512T64UH4D0FN, NT512T64UH4D0FS, NT1GT64UH8D0FN, NT1GT64UH8D0FS, NT2GT64U8HD0BN and NT2GT64U8HD0BS are unbuffered 200-Pin Double Data Rate 2 (DDR2) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as one rank (512MB)/two ranks (1GB/2GB) of 64Mx64 (512MB)/128Mx64 (1GB)/256Mx64 (2GB) high-speed memory array.

NT512T64UH4D0FN and NT512T64UH4D0FS use four 64Mx16 84-ball BGA packaged devices; NT1GT64UH8D0FN and NT1GT64UH8D0FS use eight 64Mx16 84-ball BGA packaged devices; NT2GT64U8HD0BN and NT2GT64U8HD0BS use sixteen 128Mx8 60-ball BGA packaged devices. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All NANYA DDR2 SODIMMs provide a high-performance, flexible 8-byte interface in a space-saving footprint.

The DIMM is intended for use in applications operating of 266MHz (333MHz or 400MHz) clock speeds and achieves high-speed data transfer rates of 533Mbps (667Mbps or 800Mbps). Prior to any access operation, the device CAS latency and burst/length/operation type must be programmed into the DIMM by address inputs A0-A12 (512MB/1GB)/A0-A13 (2GB) and I/O inputs BA0, BA1 and BA2 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial EEPROM using a standard IIC protocol. The first 128 bytes of SPD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

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## Ordering Information

Part Number	Speed			Organization	Power	Leads	Note
NT2GT64U8HD0BN – AC	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)	256Mx64	1.8V	Gold	
NT2GT64U8HD0BN – AD	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)				
NT2GT64U8HD0BN – 3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)				
NT2GT64U8HD0BN – 37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)				
NT2GT64U8HD0BS – AC	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)				
NT2GT64U8HD0BS – AD	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)				
NT2GT64U8HD0BS – 3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)				
NT2GT64U8HD0BS – 37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)				
NT1GT64UH8D0FN – AC	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)	128Mx64	1.8V	Gold	
NT1GT64UH8D0FN – AD	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)				
NT1GT64UH8D0FN – 3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)				
NT1GT64UH8D0FN – 37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)				
NT1GT64UH8D0FS – AC	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)				
NT1GT64UH8D0FS – AD	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)				
NT1GT64UH8D0FS – 3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)				
NT1GT64UH8D0FS – 37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)				
NT512T64UH4D0FN – AC	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)	64Mx64	1.8V	Gold	
NT512T64UH4D0FN – AD	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)				
NT512T64UH4D0FN – 3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)				
NT512T64UH4D0FN – 37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)				
NT512T64UH4D0FS – AC	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 5)				
NT512T64UH4D0FS – AD	DDR2-800	PC2-6400	400MHz (2.5ns @ CL = 6)				
NT512T64UH4D0FS – 3C	DDR2-667	PC2-5300	333MHz (3ns @ CL = 5)				
NT512T64UH4D0FS – 37B	DDR2-533	PC2-4200	266MHz (3.75ns @ CL = 4)				

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
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## Pin Description

CK0, CK1, $\overline{\text{CK0}}$ , $\overline{\text{CK1}}$	Differential Clock Inputs	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7	Bidirectional data strobes
$\overline{\text{RAS}}$	Row Address Strobe	$\overline{\text{DQS0}}$ - $\overline{\text{DQS7}}$	Differential data strobes
$\overline{\text{CAS}}$	Column Address Strobe	DM0-DM7	Input Data Masks
WE	Write Enable	V <sub>DD</sub>	Power (1.8V)
$\overline{\text{CS0}}$ , $\overline{\text{CS1}}$	Chip Selects	V <sub>REF</sub>	Ref. Voltage for SSTL_18 inputs
A0-A9 A11-A13	Row Address Inputs	V <sub>DDSPD</sub>	Serial EEPROM positive power supply
A0-A9	Column Address Inputs	V <sub>SS</sub>	Ground
A10/AP	Column Address Input/Auto-precharge	SCL	Serial Presence Detect Clock Input
BA0, BA1, BA2	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
ODT0, ODT1	Active termination control lines	SA0, SA1	Serial Presence Detect Address Inputs
NC	No Connect		

Note: CKE1,  $\overline{\text{CS1}}$  and ODT1 are for 1GB/2GB modules only.  
A13 is for 2GB modules only.

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**PC2-4200 / PC2-5300 / PC2-6400**  
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**512MB/1GB/2GB DDR2 SDRAM SODIMM Pinout**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V <sub>REF</sub>	2	V <sub>SS</sub>	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V <sub>SS</sub>	4	DQ4	53	V <sub>SS</sub>	54	V <sub>SS</sub>	103	V <sub>DD</sub>	104	V <sub>DD</sub>	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V <sub>SS</sub>	156	V <sub>SS</sub>
7	DQ1	8	V <sub>SS</sub>	57	DQ19	58	DQ23	107	BA0	108	RAS	157	DQ48	158	DQ52
9	V <sub>SS</sub>	10	DM0	59	V <sub>SS</sub>	60	V <sub>SS</sub>	109	WE	110	CS0	159	DQ49	160	DQ53
11	DQS0	12	V <sub>SS</sub>	61	DQ24	62	DQ28	111	V <sub>DD</sub>	112	V <sub>DD</sub>	161	V <sub>SS</sub>	162	V <sub>SS</sub>
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	CAS	114	ODT0	163	NC	164	CK1
15	V <sub>SS</sub>	16	DQ7	65	V <sub>SS</sub>	66	V <sub>SS</sub>	115	CS1/NC	116	A13/NC	165	V <sub>SS</sub>	166	CKT
17	DQ2	18	V <sub>SS</sub>	67	DM3	68	DQS3	117	V <sub>DD</sub>	118	V <sub>DD</sub>	167	DQS6	168	V <sub>SS</sub>
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1/NC	120	NC	169	DQS6	170	DM6
21	V <sub>SS</sub>	22	DQ13	71	V <sub>SS</sub>	72	V <sub>SS</sub>	121	V <sub>SS</sub>	122	V <sub>SS</sub>	171	V <sub>SS</sub>	172	V <sub>SS</sub>
23	DQ8	24	V <sub>SS</sub>	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V <sub>SS</sub>	28	V <sub>SS</sub>	77	V <sub>SS</sub>	78	V <sub>SS</sub>	127	V <sub>SS</sub>	128	V <sub>SS</sub>	177	V <sub>SS</sub>	178	V <sub>SS</sub>
29	DQS1	30	CK0	79	CKE0	80	CKE1/NC	129	DQS4	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	CK0	81	V <sub>DD</sub>	82	V <sub>DD</sub>	131	DQS4	132	V <sub>SS</sub>	181	DQ57	182	DQ61
33	V <sub>SS</sub>	34	V <sub>SS</sub>	83	NC	84	NC	133	V <sub>SS</sub>	134	DQ38	183	V <sub>SS</sub>	184	V <sub>SS</sub>
35	DQ10	36	DQ14	85	BA2	86	NC	135	DQ34	136	DQ39	185	DM7	186	DQS7
37	DQ11	38	DQ15	87	V <sub>DD</sub>	88	V <sub>DD</sub>	137	DQ35	138	V <sub>SS</sub>	187	V <sub>SS</sub>	188	DQS7
39	V <sub>SS</sub>	40	V <sub>SS</sub>	89	A12	90	A11	139	V <sub>SS</sub>	140	DQ44	189	DQ58	190	V <sub>SS</sub>
41	V <sub>SS</sub>	42	V <sub>SS</sub>	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V <sub>SS</sub>	193	V <sub>SS</sub>	194	DQ63
45	DQ17	46	DQ21	95	V <sub>DD</sub>	96	V <sub>DD</sub>	145	V <sub>SS</sub>	146	DQS5	195	SDA	196	V <sub>SS</sub>
47	V <sub>SS</sub>	48	V <sub>SS</sub>	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	DQS2	50	NC	99	A3	100	A2	149	V <sub>SS</sub>	150	V <sub>SS</sub>	199	V <sub>DDSPD</sub>	200	SA1

Note: All pin assignments are consistent for all 8-byte unbuffered versions.

CKE1, CS1 and ODT1 are for 1GB/2GB modules only.

A13 is for 2GB modules only.

## Input/Output Functional Description

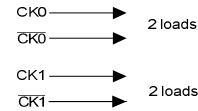
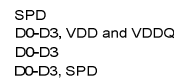
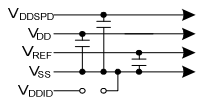
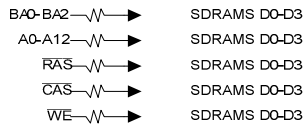
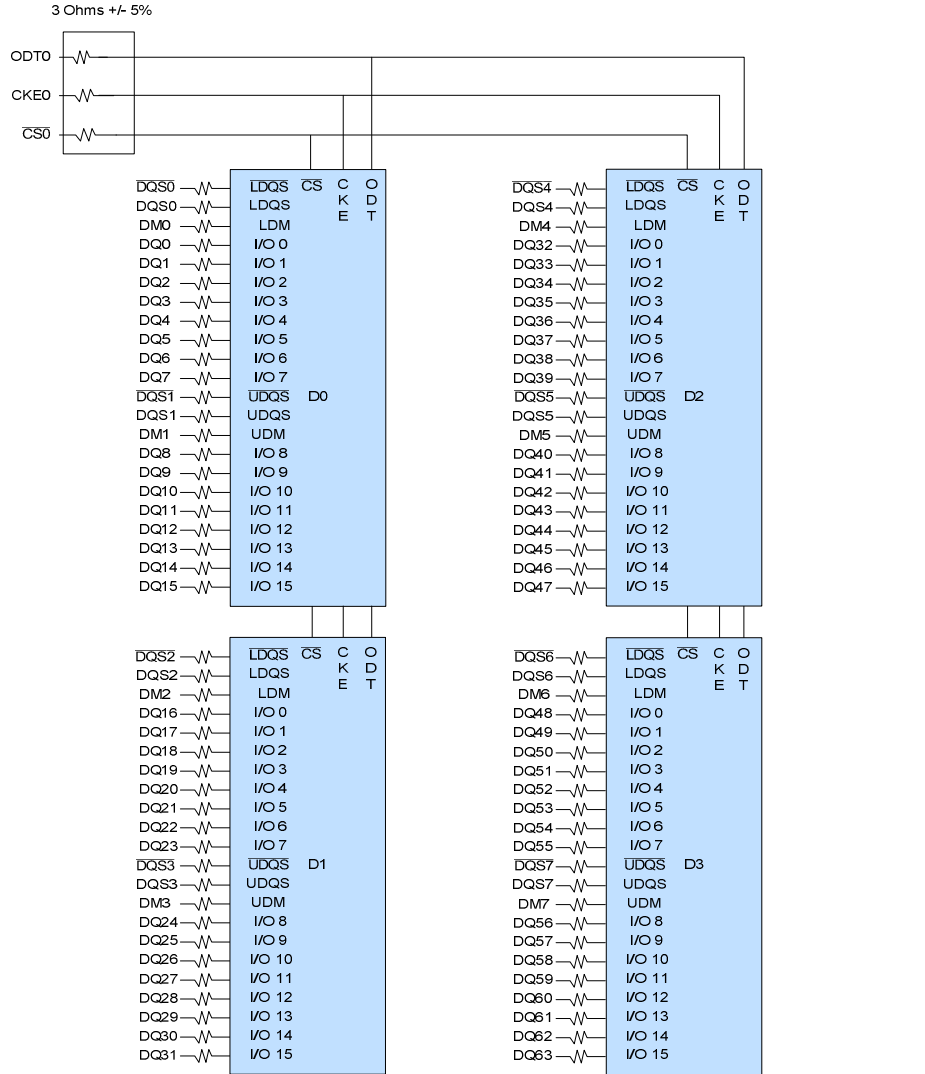
Symbol	Type	Polarity	Function
CK0, CK1	(SSTL)	Positive Edge	The positive line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL. All the DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks.
$\overline{\text{CK0}}, \overline{\text{CK1}}$	(SSTL)	Negative Edge	The negative line of the differential pair of system clock inputs which drives the input to the on-DIMM PLL.
CKE0, CKE1	(SSTL)	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{\text{CS0}}, \overline{\text{CS1}}$	(SSTL)	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$ define the operation to be executed by the SDRAM.
$V_{\text{REF}}$	Supply		Reference voltage for SSTL-18 inputs
ODT0, ODT1	Input	Active High	On-Die Termination control signals
BA0, BA1, BA2	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 – A9 A10/AP A11, A12/A13	(SSTL)	-	During a Bank Activate command cycle, A0-A12/A13 define the row address (RA0-RA12/RA13) when sampled at the rising clock edge. A13 applies on 2GB SODIMM only. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1/BA2 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1/BA2 to control which bank(s) to precharge. If AP is high all 8 banks will be precharged regardless of the state of BA0/BA1/BA2. If AP is low, then BA0/BA1/BA2 are used to define which bank to pre-charge.
DQ0 – DQ63	(SSTL)	Active High	Data and Check Bit Input/Output pins.
$V_{\text{DD}}, V_{\text{SS}}$	Supply		Power and ground for the DDR2 SDRAM input buffers and core logic
DQS0 – DQS7 $\overline{\text{DQS0}} - \overline{\text{DQS7}}$	(SSTL)	Negative and Positive Edge	Data strobe for input and output data
DM0 – DM7	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect. DM8 is associated with check bits CB0-CB7, and is not used on x64 modules.
SA0 – SA1		-	Address inputs. Connected to either VDD or VSS on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pull-up.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pull-up.
$V_{\text{DDSPD}}$	Supply		Serial EEPROM positive power supply.

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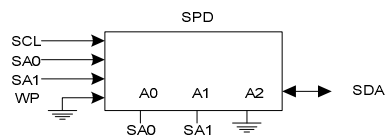
**Functional Block Diagram**

[512MB – 1 Rank, 64Mx16 DDR2 SDRAMs]



**Notes**

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22 +/- 5% Ohms
4. V<sub>DDID</sub> strap connections (for memory device V<sub>DD</sub>, V<sub>DDQ</sub>):  
 STRAP OUT (OPEN): V<sub>DD</sub> = V<sub>DDQ</sub>  
 STRAP IN (V<sub>SS</sub>): V<sub>DD</sub> is not equal to V<sub>DDQ</sub>

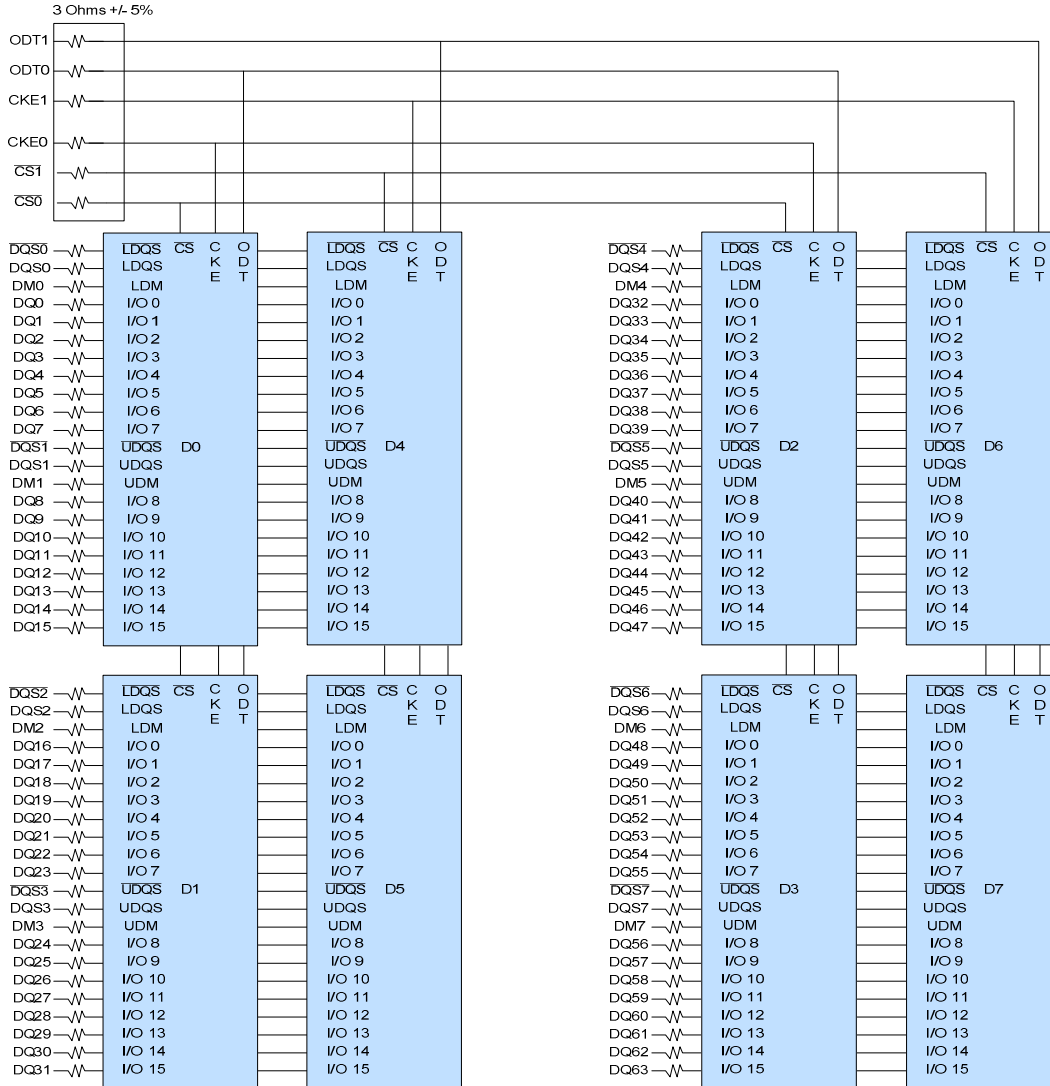


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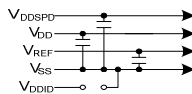


**Functional Block Diagram**

[1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs]



BA0-BA2 → SDRAMs D0-D7  
 A0-A12 → SDRAMs D0-D7  
 RAS → SDRAMs D0-D7  
 CAS → SDRAMs D0-D7  
 WE → SDRAMs D0-D7



CK0 → 4 loads  
 CK0 → 4 loads  
 CK1 → 4 loads  
 CK1 → 4 loads

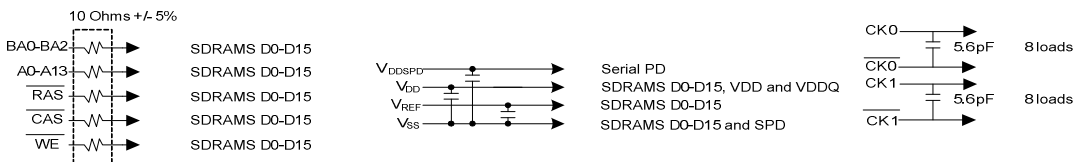
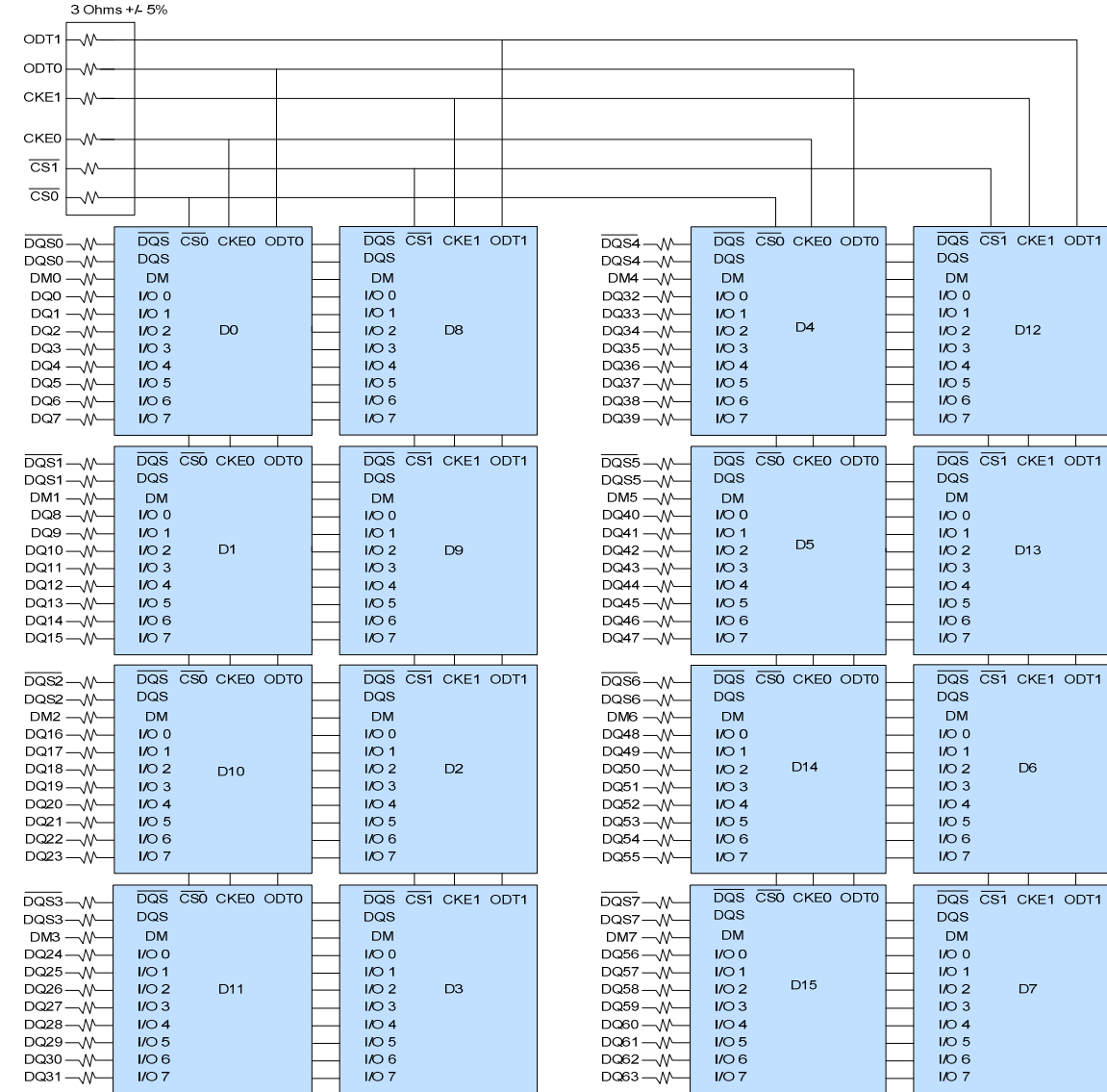
**Notes**

1. DQ wiring may differ from that described in this drawing.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22 +/- 5% Ohms
4. VDDID strap connections (for memory device V<sub>DD</sub>, V<sub>DDQ</sub>):  
 STRAP OUT (OPEN): V<sub>DD</sub> = V<sub>DDQ</sub>  
 STRAP IN (V<sub>SS</sub>): V<sub>DDIS</sub> not equal to V<sub>DDQ</sub>

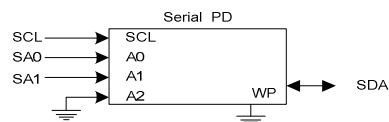


## Functional Block Diagram

[2GB – 2 Ranks, 128M x8 DDR2 SDRAMs]



**Notes**  
 Unless otherwise noted resistor values are 22 Ohms +/- 5%  
 DQ wiring may differ from that described in this drawing.  
 However, DQ/DM/DQS/DQS relationships are maintained as shown.





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**Unbuffered DDR2 SO-DIMM**



**Serial Presence Detect (512MB – 1 Rank, 64Mx16 DDR2 SDRAMs) (Part 1 of 2)**

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note
		-37B	-3C	-AD	-AC	-37B	-3C	-AD	-AC	
0	Number of Serial PD Bytes Written during Production	128				80	80	80	80	
1	Total Number of Bytes in Serial PD device	256				08	08	08	08	
2	Fundamental Memory Type	DDR2 SDRAM				08	08	08	08	
3	Number of Row Addresses on Assembly	13				0D	0D	0D	0D	
4	Number of Column Addresses on Assembly	10				0A	0A	0A	0A	
5	Number of DIMM Ranks, Package, and Height	Module Height = 30.0mm, 1 rank				60	60	60	60	
6	Data Width of Assembly	X64				40	40	40	40	
7	Reserved	Undefined				00	00	00	00	
8	Voltage Interface Level of this Assembly	SSTL 1.8V				05	05	05	05	
9	DDR2 SDRAM Device Cycle Time at CL=X	3.75ns	3ns	2.5ns		3D	30	25	25	
10	DDR2 SDRAM Device Access Time (t <sub>ac</sub> ) from Clock at CL=X	0.5ns	0.45ns	0.4ns		50	45	40	40	
11	DIMM Configuration Type	Non Address/Command Parity, Non Data ECC, Non Data Parity,				00	00	00	00	
12	Refresh Rate/Type	7.8 μs				82	82	82	82	
13	Primary DDR2 SDRAM Width	X16				10	10	10	10	
14	Error Checking DDR2 SDRAM Device Width	Undefined				00	00	00	00	
15	Reserved	Undefined				00	00	00	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8				0C	0C	0C	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8				08	08	08	08	
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3,4,5		4,5,6	3,4,5	38	38	70	38	
19	DIMM Mechanical Characteristics	x ≤ 3.80 (mm)				01	01	01	01	
20	DDR2 SDRAM DIMM Type Information	SO-DIMM (67.6mm)				04	04	04	04	
21	DDR2 SDRAM Module Attributes	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 0, Number of Active Registers : 1,				00	00	00	00	
22	DDR2 SDRAM Device Attributes: General	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,				07	07	07	07	
23	Minimum Clock Cycle at CL=X-1	3.75ns		3ns	3.75ns	3D	3D	30	3D	
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns		0.45ns	0.5ns	50	50	45	50	
25	Minimum Clock Cycle Time at CL=X-2	5ns		3.75ns	5ns	50	50	3D	50	
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns		0.5ns	0.6ns	60	60	50	60	
27	Minimum Row Precharge Time (t <sub>RP</sub> )	15ns			12.5ns	3C	3C	3C	32	
28	Minimum Row Active to Row Active delay (t <sub>RRD</sub> )	10ns				28	28	28	28	
29	Minimum RAS to $\overline{\text{CAS}}$ delay (t <sub>RCD</sub> )	15ns			12.5ns	3C	3C	3C	32	
30	Minimum Active to Precharge Time (t <sub>RAS</sub> )	45ns				2D	2D	2D	2D	
31	Module Rank Density	512MB				80	80	80	80	
32	Address and Command Setup Time Before Clock (t <sub>IS</sub> )	0.25ns	0.2ns	0.17ns		25	20	17	17	
33	Address and Command Hold Time After Clock (t <sub>IH</sub> )	0.37ns	0.27ns	0.25ns		37	27	25	25	
34	Data Input Setup Time Before Clock (t <sub>DS</sub> )	0.1ns			0.05ns	10	10	05	05	
35	Data Input Hold Time After Clock (t <sub>DH</sub> )	0.22ns	0.17ns	0.12ns		22	17	12	12	

NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN  
 NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS  
 512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64  
 PC2-4200 / PC2-5300 / PC2-6400  
 Unbuffered DDR2 SO-DIMM



**Serial Presence Detect (512MB – 1 Rank, 64Mx16 DDR2 SDRAMs) (Part 2 of 2)**

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note
		-37B	-3C	-AD	-AC	-37B	-3C	-AD	-AC	
36	Write Recovery Time ( $t_{WR}$ )	15ns				3C	3C	3C	3C	
37	Internal Write to Read Command delay ( $t_{WTR}$ )	7.5ns				1E	1E	1E	1E	
38	Internal Read to Precharge delay ( $t_{RTP}$ )	7.5ns				1E	1E	1E	1E	
39	Reserved	Undefined				00	00	00	00	
40	Extension of Byte 41 $t_{RC}$ and Byte 42 $t_{RFC}$	The number below a decimal point of $t_{RC}$ and $t_{RFC}$ are 0, $t_{RFC}$ is less than 256ns.				06	06	06	36	
41	Minimum Core Cycle Time ( $t_{RC}$ )	60ns		57.5ns		3C	3C	3C	39	
42	Min. Auto Refresh Command Cycle Time ( $t_{RFC}$ )	127.5ns				7F	7F	7F	7F	
43	Maximum Clock Cycle Time ( $t_{CK}$ )	8ns				80	80	80	80	
44	Max. DQS-DQ Skew Factor (tQHS)	0.3ns	0.24ns	0.2ns		1E	18	14	14	
45	Read Data Hold Skew Factor (tQHS)	0.4ns	0.34ns	0.3ns		28	22	1E	1E	
46-61	Reserved	Undefined				00	00	00	00	
62	SPD Reversion	1.3				13	13	13	13	
63	Checksum for Byte 0-62	Checksum Data				ED	A9	73	8F	
64-71	Manufacturer's JEDEC ID Code	Nanya				7F7F7F0B00000000				
72	Module Manufacturing Location	Manufacturing code				-				
73-91	Module Part number	Module Part Number in ASCII				-				1
92-255	Reserved	Undefined				-				

**Note 1:**

Module part number:

NT512T64UH4D0FN-37B → 4E543531325436345548344430464E2D333742  
 NT512T64UH4D0FN-3C → 4E543531325436345548344430464E2D334320  
 NT512T64UH4D0FN-AD → 4E543531325436345548344430464E2D414420  
 NT512T64UH4D0FN-AC → 4E543531325436345548344430464E2D414320  
 NT512T64UH4D0FS-37B → 4E54353132543634554834443046532D333742  
 NT512T64UH4D0FS-3C → 4E54353132543634554834443046532D334320  
 NT512T64UH4D0FS-AD → 4E54353132543634554834443046532D414420  
 NT512T64UH4D0FS-AC → 4E54353132543634554834443046532D414320

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



**Serial Presence Detect (1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs) (Part 1 of 2)**

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note
		-37B	-3C	-AD	-AC	-37B	-3C	-AD	-AC	
0	Number of Serial PD Bytes Written during Production	128				80	80	80	80	
1	Total Number of Bytes in Serial PD device	256				08	08	08	08	
2	Fundamental Memory Type	DDR2 SDRAM				08	08	08	08	
3	Number of Row Addresses on Assembly	13				0D	0D	0D	0D	
4	Number of Column Addresses on Assembly	10				0A	0A	0A	0A	
5	Number of DIMM Ranks, Package, and Height	Module Height = 30.0mm, 2 ranks				61	61	61	61	
6	Data Width of Assembly	X64				40	40	40	40	
7	Reserved	Undefined				00	00	00	00	
8	Voltage Interface Level of this Assembly	SSTL 1.8V				05	05	05	05	
9	DDR2 SDRAM Device Cycle Time at CL=X	3.75ns	3ns	2.5ns		3D	30	25	25	
10	DDR2 SDRAM Device Access Time (t <sub>ac</sub> ) from Clock at CL=X	0.5ns	0.45ns	0.4ns		50	45	40	40	
11	DIMM Configuration Type	Non Address/Command Parity, Non Data ECC, Non Data Parity,				00	00	00	00	
12	Refresh Rate/Type	7.8 μs				82	82	82	82	
13	Primary DDR2 SDRAM Width	X16				10	10	10	10	
14	Error Checking DDR2 SDRAM Device Width	Undefined				00	00	00	00	
15	Reserved	Undefined				00	00	00	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8				0C	0C	0C	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8				08	08	08	08	
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3,4,5		4,5,6	3,4,5	38	38	70	38	
19	DIMM Mechanical Characteristics	x ≤ 3.80 (mm)				01	01	01	01	
20	DDR2 SDRAM DIMM Type Information	SO-DIMM (67.6mm)				04	04	04	04	
21	DDR2 SDRAM Module Attributes	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 0, Number of Active Registers : 1,				00	00	00	00	
22	DDR2 SDRAM Device Attributes: General	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,				07	07	07	07	
23	Minimum Clock Cycle at CL=X-1	3.75ns		3ns	3.75ns	3D	3D	30	3D	
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns		0.45ns	0.5ns	50	50	45	50	
25	Minimum Clock Cycle Time at CL=X-2	5ns		3.75ns	5ns	50	50	3D	50	
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns		0.5ns	0.6ns	60	60	50	60	
27	Minimum Row Precharge Time (t <sub>RP</sub> )	15ns			12.5ns	3C	3C	3C	32	
28	Minimum Row Active to Row Active delay (t <sub>RRD</sub> )	10ns				28	28	28	28	
29	Minimum RAS to $\overline{\text{CAS}}$ delay (t <sub>RCD</sub> )	15ns			12.5ns	3C	3C	3C	32	
30	Minimum Active to Precharge Time (t <sub>RAS</sub> )	45ns				2D	2D	2D	2D	
31	Module Rank Density	512MB				80	80	80	80	
32	Address and Command Setup Time Before Clock (t <sub>IS</sub> )	0.25ns	0.2ns	0.17ns		25	20	17	17	
33	Address and Command Hold Time After Clock (t <sub>IH</sub> )	0.37ns	0.27ns	0.25ns		37	27	25	25	
34	Data Input Setup Time Before Clock (t <sub>DS</sub> )	0.1ns			0.05ns	10	10	05	05	
35	Data Input Hold Time After Clock (t <sub>DH</sub> )	0.22ns	0.17ns	0.12ns		22	17	12	12	

NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN  
 NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS  
 512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64  
 PC2-4200 / PC2-5300 / PC2-6400  
 Unbuffered DDR2 SO-DIMM



**Serial Presence Detect (1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs) (Part 2 of 2)**

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note
		-37B	-3C	-AD	-AC	-37B	-3C	-AD	-AC	
36	Write Recovery Time ( $t_{WR}$ )	15ns				3C	3C	3C	3C	
37	Internal Write to Read Command delay ( $t_{WTR}$ )	7.5ns				1E	1E	1E	1E	
38	Internal Read to Precharge delay ( $t_{RTP}$ )	7.5ns				1E	1E	1E	1E	
39	Reserved	Undefined				00	00	00	00	
40	Extension of Byte 41 $t_{RC}$ and Byte 42 $t_{RFC}$	The number below a decimal point of $t_{RC}$ and $t_{RFC}$ are 0, $t_{RFC}$ is less than 256ns.				06	06	06	36	
41	Minimum Core Cycle Time ( $t_{RC}$ )	60ns				3C	3C	3C	39	
42	Min. Auto Refresh Command Cycle Time ( $t_{RFC}$ )	127.5ns				7F	7F	7F	7F	
43	Maximum Clock Cycle Time ( $t_{CK}$ )	8ns				80	80	80	80	
44	Max. DQS-DQ Skew Factor (tQHS)	0.3ns	0.24ns	0.2ns		1E	18	14	14	
45	Read Data Hold Skew Factor (tQHS)	0.4ns	0.34ns	0.3ns		28	22	1E	1E	
46-61	Reserved	Undefined				00	00	00	00	
62	SPD Reversion	1.3				13	13	13	13	
63	Checksum for Byte 0-62	Checksum Data				EE	AA	74	90	
64-71	Manufacturer's JEDEC ID Code	NANYA				7F7F7F0B00000000				
72	Module Manufacturing Location	Manufacturing code				-				
73-91	Module Part number	Module Part Number in ASCII				-				1
92-255	Reserved	undefined				-				

**Note 1:**

Module part number:

NT1GT64UH8D0FN-37B→4E5431475436345548384430464E2D33374220  
 NT1GT64UH8D0FN-3C→4E5431475436345548384430464E2D33432020  
 NT1GT64UH8D0FN-AD→4E5431475436345548384430464E2D41442020  
 NT1GT64UH8D0FN-AC→4E5431475436345548384430464E2D41432020  
 NT1GT64UH8D0FS-37B→4E543147543634554838443046532D33374220  
 NT1GT64UH8D0FS-3C→4E543147543634554838443046532D33432020  
 NT1GT64UH8D0FS-AD→4E543147543634554838443046532D41442020  
 NT1GT64UH8D0FS-AC→4E543147543634554838443046532D41432020

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



**Serial Presence Detect (2GB – 2 Ranks, 128Mx8 DDR2 SDRAMs) (Part 1 of 2)**

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note
		-37B	-3C	-AD	-AC	-37B	-3C	-AD	-AC	
0	Number of Serial PD Bytes Written during Production	128				80	80	80	80	
1	Total Number of Bytes in Serial PD device	256				08	08	08	08	
2	Fundamental Memory Type	DDR2 SDRAM				08	08	08	08	
3	Number of Row Addresses on Assembly	14				0E	0E	0E	0E	
4	Number of Column Addresses on Assembly	10				0A	0A	0A	0A	
5	Number of DIMM Ranks, Package, and Height	Module Height = 30.0mm, 2 ranks				61	61	61	61	
6	Data Width of Assembly	X64				40	40	40	40	
7	Reserved	Undefined				00	00	00	00	
8	Voltage Interface Level of this Assembly	SSTL 1.8V				05	05	05	05	
9	DDR2 SDRAM Device Cycle Time at CL=X	3.75ns	3ns	2.5ns		3D	30	25	25	
10	DDR2 SDRAM Device Access Time (t <sub>ac</sub> ) from Clock at CL=X	0.5ns	0.45ns	0.4ns		50	45	40	40	
11	DIMM Configuration Type	Non Address/Command Parity, Non Data ECC, Non Data Parity,				00	00	00	00	
12	Refresh Rate/Type	7.8 μs				82	82	82	82	
13	Primary DDR2 SDRAM Width	X8				08	08	08	08	
14	Error Checking DDR2 SDRAM Device Width	Undefined				00	00	00	00	
15	Reserved	Undefined				00	00	00	00	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	4,8				0C	0C	0C	0C	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	8				08	08	08	08	
18	DDR2 SDRAM Device Attributes: $\overline{\text{CAS}}$ Latencies Supported	3,4,5		4,5,6	3,4,5	38	38	70	38	
19	DIMM Mechanical Characteristics	x ≤ 3.80 (mm)				01	01	01	01	
20	DDR2 SDRAM DIMM Type Information	SO-DIMM (67.6mm)				04	04	04	04	
21	DDR2 SDRAM Module Attributes	Analysis probe installed : No, FET Switch External Enable : No, Number of PLLs : 0, Number of Active Registers : 1,				00	00	00	00	
22	DDR2 SDRAM Device Attributes: General	Supports Weak Driver, Supports 50 ohm ODT, Supports PASR,				07	07	07	07	
23	Minimum Clock Cycle at CL=X-1	3.75ns		3ns	3.75ns	3D	3D	30	3D	
24	Maximum Data Access Time from Clock at CL=X-1	0.5ns		0.45ns	0.5ns	50	50	45	50	
25	Minimum Clock Cycle Time at CL=X-2	5ns		3.75ns	5ns	50	50	3D	50	
26	Maximum Data Access Time from Clock at CL=X-2	0.6ns		0.5ns	0.6ns	60	60	50	60	
27	Minimum Row Precharge Time (t <sub>RP</sub> )	15ns			12.5ns	3C	3C	3C	32	
28	Minimum Row Active to Row Active delay (t <sub>RRD</sub> )	7.5ns				1E	1E	1E	1E	
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t <sub>RCD</sub> )	15ns			12.5ns	3C	3C	3C	32	
30	Minimum Active to Precharge Time (t <sub>RAS</sub> )	45ns				2D	2D	2D	2D	
31	Module Rank Density	1GB				01	01	01	01	
32	Address and Command Setup Time Before Clock (t <sub>IS</sub> )	0.25ns	0.2ns	0.17ns		25	20	17	17	
33	Address and Command Hold Time After Clock (t <sub>IH</sub> )	0.37ns	0.27ns	0.25ns		37	27	25	25	
34	Data Input Setup Time Before Clock (t <sub>DS</sub> )	0.1ns			0.05ns	10	10	05	05	
35	Data Input Hold Time After Clock (t <sub>DH</sub> )	0.22ns	0.17ns	0.12ns		22	17	12	12	

NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN  
 NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS  
 512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64  
 PC2-4200 / PC2-5300 / PC2-6400  
 Unbuffered DDR2 SO-DIMM



**Serial Presence Detect (2GB – 2 Ranks, 128 M x 8 DDR2 SDRAMs) (Part 2 of 2)**

Byte	Description	SPD Entry Value				Serial PD Data Entry (Hex.)				Note
		-37B	-3C	-AD	-AC	-37B	-3C	-AD	-AC	
36	Write Recovery Time ( $t_{WR}$ )	15ns				3C	3C	3C	3C	
37	Internal Write to Read Command delay ( $t_{WTR}$ )	7.5ns				1E	1E	1E	1E	
38	Internal Read to Precharge delay ( $t_{RTP}$ )	7.5ns				1E	1E	1E	1E	
39	Reserved	Undefined				00	00	00	00	
40	Extension of Byte 41 $t_{RC}$ and Byte 42 $t_{RFC}$	The number below a decimal point of $t_{RC}$ and $t_{RFC}$ are 0, $t_{RFC}$ is less than 256ns.				06	06	06	36	
41	Minimum Core Cycle Time ( $t_{RC}$ )	60ns				3C	3C	3C	39	
42	Min. Auto Refresh Command Cycle Time ( $t_{RFC}$ )	127.5ns				7F	7F	7F	7F	
43	Maximum Clock Cycle Time ( $t_{CK}$ )	8ns				80	80	80	80	
44	Max. DQS-DQ Skew Factor ( $t_{QHS}$ )	0.3ns	0.24ns	0.2ns		1E	18	14	14	
45	Read Data Hold Skew Factor ( $t_{QHS}$ )	0.4ns	0.34ns	0.3ns		28	22	1E	1E	
46-61	Reserved	Undefined				00	00	00	00	
62	SPD Reversion	1.3				13	13	13	13	
63	Checksum for Byte 0-62	Checksum Data				5E	1A	E4	00	
64-71	Manufacturer's JEDEC ID Code	NANYA				7F7F7F0B00000000				
72	Module Manufacturing Location	Manufacturing code				-				
73-91	Module Part number	Module Part Number in ASCII				-				1
92-255	Reserved	undefined				-				

**Note 1:**

Module part number:

NT2GT64U8HD0BN-37B → 4E5432475436345538484430424E2D33374220  
 NT2GT64U8HD0BN-3C → 4E5432475436345538484430424E2D33432020  
 NT2GT64U8HD0BN-AD → 4E5432475436345538484430424E2D41442020  
 NT2GT64U8HD0BN-AC → 4E5432475436345538484430424E2D41432020  
 NT2GT64U8HD0BS-37B → 4E543247543634553848443042532D33374220  
 NT2GT64U8HD0BS-3C → 4E543247543634553848443042532D33432020  
 NT2GT64U8HD0BS-AD → 4E543247543634553848443042532D41442020  
 NT2GT64U8HD0BS-AC → 4E543247543634553848443042532D41432020

NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN  
 NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS  
 512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64  
 PC2-4200 / PC2-5300 / PC2-6400  
 Unbuffered DDR2 SO-DIMM



## Environmental Requirements

Symbol	Parameter	Rating	Units
T <sub>OPR</sub>	Operating Temperature (ambient)	0 to 65	°C
H <sub>OPR</sub>	Operating Humidity (relative)	10 to 90	%
T <sub>STG</sub>	Storage Temperature	-50 to 100	°C
H <sub>STG</sub>	Storage Humidity (without condensation)	5 to 95	%
	Barometric pressure (operating & storage) up to 9850ft.	105 to 69	kPa

**Note:** Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

## Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
V <sub>DD</sub>	Voltage on VDD pins relative to V <sub>SS</sub>	-1.0 to +2.3	V
V <sub>DDQ</sub>	Voltage on VDDQ pins relative to V <sub>SS</sub>	-0.5 to +2.3	V
V <sub>DDL</sub>	Voltage on VDDL pins relative to V <sub>SS</sub>	-0.5 to +2.3	V
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on I/O pins relative to V <sub>SS</sub>	-0.5 to +2.3	V
T <sub>STG</sub>	Storage Temperature (Plastic)	-55 to +100	°C

**Note:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Storage temperature is the case surface temperature on the center/top side of the DRAM.

## Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T <sub>CASE</sub>	Operating Temperature (Ambient)	0 to 95	°C	1

**Note:**

- Case temperature is measured at top and center side of any DRAMs.
- t<sub>CASE</sub> > 85 °C → t<sub>REFI</sub> = 3.9 μs

## DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V <sub>DD</sub>	Supply Voltage	1.7	1.9	V	1
V <sub>DDL</sub>	DLL Supply Voltage	1.7	1.9	V	1
V <sub>DDQ</sub>	Output Supply Voltage	1.7	1.9	V	1
V <sub>SS</sub> , V <sub>SSQ</sub>	Supply Voltage, I/O Supply Voltage	0	0	V	
V <sub>REF</sub>	Input Reference Voltage	0.49V <sub>DDQ</sub>	0.51V <sub>DDQ</sub>	V	1, 2
V <sub>TT</sub>	Termination Voltage	V <sub>REF</sub> - 0.04	V <sub>REF</sub> + 0.04	V	3

**Note:**

- There is no specific device VDD supply voltage requirement for SSTL\_18 compliance. However, VDDQ must be less than or equal to VDD under all conditions.
- VREF is expected to be equal to 0.5 V<sub>DDQ</sub> of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
- VTT of transmitting device must track VREF of receiving device.

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



**ODT DC Electrical Characteristics**

Parameter/Condition	Symbol	Min.	Nom.	Max.	Units	Note
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75ohm	Rtt1 (eff)	60	75	90	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150ohm	Rtt2 (eff)	120	150	180	ohm	1
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50ohm	Rtt3 (eff)	40	50	60	ohm	1
Deviation of $V_M$ with respect to $V_{DDQ}/2$	Delta VM	-6		+6	%	1

Note1: Test condition for Rtt measurements.

**Input AC/DC logic level**

Symbol	Parameter	PC2-4300		PC2-5300		PC2-6400		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>IH</sub> (AC)	Input High (Logic1) Voltage	V <sub>REF</sub> + 0.250	-	V <sub>REF</sub> + 0.200	-	V <sub>REF</sub> + 0.200	-	V
V <sub>IL</sub> (AC)	Input Low (Logic0) Voltage	-	V <sub>REF</sub> - 0.250	-	V <sub>REF</sub> - 0.200	-	V <sub>REF</sub> - 0.200	V
V <sub>IH</sub> (DC)	Input High (Logic1) Voltage	V <sub>REF</sub> + 0.125	V <sub>DDQ</sub> + 0.3	V <sub>REF</sub> + 0.125	V <sub>DDQ</sub> + 0.3	V <sub>REF</sub> + 0.125	V <sub>DDQ</sub> + 0.3	V
V <sub>IL</sub> (DC)	Input Low (Logic0) Voltage	-0.3	V <sub>REF</sub> - 0.125	-0.3	V <sub>REF</sub> - 0.125	-0.3	V <sub>REF</sub> - 0.125	V



**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



### Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$  [512MB, 1 Rank, 64Mx16 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-4200 (-37B)	PC2-5300 (-3C)	PC2-6400 (-AD)	PC2-6400 (-AC)	Unit
IDD0	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC(MIN)}$ ; $t_{CK} = t_{CK(MIN)}$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	373	438	502	502	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC} = t_{RC(MIN)}$ ; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$ ; $I_{OUT} = 0\text{mA}$ ; address and control inputs changing once per clock cycle	458	541	620	620	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$	35	35	35	35	mA
IDD2Q	Precharge quiet standby current	172	189	206	206	mA
IDD2N	Idle Standby Current: $CS \geq V_{IH(MIN)}$ ; all banks idle; $CKE \geq V_{IH(MIN)}$ ; $t_{CK} = t_{CK(MIN)}$ ; address and control inputs changing once per clock cycle	241	274	310	310	mA
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; $MRS(12)=0$	118	125	133	133	mA
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; $MRS(12)=1$	53	53	53	53	mA
IDD3N	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH(MIN)}$ ; $CKE \geq V_{IH(MIN)}$ ; $t_{RC} = t_{RAS(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	232	255	280	280	mA
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$ ; $I_{OUT} = 0\text{mA}$	585	673	752	752	mA
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$	491	549	606	606	mA
IDD5B	Burst Refresh Current: $t_{RC} = t_{RFC(MIN)}$	880	968	990	990	mA
IDD6	Self-Refresh Current: $CKE \leq 0.2\text{V}$	40	40	40	40	mA
IDD7	Operating Current: four bank; four bank interleaving with $BL = 4$ , address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC(MIN)}$ ; $I_{OUT} = 0\text{mA}$ .	1276	1496	1672	1672	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



**Operating, Standby, and Refresh Currents**

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$  [1GB, 2 Ranks, 64Mx16 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-4200 (-37B)	PC2-5300 (-3C)	PC2-6400 (-AD)	PC2-6400 (-AC)	Unit
IDD0	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC(MIN)}$ ; $t_{CK} = t_{CK(MIN)}$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	605	693	782	782	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC} = t_{RC(MIN)}$ ; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$ ; $I_{OUT} = 0\text{mA}$ ; address and control inputs changing once per clock cycle	690	796	900	900	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$	70	70	70	70	mA
IDD2Q	Precharge quiet standby current	344	379	412	412	mA
IDD2N	Idle Standby Current: $CS \geq V_{IH(MIN)}$ ; all banks idle; $CKE \geq V_{IH(MIN)}$ ; $t_{CK} = t_{CK(MIN)}$ ; address and control inputs changing once per clock cycle	482	549	620	620	mA
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; $MRS(12)=0$	235	250	265	265	mA
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; $MRS(12)=1$	106	106	106	106	mA
IDD3N	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH(MIN)}$ ; $CKE \geq V_{IH(MIN)}$ ; $t_{RC} = t_{RAS(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	463	510	561	561	mA
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$ ; $I_{OUT} = 0\text{mA}$	816	928	1032	1032	mA
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$	723	804	886	886	mA
IDD5B	Burst Refresh Current: $t_{RC} = t_{RFC(MIN)}$	1112	1223	1270	1270	mA
IDD6	Self-Refresh Current: $CKE \leq 0.2\text{V}$	79	79	79	79	mA
IDD7	Operating Current: four bank; four bank interleaving with $BL = 4$ , address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC(MIN)}$ ; $I_{OUT} = 0\text{mA}$ .	1508	1751	1952	1952	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



## Operating, Standby, and Refresh Currents

$T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = V_{DD} = 1.8\text{V} \pm 0.1\text{V}$  [2GB, 2 Ranks, 128Mx8 DDR2 SDRAMs]

Symbol	Parameter/Condition	PC2-4200 (-37B)	PC2-5300 (-3C)	PC2-6400 (-AD)	PC2-6400 (-AC)	Unit
IDD0	Operating Current: one bank; active/precharge; $t_{RC} = t_{RC(MIN)}$ ; $t_{CK} = t_{CK(MIN)}$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1204	1379	1556	1556	mA
IDD1	Operating Current: one bank; active/read/precharge; Burst = 4; $t_{RC} = t_{RC(MIN)}$ ; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$ ; $I_{OUT} = 0\text{mA}$ ; address and control inputs changing once per clock cycle	1138	1293	1447	1447	mA
IDD2P	Precharge Power-Down Standby Current: all banks idle; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$	141	141	141	141	mA
IDD2Q	Precharge quiet standby current	705	771	840	840	mA
IDD2N	Idle Standby Current: $CS \geq V_{IH(MIN)}$ ; all banks idle; $CKE \geq V_{IH(MIN)}$ ; $t_{CK} = t_{CK(MIN)}$ ; address and control inputs changing once per clock cycle	983	1115	1252	1252	mA
IDD3PF	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; $MRS(12)=0$	490	524	553	553	mA
IDD3PS	Active Power-Down Standby Current: one bank active; power-down mode; $CKE \leq V_{IL(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; $MRS(12)=1$	231	231	234	234	mA
IDD3N	Active Standby Current: one bank; active/precharge; $CS \geq V_{IH(MIN)}$ ; $CKE \geq V_{IH(MIN)}$ ; $t_{RC} = t_{RAS(MAX)}$ ; $t_{CK} = t_{CK(MIN)}$ ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	897	989	1086	1086	mA
IDD4R	Operating Current: one bank; Burst = 4; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$ ; $I_{OUT} = 0\text{mA}$	1396	1572	1740	1740	mA
IDD4W	Operating Current: one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; $CL = 4$ ; $t_{CK} = t_{CK(MIN)}$	1280	1417	1556	1556	mA
IDD5B	Burst Refresh Current: $t_{RC} = t_{RFC(MIN)}$	2208	2431	2523	2523	mA
IDD6	Self-Refresh Current: $CKE \leq 0.2\text{V}$	158	158	158	158	mA
IDD7	Operating Current: four bank; four bank interleaving with $BL = 4$ , address and control inputs randomly changing; 50% of data changing at every transfer; $t_{RC} = t_{RC(MIN)}$ ; $I_{OUT} = 0\text{mA}$ .	2195	2593	2991	2991	mA

Note: Module IDD was calculated from component IDD. It may differ from the actual measurement.

## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

( $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ ;  $V_{DDQ} = 1.8\text{V} \pm 0.1\text{V}$ ;  $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$ , See AC Characteristics) (Part 1 of 2)

Symbol	Parameter	-37B		-3C		-AD/-AC		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{AC}$	DQ output access time from $\text{CK}/\overline{\text{CK}}$	-0.5	+0.5	-0.48	+0.52	-0.40	+0.40	ns	
$t_{DQSCK}$	DQS output access time from $\text{CK}/\overline{\text{CK}}$	-0.45	+0.45	-0.4	+0.4	-0.35	+0.35	ns	
$t_{CH}$	CK high-level width	0.45	0.55	0.48	0.52	0.48	0.52	$t_{CK}$	
$t_{CL}$	CK low-level width	0.45	0.55	0.48	0.52	0.48	0.52	$t_{CK}$	
$t_{HP}$	Minimum half clk period for any given cycle; defined by clk high ( $t_{CH}$ ) or clk low ( $t_{CL}$ ) time	$t_{CH}$ or $t_{CL}$	-	$t_{CH}$ or $t_{CL}$	-	$t_{CH}$ or $t_{CL}$	-	$t_{CK}$	
$t_{CK}$	Clock Cycle Time	3.75	8	3	8	2.5	8	ns	
$t_{DH}$	DQ and DM input hold time	225	-	175	-	125	-	ps	
$t_{DS}$	DQ and DM input setup time	100	-	100	-	50	-	ps	
$t_{IPW}$	Input pulse width	0.6	-	0.6	-	0.6	-	$t_{CK}$	
$t_{DIPW}$	DQ and DM input pulse width (each input)	0.35	-	0.35	-	0.35	-	$t_{CK}$	
$t_{HZ}$	Data-out high-impedance time from $\text{CK}/\overline{\text{CK}}$	-	$t_{AC\text{ max}}$	-	$t_{AC\text{ max}}$	-	$t_{AC\text{ max}}$	ns	
$t_{LZ(DQ)}$	Data-out low-impedance time from $\text{CK}/\overline{\text{CK}}$	$2t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$2t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$2t_{AC\text{ min}}$	$t_{AC\text{ max}}$	ns	
$t_{LZ(DQS)}$	DQS low-impedance time from $\text{CK}/\overline{\text{CK}}$	$t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$t_{AC\text{ min}}$	$t_{AC\text{ max}}$	$t_{AC\text{ min}}$	$t_{AC\text{ max}}$	ns	
$t_{DQSQ}$	DQS-DQ skew (DQS & associated DQ signals)	-	0.30	-	0.24	-	0.20	ns	
$t_{QHS}$	Data hold Skew Factor	-	0.4	-	0.34	-	0.30	ns	
$t_{QH}$	Data output hold time from DQS	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	ns	
$t_{DQSS}$	Write command to 1 <sup>st</sup> DQS latching transition	-0.25	0.25	-0.25	0.25	-0.25	0.25	$t_{CK}$	
$t_{DQSH}$	DQS input high pulse width	0.35	-	0.35	-	0.35	-	$t_{CK}$	
$t_{DQSL}$	DQS input low pulse width	0.35	-	0.35	-	0.35	-	$t_{CK}$	
$t_{DSS}$	DQS falling edge to CK setup time (write cycle)	0.2	-	0.2	-	0.2	-	$t_{CK}$	
$t_{DSH}$	DQS falling edge hold time from CK (write cycle)	0.2	-	0.2	-	0.2	-	$t_{CK}$	
$t_{MRD}$	Mode register set command cycle time	2	-	2	-	2	-	$t_{CK}$	
$t_{WPST}$	Write postamble	0.40	0.60	0.40	0.60	0.40	0.60	$t_{CK}$	
$t_{WPRE}$	Write preamble	0.35	-	0.35	-	0.35	-	$t_{CK}$	
$t_{IH}$	Address and control input hold time	0.375	-	0.275	-	0.250	-	ns	
$t_{IS}$	Address and control input setup time	0.25	-	0.2	-	0.175	-	ns	
$t_{RPRE}$	Read preamble	0.9	1.1	0.9	1.1	0.9	1.1	$t_{CK}$	
$t_{RPST}$	Read postamble	0.4	0.6	0.4	0.6	0.4	0.6	$t_{CK}$	
$t_{Delay}$	Minimum time clocks remains ON after CKE asynchronously drops Low	$t_{IS} + t_{CK} + t_{IH}$	-	$t_{IS} + t_{CK} + t_{IH}$	-	$t_{IS} + t_{CK} + t_{IH}$	-	ns	
$t_{RFC}$	Refresh to active/Refresh command time	105		105		105		ns	
$t_{REFI}$	Average Periodic Refresh Interval ( $85^{\circ}\text{C} < T_{CASE} \leq 95^{\circ}\text{C}$ )	3.9		3.9		3.9		$\mu\text{s}$	
	Average Periodic Refresh Interval ( $0^{\circ}\text{C} \leq T_{CASE} \leq 85^{\circ}\text{C}$ )	7.8		7.8		7.8		$\mu\text{s}$	

## AC Timing Specifications for DDR2 SDRAM Devices Used on Module

(T<sub>CASE</sub> = 0 °C ~ 85 °C; V<sub>DDQ</sub> = 1.8V ± 0.1V; V<sub>DD</sub> = 1.8V ± 0.1V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-37B		-3C		-AD/-AC		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>RRD</sub>	Active bank A to Active bank B command	7.5	-	7.5	-	7.5	-	ns	
t <sub>CCD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$	2	-	2	-	2	-	t <sub>CK</sub>	
t <sub>WR</sub>	Write recovery time	15	-	15	-	15	-	ns	
WR	Write recovery time with Auto-Precharge	t <sub>WR</sub> /t <sub>CK</sub>		t <sub>WR</sub> /t <sub>CK</sub>		t <sub>WR</sub> /t <sub>CK</sub>		ns	
t <sub>DAL</sub>	Auto precharge write recovery + precharge time	WR + t <sub>RP</sub>	-	WR + t <sub>RP</sub>	-	WR + t <sub>RP</sub>	-	t <sub>CK</sub>	
t <sub>WTR</sub>	Internal write to read command delay	7.5	-	7.5	-	7.5	-	ns	
t <sub>RTP</sub>	Internal read to precharge command delay	7.5	-	7.5	-	7.5	-	ns	
t <sub>XSNR</sub>	Exit self refresh to a Non-read command	t <sub>RFC</sub> + 10	-	t <sub>RFC</sub> + 10	-	t <sub>RFC</sub> + 10	-	ns	
t <sub>XSRD</sub>	Exit self refresh to a Read command	200	-	200	-	200	-	t <sub>CK</sub>	
t <sub>XP</sub>	Exit precharge power down to any Non-read command	2	-	2	-	2	-	t <sub>CK</sub>	
t <sub>XARD</sub>	Exit active power down to read command	2	-	2	-	2	-	t <sub>CK</sub>	
t <sub>XARDS</sub>	Exit active power down to read command	6-AL	-	7-AL	-	8-AL	-	t <sub>CK</sub>	
t <sub>CKE</sub>	CKE minimum pulse width	3	-	3	-	3	-	t <sub>CK</sub>	
t <sub>OIT</sub>	OCD drive mode output delay	0	12	0	12	0	12	ns	
<b>ODT</b>									
t <sub>AOND</sub>	ODT turn-on delay	2	2	2	2	2	2	t <sub>CK</sub>	
t <sub>AON</sub>	ODT turn-on	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 1	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 0.7	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 0.7	ns	
t <sub>AONPD</sub>	ODT turn-on (Power down mode)	t <sub>AC</sub> (min) + 2	2t <sub>CK</sub> + t <sub>AC</sub> (max) + 1	t <sub>AC</sub> (min) + 2	2t <sub>CK</sub> + t <sub>AC</sub> (max) + 1	t <sub>AC</sub> (min) + 2	2t <sub>CK</sub> + t <sub>AC</sub> (max) + 1	ns	
t <sub>AOFD</sub>	ODT turn-off delay	2.5	2.5	2.5	2.5	2.5	2.5	t <sub>CK</sub>	
t <sub>AOF</sub>	ODT turn-off	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 0.6	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 0.6	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 0.6	ns	
t <sub>AOFPD</sub>	ODT turn-off (Power down mode)	t <sub>AC</sub> (min) + 2	2.5t <sub>CK</sub> + t <sub>AC</sub> (max) + 1	t <sub>AC</sub> (min) + 2	2.5t <sub>CK</sub> + t <sub>AC</sub> (max) + 1	t <sub>AC</sub> (min) + 2	2.5t <sub>CK</sub> + t <sub>AC</sub> (max) + 1	ns	
t <sub>ANPD</sub>	ODT to power down entry latency	3	-	3	-	3	-	t <sub>CK</sub>	
t <sub>AXPD</sub>	ODT power down exit latency	8	-	8	-	8	-	t <sub>CK</sub>	

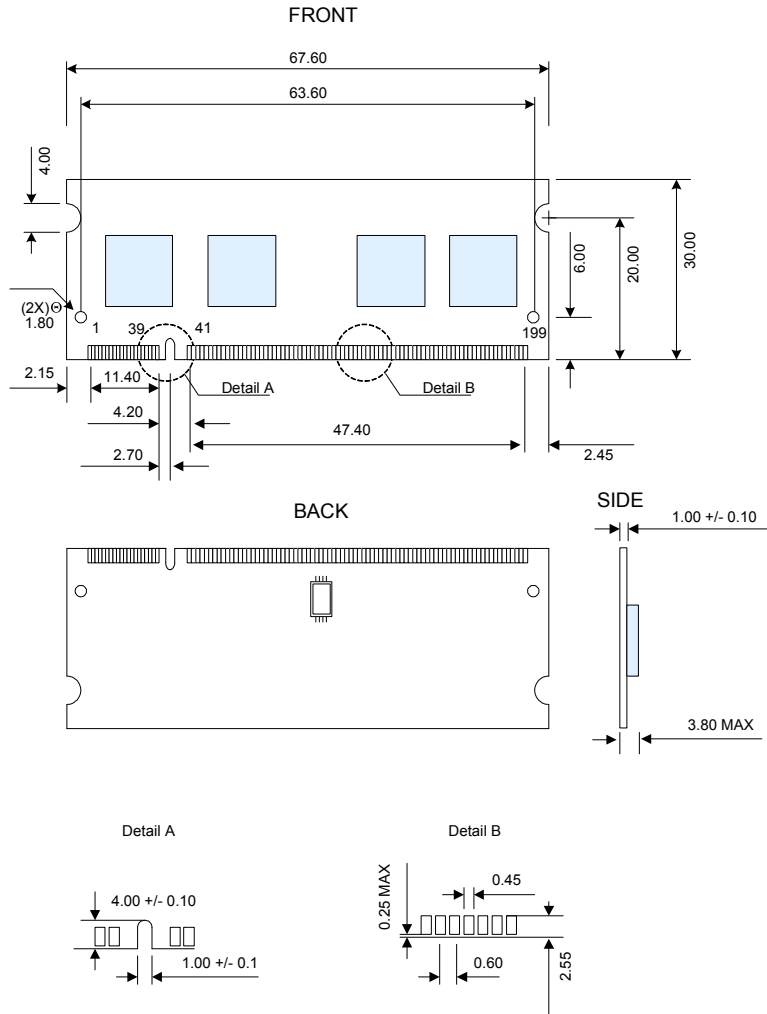
<b>Speed Grade Definition</b>										
Symbol	Parameter	-37B		-3C		-AD		-AC		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RAS</sub>	Row Active Time	45	70000	45	70000	45	70000	45	70000	ns
t <sub>RCD</sub>	RAS to CAS delay	15	-	15	-	15	-	12.5	-	ns
t <sub>RC</sub>	Row Cycle Time	60	-	60	-	60	-	57.5	-	ns
t <sub>RP</sub>	Row Precharge Time	15	-	15	-	15	-	12.5	-	ns

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



## Package Dimensions

[512MB – 1 Rank, 64Mx16 DDR2 SDRAMs]



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.  
Units: Millimeters (Inches)

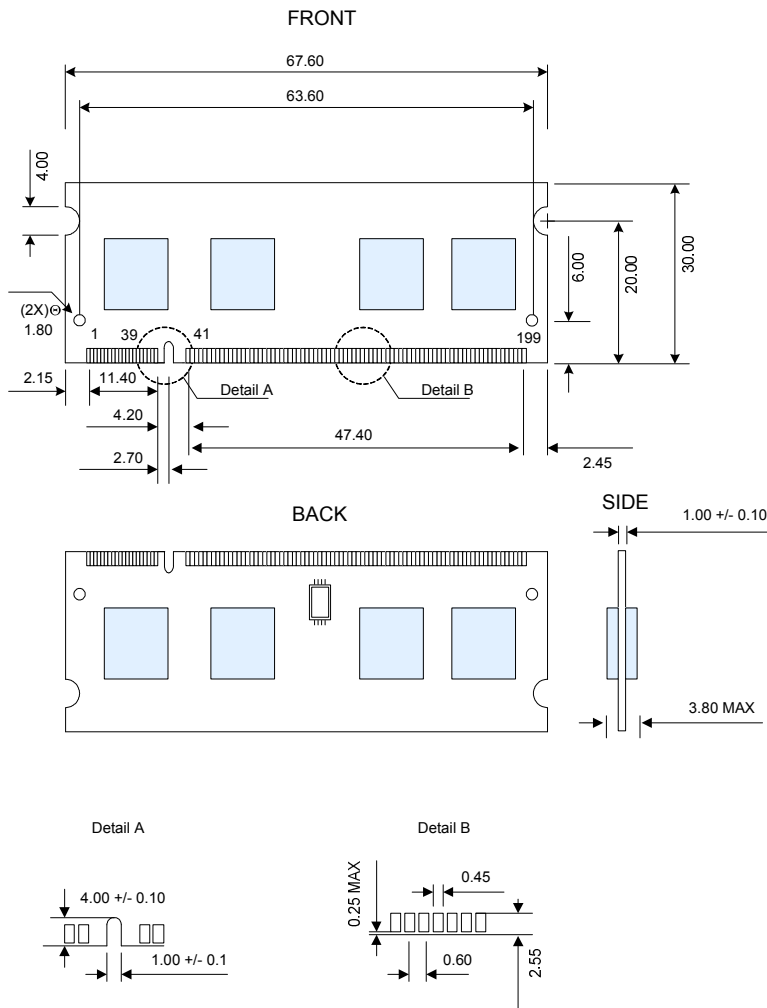
Note: Device position and scale are only for reference.

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



## Package Dimensions

[1GB – 2 Ranks, 64Mx16 DDR2 SDRAMs]



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.  
Units: Millimeters (Inches)

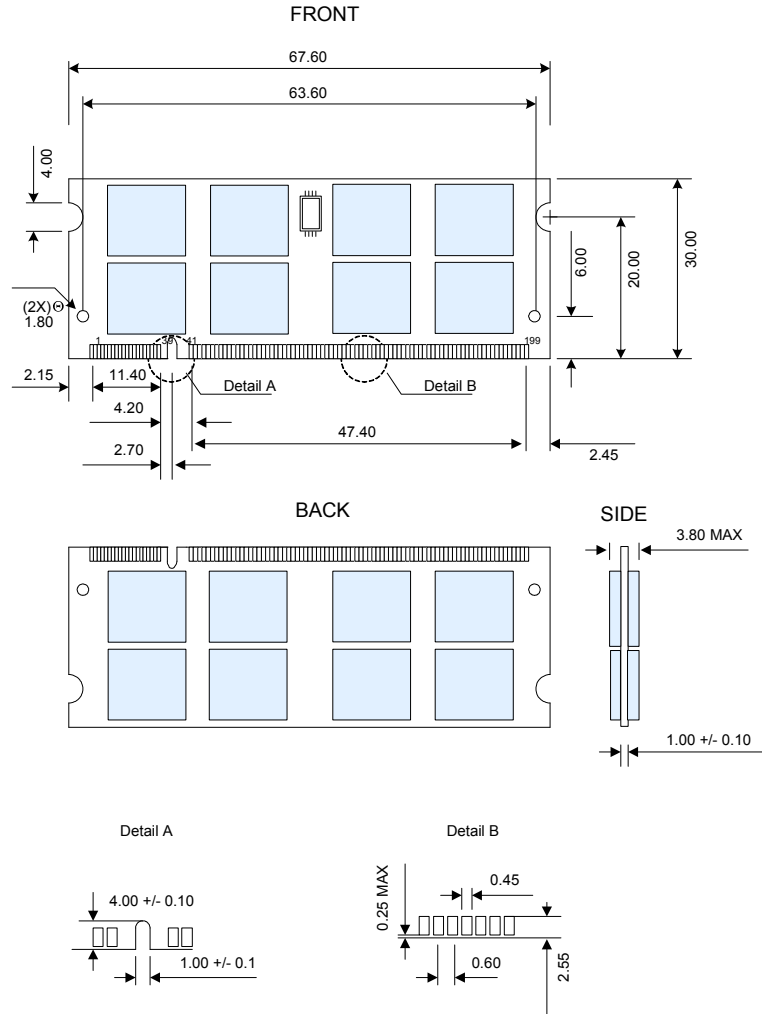
Note: Device position and scale are only for reference.

**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
**NT512T64UH4D0FS / NT1GT64UH8D0FS / NT2GT64U8HD0BS**  
**512MB: 64M x 64 / 1GB: 128M x 64 / 2GB: 256M x 64**  
**PC2-4200 / PC2-5300 / PC2-6400**  
**Unbuffered DDR2 SO-DIMM**



## Package Dimensions

[2GB – 2 Ranks, 128M x8 DDR2 SDRAMs]



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.  
Units: Millimeters (Inches)

Note: Device position and scale are only for reference.



**NT512T64UH4D0FN / NT1GT64UH8D0FN / NT2GT64U8HD0BN**  
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**Unbuffered DDR2 SO-DIMM**

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## Revision Log

Rev	Date	Modification
0.1	01/2008	Preliminary Release
1.0	01/2008	Official Release.
1.1	02/2008	Add Halogen-Free Product Information
1.2	03/2008	Update New IDD Currents, SPD and 512MB Product Information

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03/2008

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