1.0 General Description

MG87FE/L52 is a single-chip 8 bits microcontroller with the instruction sets fully compatible with industrial-standard 80C51 series microcontroller. 8K bytes flash memory and 256 bytes RAM has been embedded to provide wide field application. In-System-Programming and In-Application-Programming allow the users to download new code or data while the microcontroller sits in the application. This device executes one machine cycle in 6 clock or 12 clock cycles. MG87FE/L52 has four 8-bit I/O ports, one 4-bit I/O ports, three 16-bit timer/counters, an eight-source, four-priority-level interrupt structure, an enhanced UART, on-chip crystal oscillator.

Excellent flash-endurance, flash-retention, and code-protecting security make MG87FE/L52 as an excellent micro-controller.

2.0 Features

- 80C51 Central Processing Unit
- 8KB On-Chip program memory for program ROM, ISP ROM & IAP zone.
- ISP capability; optional 0.5K/1KB/1.5K~3.5KB ISP memory shared with 8KB flash memory.
- IAP capability; program controlled IAP memory size shared with 8KB flash memory.
- On-Chip 256 bytes scratch-pad RAM. Also, the MCU can address up to 64K bytes external memory.
- MOVC-disabling, encrypting, and locking flash memory realize security mechanism.
- Three 16-bits timer/counter, Timer2 is an up/down counter with programmable clock output on P1.0
- Eight sources, four-level-priority interrupt capability
- Enhanced UART, provides frame-error detection and hardware address-recognition
- Dual DPTR for fast-accessing of data memory
- 15 bits Watch-Dog-Timer with 8-bits pre-scaler, one-time enabled
- Low EMI: inhibits ALE emission
- Power control: Idle mode and Power-Down mode; Power-Down can be woken-up by P3.2/P3.3/P4.2/P4.3, Idle mode could be woken up by all interrupt sources.
- I/O port: 32+4 I/O ports :
  - PDIP-40 (MG87FE/L52AE or MG87FE/L52GE) has 32 I/O ports;

- PLCC-44 & PQFP-44(MG87FE/L52AP//AF, MG87FE/L52AF//GF) will have 36 I/O ports

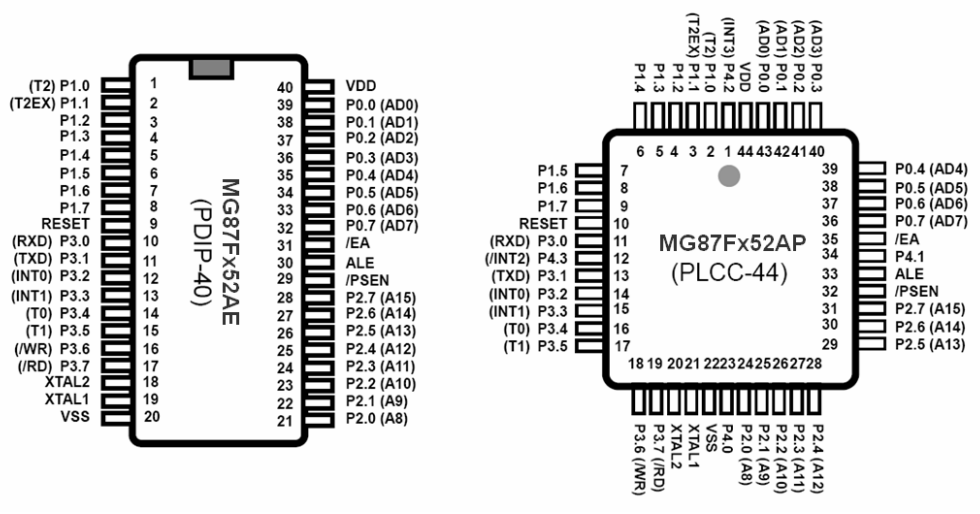
- On-Chip flash program/data memory:
  - The data endurance of the embedded flash gets over 20,000 times.
  - Greater than 100 years data retention under room temperature. (at 25℃)
- Operating Voltage:
  - 4.5V~5.5V for MG87FE52
  - 2.4V~3.6V for MG87FL52, minimum 2.7V requirement in flash write operation
  - Built-in Low-Voltage-Reset circuit
- Operating Temperature range from -40°C to +85°C.
- Maximum Operating Frequency:
  - Up to 48MHz at 12T mode or 24MHz at 6T mode, Industrial range.
- Built-in internal oscillator frequency selection with +/- 4% deviation:

	Internal oscillator frequency
1	6MHz
2	11.059MHz
3	12MHz
4	22.118MHz
5	24MHz
6	24.576MHz

- Three package types:

	Pb-free Package
PDIP-40	MG87FE/L52AE
PLCC-44	MG87FE/L52AP
PQFP-44	MG87FE/L52AF

3.0 Package & Pin assignment



3.1 Order Information

Part Number	Package Type	perating Voltage Range (x=E/L	Temperature Range	Packing
MG87Fx52AE	PDIP-40	E: 5.0V // L: 3.3V	-40℃	Tube
MG87Fx52AP	PLCC-44			
MG87Fx52AF	PQFP-44			

Example: MG87FE52AE is PDIP-40 package type & 5.0V operating voltage.
Example: MG87FL52AP is PLCC-44 package type & 3.0V operating voltage.
Example: MG87FE52AF is PQFP-44 package type & 5.0V operating voltage.

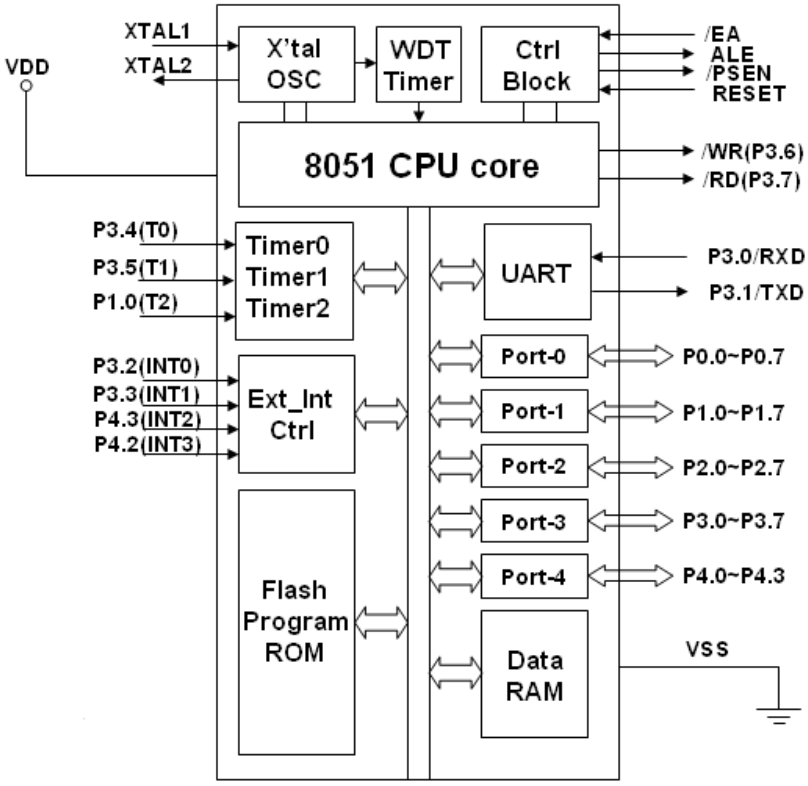
4.0 Pin description

Pin Name	Pin Number			Type	Description
	DIP-40	PLCC-44	PQFP-44		
P0.0 (AD0)	39	43	37	I/O	Port0 is an open-drain, bi-directional IO port. When *1*s are written to Port0, they become high-impedance inputs. Port0 is also multiplexed with low-order address or data bus during accesses to external program and data memory.
P0.1 (AD1)	38	42	36		
P0.2 (AD2)	37	41	35		
P0.3 (AD3)	36	40	34		
P0.4 (AD4)	35	39	33		
P0.5 (AD5)	34	38	32		
P0.6 (AD6)	33	37	31		
P0.7 (AD7)	32	36	30		
P1.0 (T2)	1	2	40	I/O	Port 1 is an 8-bit bidirectional I/O port with internal pull-ups and can be used as inputs. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. P1.0 is also used as one of event sources for timer2, or output carrier of timer2, alias T2. P1.1 is also used as one of interrupt-controlling sources for timer2, alias T2EX.
P1.1 (T2EX)	2	3	41		
P1.2	3	4	42		
P1.3	4	5	43		
P1.4	5	6	44		
P1.5	6	7	1		
P1.6	7	8	2		
P1.7	8	9	3		
P2.0 (A8)	21	24	18	I/O	Port 2 is an 8-bit bidirectional I/O port with internal pull-ups and can be used as inputs. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally pulled low will source current because of the internal pull-ups. Except being as GPIO, Port2 emits the high-order address bytes during accessing to external program and data memory.
P2.1 (A9)	22	25	19		
P2.2 (A10)	23	26	20		
P2.3 (A11)	24	27	21		
P2.4 (A12)	25	28	22		
P2.5 (A13)	26	29	23		
P2.6 (A14)	27	30	24		
P2.7 (A15)	28	31	25		

P3.0 (RXD) P3.1 (TXD) P3.2 (INT0) P3.3 (INT1) P3.4 (T0) P3.5 (T1) P3.6 (/WR) P3.7 (/RD)	10 11 12 13 14 15 16 17	11 13 14 15 16 17 18 19	5 7 8 9 10 11 12 13	I/O	Port 3 is an 8-bit bidirectional I/O port with internal pull-ups and can be used as inputs. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port3 also serves other special functions of this device. P3.0 and P3.1 act as receiver and transceiver of the data for UART function block, Alias RXD and TXD. P3.2 and P3.3 also act as external interrupt sources, alias INT0 and INT1. P3.4 and P3.5 also act as event sources for timer0 and timer1 individually, alias T0 and T1. P3.6 also acts as write signal while access to external memory, alias /WR. P3.7 also acts as read signal while access to external memory, alias /RD.
P4.0 P4.1 P4.2 (/INT3) P4.3 (/INT2)		23 34 1 12	17 28 39 6	I/O	Port4 is extended I/O ports such like Port1. It can be available only on 44L-PLCC and 44L-PQFP package. P4.2 and P4.3 also act as external interrupt sources, alias INT3 and INT2.
RESET	9	10	4	I	A high on this pin for at least two machine cycles will reset the device.
ALE	30	33	27	O	Output pulse for latching the low bytes of address during accesses to external memory.
/PSEN	29	32	26	O	The read strobe to external program memory, low active.
/EA	31	35	29	I	/EA must be kept at low to enable the device to fetch program code from external flash memory. An internal pull-up resistor has been embedded in this pin.
XTAL1	19	21	15	I	Input to the inverting oscillator amplifier.
XTAL2	18	20	14	O	Output from the inverting amplifier.

VDD	40	44	38	P	Power Supply
VSS	20	22	16	G	Ground

5.0 Block Diagram of MG87FE/L52



6.0 Special Function Registers (SFR)

F8								
F0	B							
E8	P4							
E0	ACC	WDTCR	IFD	IFADRH	IFADRL	IFMT	SCMD	ISPCR
D8								
D0	PSW							
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0	XICON							CKCON
B8	IPL	SADEN						CKCON2
B0	P3							IPH
A8	IE	SADDR						
A0	P2		AUXR1					
98	SCON	SBUF						
90	P1			*Reserved*				
88	TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	
80	P0	SP	DPL	DPH				PCON

SYMBOL	ADDR	DESCRIPTION	BIT ADDRESS & SYMBOL								INITIAL VALUE
P0	80H	Port 0									11111111B
SP	81H	Stack Pointer									00000111B
DPL	82H	Data Pointer Low									00000000B
DPH	83H	Data Pointer High									00000000B
PCON	87H	Power Control	SMOD	SMOD0	x	POF	GF1	GF0	PD	IDL	00x10000B
TCON	88H	Timer Control	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000B
TMOD	89H	Timer Mode	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00000000B
TL0	8AH	Timer Low 0									00000000B
TL1	8BH	Timer Low 1									00000000B
TH0	8CH	Timer High 0									00000000B
TH1	8DH	Timer High 1									00000000B
AUXR	8EH	Auxiliary	P0PUEN	x	x	x	x	x	x	A0	0xxxxx0B
P1	90H	Port 1							T2EX	T2	11111111B
SCON	98H	Serial Control	SM0 /FE	SM1	SM2	REN	TB8	RB8	TI	RI	00000000B
SBUF	99H	Serial Buffer									xxxxxxxxB
P2	A0H	Port 2									11111111B
AUXR1	A2H	Auxiliary 1	P1OFD	x	x	x	GF2	x	x	DPS	0xxx0xx0B
IE	A8H	Interrupt Enable	EA	x	ET2	ES	ET1	EX1	ET0	EX0	0x000000B
SADDR	A9H	Slave Address									00000000B
P3	B0H	Port 3	RD	WR	T1	T0	INT1	INT0	TXD	RXD	11111111B
IPH	B7H	Interrupt Priority High	PX3H	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H	00000000B
IPL	B8H	Interrupt Priority Low	x	x	PT2	PS	PT1	PX1	PT0	PX0	xx000000B
SADEN	B9H	Slave Address Mask									00000000B
CKCON2	BFH	Clock Control 2	OSCDR	EN6TR	XCKS5	XCKS4	XCKS3	XCKS2	XCKS1	XCKS0	xx001010B
XICON	C0H	Ext. Interrupt Control	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2	00000000B
CKCON	C7H	Clock Control	x	x	x	x	x	SCKS2	SCKS1	SCKS0	xxxxx000B
T2CON	C8H	Timer 2 Control	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL	00000000B
T2MOD	C9H	Timer2 mode	x	x	x	x	x	x	T2OE	DCEN	xxxxxx00B
RCAP2L	CAH	Timer2 Capture Low									00000000B
RCAP2H	CBH	Timer2 Capture High									00000000B
TL2	CCH	Timer Low 2									00000000B
TH2	CDH	Timer High 2									00000000B
PSW	D0H	Program Status Word	CY	AC	F0	RS1	RS0	OV	x	P	000000x0B

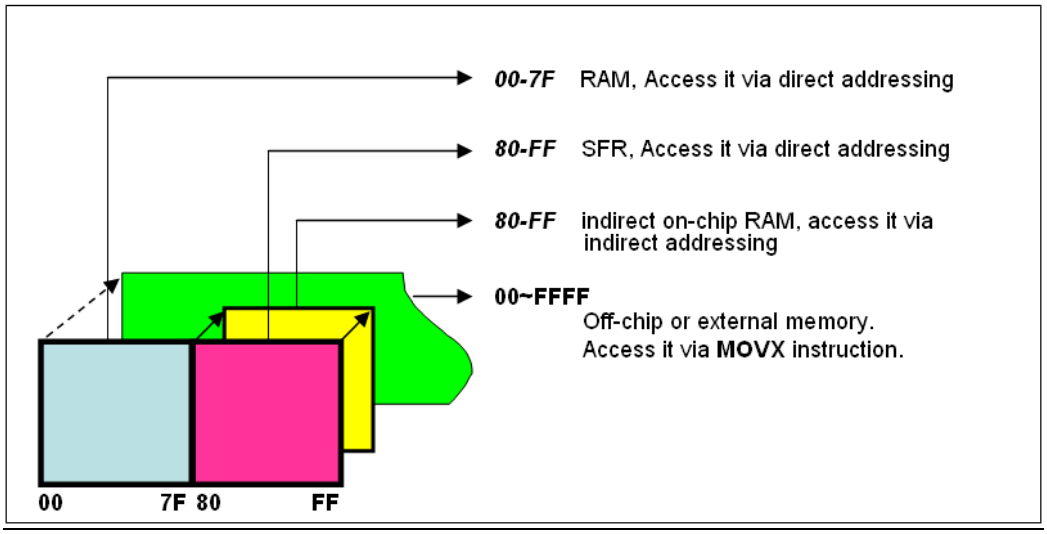
SYMBOL	ADDR	DESCRIPTION	BIT ADDRESS & SYMBOL								INITIAL VALUE
ACC	E0H	Accumulator									00000000B
WDTCR	E1H	Watch-dog-timer	WRF	—	ENW	CLW	WIDL	PS2	PS1	PS0	xx000000B
IFD	E2H	ISP Flash data									11111111B
IFADRH	E3H	ISP Flash Hi-Address									00000000B
IFADRL	E4H	ISP Flash Lo-Address									00000000B
IFMT	E5H	ISP Mode Table	—	—	—	—	—	MS2	MS1	MS0	xxxxx000B
IAPLB	Note1	IAP Low Boundary									11111111B
SCMD	E6H	ISP Serial Command									xxxxxxxxB
ISPCR	E7H	ISP Control Register	ISPEN	BS	SRST	CFAIL	—				0000xxxxB
P4	E8H	Port 4	x	x	x	x	—	—	—	—	xxxx1111B
B	F0H	B Register									00000000B

Note1: The register is addressed by IFMT and SCMD. Please refer to the IAPLB register description for more detail information.

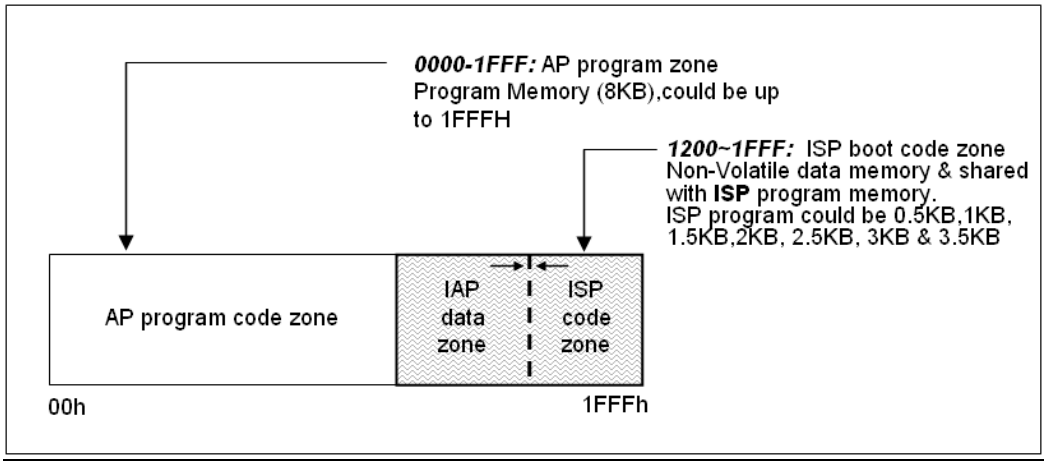
7.0 Memory: Data RAM Addressing & Program Flash ROM

7.1 Organization

Address Space for MG87FE/L52 RAM



Address Space for MG87FE/L52 Embedded Flash Memory

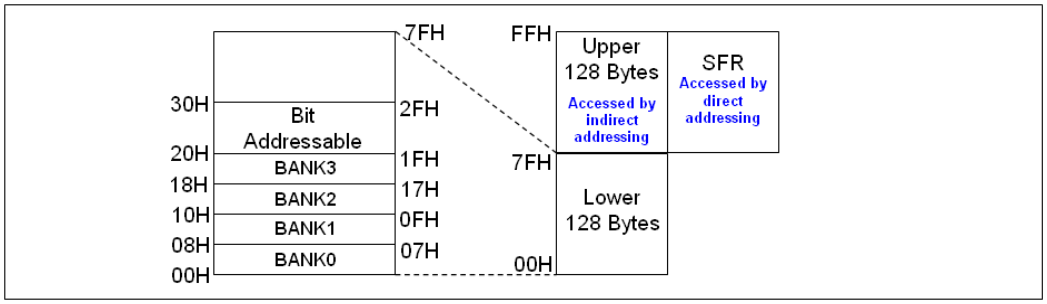


7.2 Option setting:

LOCK	ROM code lock-option. When read ROM code & always get 0xFF, PAGE-ERASE and PROGRAM is also disabled.
SB	When enabled, dump ROM code & the data will be scrambled.
MOVCL	When enabled, the MOVC operation will be disabled at external mode.
HWBS	When power-up, MCU will boot from ISP-memory if ISP-memory is configured.
HWBS2	In addition to power-up, the reset from RESET-pin will also force MCU to boot from ISP-memory if ISP-memory is configured.
EN6T	MCU 6T/12T mode, MCU will work at 6T mode when this option was enabled.
OSCDN	The gain of oscillator driving capability. Enable this option could help to reduce EMI and cause the lower power consumption. *note-1
FZWDTCR	When enabled, The WDTCR register will be initialized to its reset value only by power-on reset.

Note-1: When OSCDN option was enabled, the power consumption could be lower.

7.3 Data RAM Addressing



MG87FE/L52 has internal data RAM that is mapped to three separated segments. The lower 128 bytes of RAM, upper 128 bytes of RAM and 128 bytes Special Function Register(SFR).

Lower 128 bytes of RAM: (addresses 0x00 to 0x7F) are accessed by either direct or indirect addressing. Upper 128 bytes of RAM: (addresses 0x80 to 0xFF) are accessed only by indirect addressing (using R0 or R1). The Special Function Registers: (addresses 0x80 to 0xFF) are accessed only by direct addressing.

While the program counter is spanning over 1FFFh, the device will fetch its program code from the external memory at once ignoring the **/EA** pin status. In that case, it will never fetch the program code from the following embedded flash.

AUXR Register (0x8E)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AUXR	P0PUEN	-	-	-	-	-	-	AO

AO	= 0, ALE is emitted at a constant rate of 1/6 or 1/3 the oscillator frequency for 12T or 6T mode. = 1, ALE is active only during access to external memory for both MOVC & MOVX.
P0PUEN	= 0, P0 without pull-up resistor in open-drain mode. = 1, P0 with pull-up resistor in open-drain mode.

AUXR1 Resistor (0xA2)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
AUXR1	P10FD	-	-	-	GF2	-	-	DPS

DPS	It is used to switch one DPTR register from two available DPTRs.
GF2	General purpose flag.
P10FD	= 0, P10 has normal driving capability. = 1, P10 has fast driving.

CKCON Register (0xC7)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CKCON	-	-	-	-	-	SCKS2	SCKS1	SCKS0

SCKS2 ~ 0: System clock prescaler.

SCKS2	SCKS1	SCKS0	CLKin(System Clock)
0	0	0	OSCin
0	0	1	OSCin/2
0	1	0	OSCin/4
0	1	1	OSCin/8
1	0	0	OSCin/16
1	0	1	OSCin/32
1	1	0	OSCin/64
1	1	1	OSCin/128

CKCON2 Register (0xBF)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CKCON2	OSCDR	EN6TR	XCKS5	XCKS4	XCKS3	XCKS2	XCKS1	XCKS0

OSCDR	=0, the gain of crystal oscillator is enough for oscillation up to 48MHz. =1, the gain of crystal oscillator is reduced. It will helpful in EMI reduction. Regarding application not needing high frequency clock, it is recommended to do so.
EN6TR	=0, MG87FE/L52 will run in 12T mode; =1, MG87FE/L52 will run in 6T mode. It gets double performance than 12T. The default value of this bit is load from Option Setting “EN6T”.
XCKS5~0	Set the crystal frequency value to define the time base of ISP/IAP programming. Fill in the proper value according to XTAL1 as listed below.

XTAL1 @ 12T	XTAL1 @ 6T	XCKS5~0 setting
1MHz	0.5MHz	000000B
2MHz	1MHz	000001B
3MHz	1.5MHz	000010B
4MHz	2MHz	000011B
…….	…….	…….
45MHz	22.5MHz	101100B
46MHz	23MHz	101101B
47MHz	23.5MHz	101110B
48MHz	24MHz	101111B

The default value of XCKS=001010B for XTAL1=11MHz @ 12T.

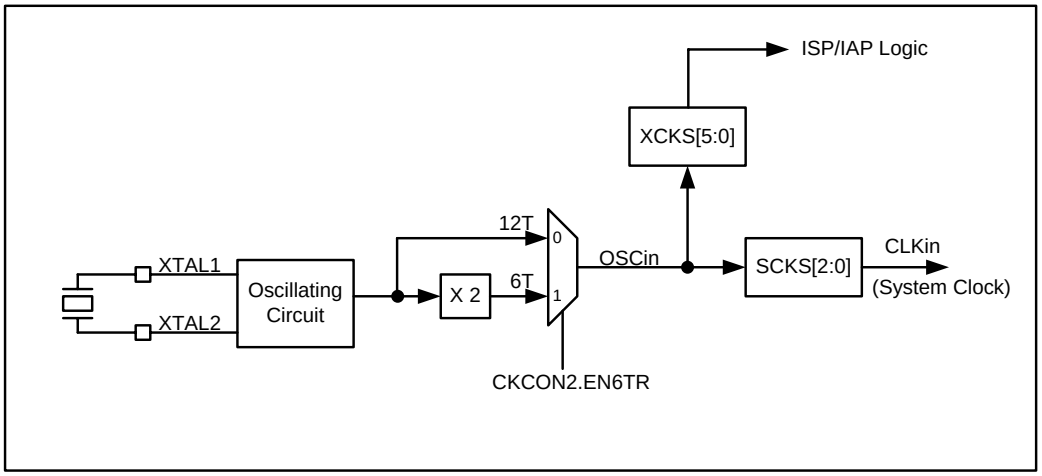


Figure 7-3-2

8.0 Timer0, Timer1 & Timer2

8.1 Timers/Counters

MG87FE/L52 has three 16-bit timers, and they are named **T0**, **T1** and **T2**. Each of them can also be used as a general event counter, which counts the transition from 1 to 0.

While **T0/T1/T2** is used as "timer" function, the time unit that used to measure the timer is *machine cycle*. A machine cycle equals to 12 or 6 oscillator periods, and depends on 12T mode or 6T mode that the user configured this device.

While **T0/T1/T2** is used as "1-0 event counter" function, the counting event is the "high-to-low transition" of primitive pin **T0/T1/T2**. In this mode, the device periodically samples the status of pin **T0/T1/T2** once for each machine cycle. Whenever the sampled result turns from 1 to 0, the device will count once on the counter. Be carefully, this kind of implementation for the counter requires the high-duty or low-duty from pin **T0/T1/T2** and must not too short compared to a machine cycle.

There are two SFR designed to configure timers **T0** and **T1**. They are **TMOD**, and **TCON**.

TMOD:

Timer-1				Timer-0			
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GATE	C//T	M1	M0	GATE	C//T	M1	M0

GATE	= 0, when TR0/1=1, Timer0/1 will be enabled. = 1, Timer0/1 *x* is enabled only while "**/INTx**" pin is high and "TR0/1" control bits is set. That x=0 or 1.
C//T	= 0, active as timer function; (Default) = 1, active as counter function.

M1	M0	Operating Mode
0	0	13-bit timer/counter for Timer0 and Timer1
0	1	16-bits timer/counter for Timer0 and Timer1
1	0	8-bits timer/counter with automatic reload for Timer0 and Timer1
1	1	(Timer 0) TL0 is 8-bit timer/counter, TH0 is locked into 8-bit timer
1	1	(Timer 1) Timer/Counter1 Stopped

TCON

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1	Timer1 overflow flag. Set by hardware when Timer/Counter overflows. Cleared by hardware when the MCU vectors to the interrupt routine, or clearing the bit in software.
TR1	Timer1 run control bit. It could be set or cleared by software.
TF0	Timer0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when the processor vectors to the interrupt routine, or clearing the bit in software.
TR0	Timer0 run control bits. It could be set or cleared by software.
IE1	Interrupt-1 edge flag. Set by hardware when external interrupt edge detected. It will be cleared when interrupt was processed.
IT1	Interrupt-1 type control bit. Set/Cleared by software to specified falling edge & low level triggered interrupt.
IE0	Interrupt-0 edge flag. Set by hardware when external interrupt edge detected. And cleared when interrupt processed.
IT0	Interrupt 0 type control bit. Set/Cleared by software to specified falling edge/low level triggered interrupt.

There are two extra SFR designed to configure timer **T2**. They are **T2MOD**, and **T2CON.**

T2MOD

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2MOD	-	-	-	-	-	-	T2OE	DCEN

T2OE	Timer-2 output enable bit. It enables Timer2 overflow rate to toggle P1.0
DCEN	Down Count Enable bit. When set, this will allow Timer2 to be configured as a down counter.

T2CON

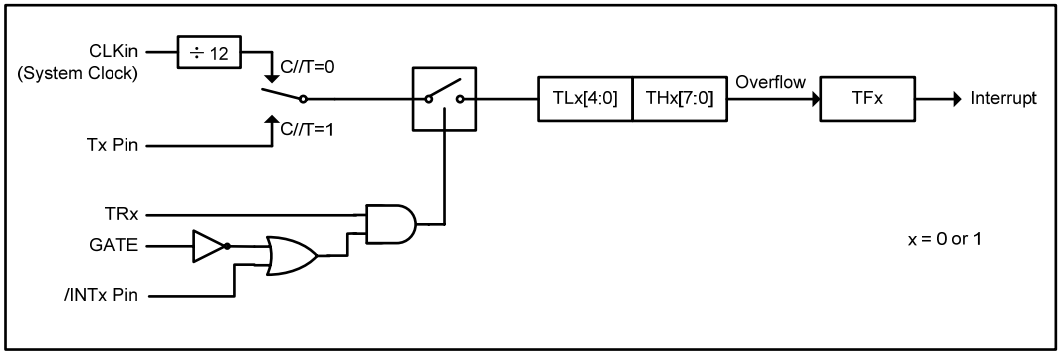
Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C//T2	CP/RL2

TF2	Timer2 overflow flag. It will be set by Timer2 overflow and must be cleared by software. TF2 will not be set when either **TCLK** or **RCLK** =1.
EXF2	Timer2 external flag. It will be set when either a capture or reload is caused by a negative transition on pin **T2EX** and **EXEN2**=1. When Timer2 interrupt is enabled, **EXF2**=1 will cause the CPU vector to the Timer2 interrupt routine. **EXF2** must be cleared by software. **EXF2** does not cause an interrupt in Auto-Reload Up-Down mode (**ARUD**).
RCLK	When this bit was set and will cause the serial port to use Timer2 overflow pulse for its receive-clock in mode-1 and mode-3. **RCLK**=0 will cause Timer1 overflow pulse to be used.
TCLK	When this bit was set and will cause the serial port to use Timer2 overflow pulse for its transmit-clock in mode-1 and mode-3. **TCLK**=0 will cause Timer1 overflow pulse to be used.
EXEN2	Timer-2 external enable flag. When set, allows a capture or reload to be occurred. As a result of a negative transition on **T2EX,** if Timer2 is not used to clock the serial port. **EXEN2**=0 will cause Timer2 to ignore events at **T2EX**.
TR2	Start/Stop control bit for Timer2.
C//T2	=0, will set as Timer function; =1, will set as external event counter.
CP/RL2	Capture/Reload flag. When set, captures will occurs on a negative transition at **T2EX** if **EXEN2**=1. When cleared, auto-reload function will occur either with Timer2 overflows or a negative transition at **T2EX** when **EXEN2**=1. When whether **TCLK** or **RCLK** is 1, this bit is ignored and the timer is forced to auto-reload on Timer2 overflow.

8.2 Timer0/T0 & Timer1/T1

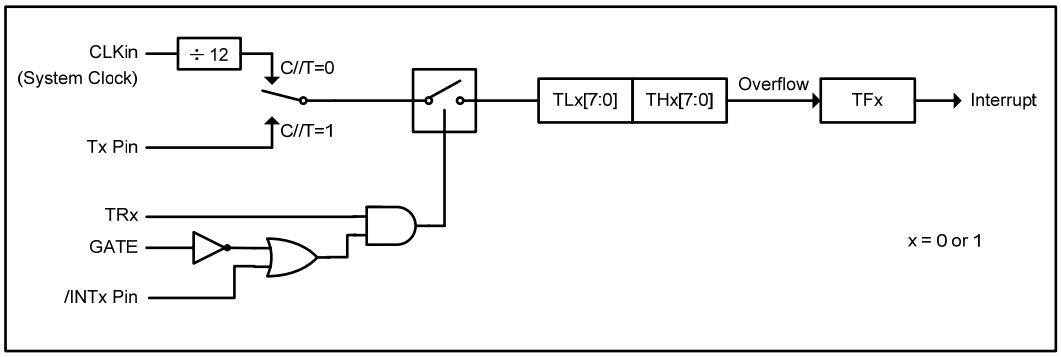
Mode 0

The timer register is configured as a 13-bits register. As when the count rolls over from all 1s to all 0s, it sets the timer interrupt flag **TFx**. The counted input is enabled to the timer when **TRx** = 1 and either GATE=0 or INTx = 1. Mode 0 operation is the same for Timer0 and Timer1.



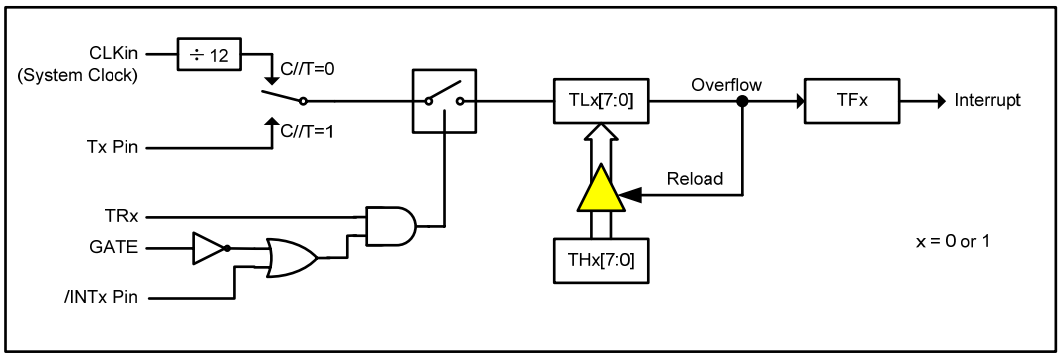
Mode 1

Mode1 is the same as Mode0, except that the timer register is being run with all 16 bits.



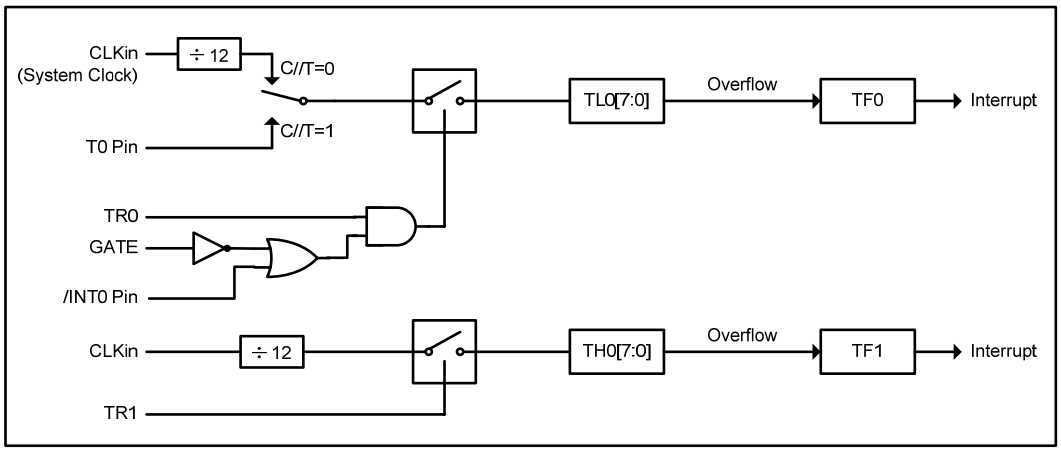
Mode 2

Mode 2 configures the timer register as an 8-bits counter (TL*x*) with automatic reload. Overflow from TL*x* does not only set TF*x*, but also reloads TL*x* with the content of TH*x*, which is determined by user's program. The reload leaves TH*x* unchanged. Mode 2 operation is the same for Timer0 and Timer1.



Mode 3

Timer 1 in Mode 3 simply holds its count, the effect is the same as setting TR1 = 1. Timer 0 in Mode 3 enables TL0 and TH0 as two separate 8-bits counters. TL0 uses the Timer0 control bits such like C/T, GATE, TR0, INT0 and TF0. TH0 is locked into a timer function (can not be external event counter) and take over the use of TR1, TF1 from Timer 1. TH0 now controls the Timer 1 interrupt.



8.3 Timer2

Timer2 is a 16-bit timer/counter which can operate as either an event timer or an event counter as selected by C//T2 in the special function register T2CON. Timer2 has four operation modes: Capture Mode(CP), Auto-Reload Up/Down Mode(ARUD), Auto-Reload Up-Only Mode(ARUO) and Baud-Rate Generator Mode(BRG).

Table 8-1. Timer-2 Mode Table

Logical OR (RCLK, TCLK)	CP/RL2	TR2	DCEN	Mode
x	x	0	x	OFF
1	x	1	0	Baud-Rate Generation
0	1	1	0	Capture
0	0	1	0	Auto-Reload Up-only
0	0	1	1	Auto-Reload Up/Down

Timer2 is also can be configured as a periodical signal generator.

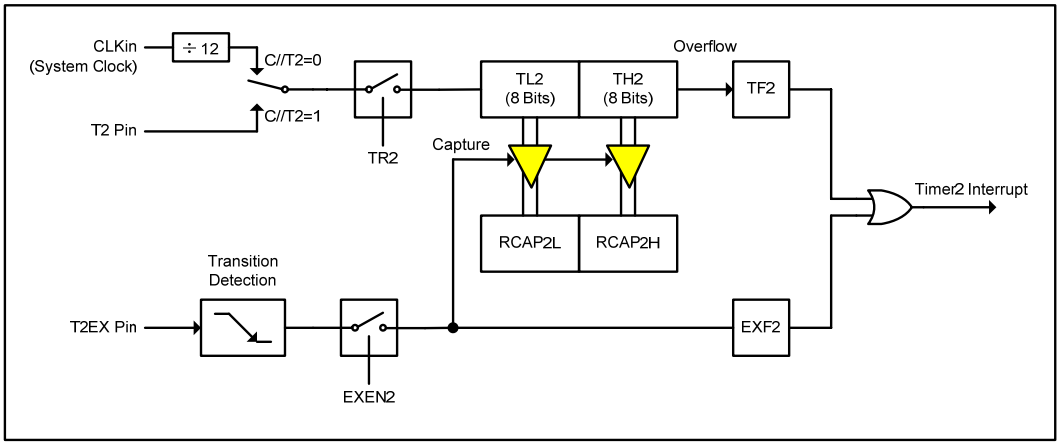
The MG87FE/L52 is able to generate a programmable clock output from P1.0. When T2OE bits is set and C//T2 bits is cleared, Timer2 overflow pulse will generate a 50% duty clock and output to P1.0. The frequency of clock-out is calculated according to the following formula.

$$\text{Clock-out Frequency} = \frac{\text{CLKin Frequency}}{4 \times (65536 - (\text{RCAP2H, RCAP2L}))}$$

In the clock-out mode, Timer2 overflowed will not generate an interrupt.

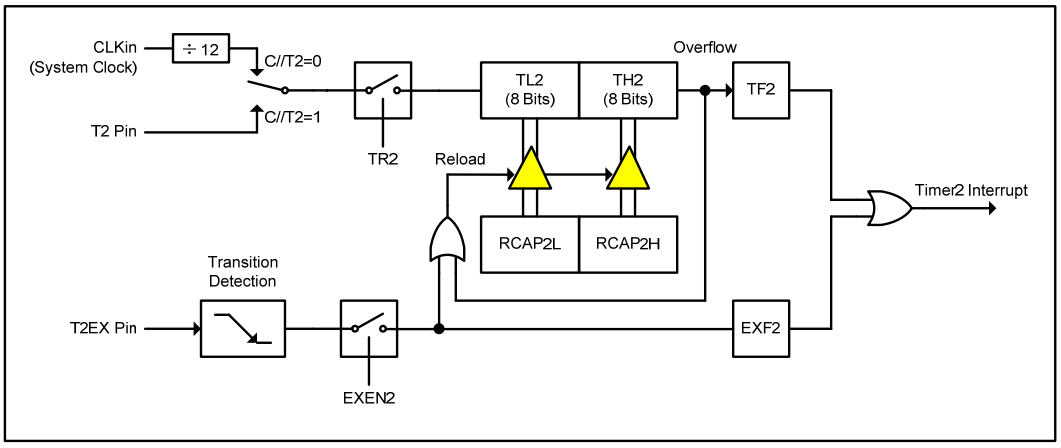
Capture Mode (CP)

In the Capture mode, Timer2 is incremented by either CLKin(System Clock) or external pin (T2) 1-to-0 transition. TR2 controls the event to timer2 and a 1-to-0 transition on T2EX pin will trigger RCAP2H and RCAP2L registers to capture the Timer2 contents onto them if EXEN2 is set. An overflow in Timer2 set TF2 flag and a 1-to-0 transition in T2EX pin sets EXF2 flag if EXEN2=1. TF2 and EXF2 is logic OR to request the interrupt service.



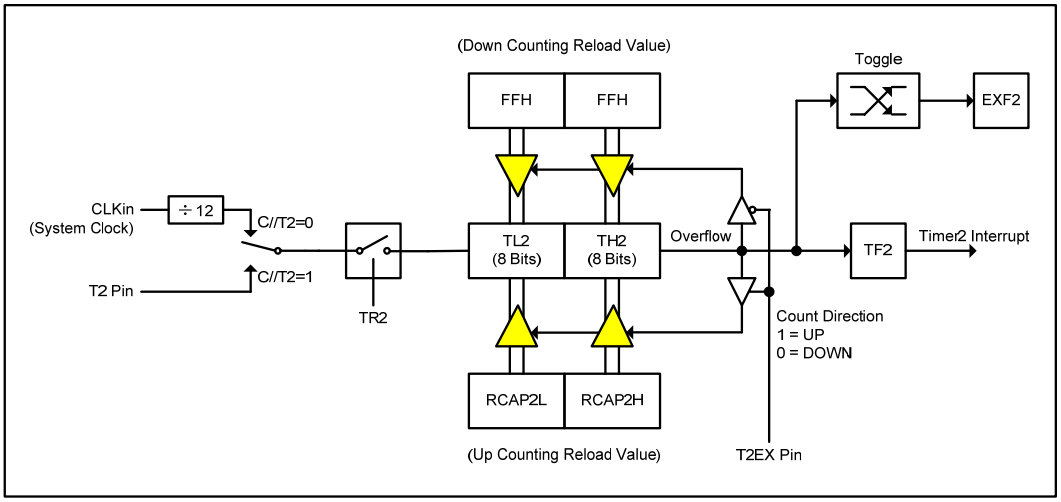
Auto-Reload Up-Only Mode (ARUO)

In ARUO mode, Timer2 can be configured to count up with a software-defined value to be reloaded. When reset is applied the DCEN =0 and CP/RL2=0, Timer2 is at ARUO mode. An overflow on Timer2 or 1-to-0 transition on T2EX pin will load RCAP2H and RCAP2L contents onto Timer2, also set TF2 and EXF2, respectively.



Auto-Reload Up-Down Mode (ARUD)

In ARUD mode, Timer2 can be configured to count up or down. When DCEN =1 and CP/RL2=0, Timer2 is at ARUD mode. The counting direction is determined by T2EX pin. If T2EX=1, counting up, otherwise counting down. An overflow on Timer2 will set TF2 and toggle EXF2. EXF2 can not generate interrupt request in this mode. If the counting direction is DOWN, the overflow loads 0xFFFF onto Timer2 and loads RCAP2H, RCAP2L contents onto Timer2 if counting direction is UP.



Baud-Rate Generator Mode (BRG)

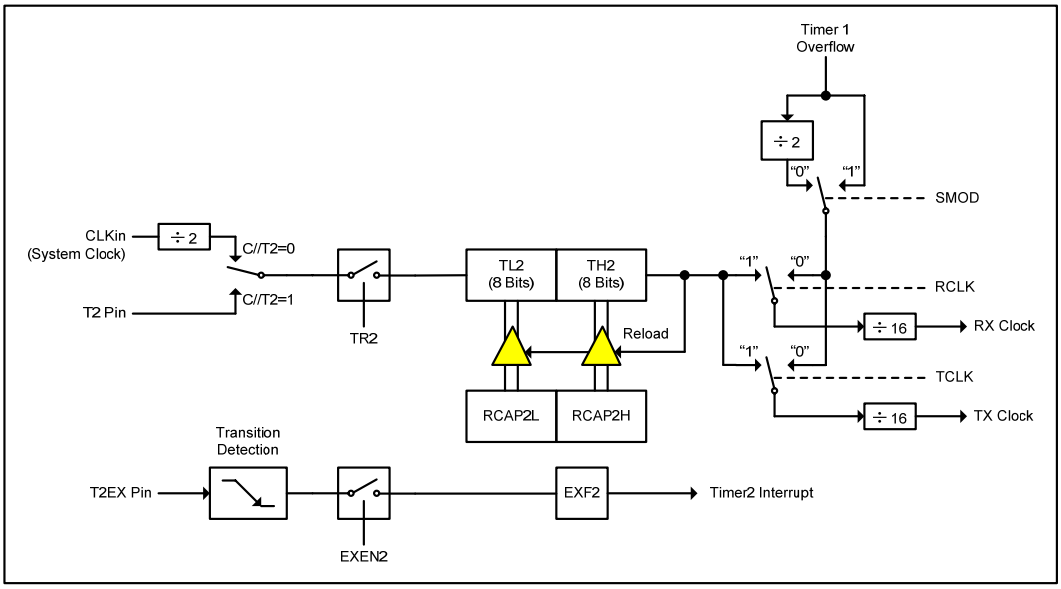
Timer2 can be configured to generate various baud rate. Bit TCLK and/or RCLK in T2CON allow the serial port transmit and receive baud rates to be derived from either Timer1 or Timer2. When TCLK=0, Timer1 is used as the serial port transmit baud rate generator. When TCLK=1, Timer2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated from Timer1 and the other from Timer2.

In BRG mode, Timer2 is operated very like auto-reload up-only mode except that the T2EX pin can not control reload. An overflow on Timer2 will load RCAP2H, RCAP2L contents onto Timer2 but TF2 will not be set. A 1-to-0 transition on T2EX pin can set EXF2 to request interrupt service if EXEN2=1.

The baud rate in UART Mode-1 and Mode-3 are determined by Timer2's overflow rate given below:

$$\text{Mode 1, 3 Baud Rate} = \frac{\text{Timer2 overflow rate}}{16} \text{ ; counting T2EX pin}$$

$$\text{Mode 1, 3 Baud Rate} = \frac{\text{CLKin Frequency}}{32 \times (65536 - (\text{RCAP2H, RCAP2L}))} \text{ ; as the timer}$$



8.4 UART (Universal Asynchronous Receiver & Transmitter interface)

The serial port of MG87FE/L52 support full-duplex transmission. It can transmit and receive simultaneously. The serial port receive and transmit share the same SFR – SBUF, but actually there is two SBUFs in the chip, one is for transmitter and the other is for receiver. The serial port could be operated in 4 different modes.

Mode 0

Serial data enters and exits through RXD(P3.0) and TXD(P3.1) outputs the shift clock. 8-bits are transmitted/received with LSB first. The baud rate is fixed at 1/12 the frequency of system clock (CLKin).

$$\text{Mode 0 Baud Rate} = \frac{\text{CLKin Frequency}}{12}$$

Mode1

10 bits are transmitted through TXD or received through RXD. The frame data includes a start bit(0), 8 data bits and a stop bit(1). One receive, the stop bit goes into RB8 in SFR – SCON. The baud rate is variable.

$$\text{Mode 1 Baud Rate} = \frac{2^{\text{SMOD}}}{32} \times (\text{Timer1 overflow rate})$$

$$\text{or} = \frac{\text{Timer2 overflow rate}}{16}$$

Mode2

11 bits are transmitted through TXD or received through RXD. The frame data includes a start bit(0), 8 data bits, a programmable 9th bit and a stop bit(1). On transmit, the 9th data bit comes from TB8 in SCON. On receive, the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the frequency of system clock (CLKin).

$$\text{Mode 2 Baud Rate} = \frac{2^{SMOD}}{64} \text{ X (CLKin Frequency)}$$

Mode3

Mode 3 is the same as mode 2 except the baud rate is variable.

$$\text{Mode 3 Baud Rate} = \frac{2^{SMOD}}{32} \text{ X (Timer1 overflow rate)}$$

$$\text{or} = \frac{\text{Timer2 overflow rate}}{16}$$

In all four modes, transmission is initiated by any instruction that use SBUF as a destination register. Reception is initiated in mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit with 1-to-0 transition if REN = 1.

Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware comparison circuit. This feature improves the overhead of software by eliminating the need in examine every incoming address. This feature is enabled by setting the SM2 bit in SCON. In mode2 and mode3, the receive interrupt flag(RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. These two modes require the 9^{th} received bit is a 1 to indicate that received information is an address and not the data byte.

In mode1, the RI flag will be set if SM2 is enabled and a valid stop bit is received which the stop bit follows the 8 address bits and the information is either a Given or Broadcast address.
In mode 0, SM2 is ignored.

Frame Error Detection

A missing bit in stop bit will set the FE bit in the SCON register. The FE bit shares the SCON bit 7 with SM0 and its actual function for SCON.7 is determined by SMOD0(PCON.6). If SMOD0 is set, SCON.7 functions as FE, otherwise functions as SM0. When used as FE bit, it can only be cleared by software.

SCON register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

FE	Frame Error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 (PCON.6) bit must be set to enable access to the FE bits.

SM0, SM1: Serial Port Mode bit 0/1, it is enabled to access by clearing SMOD0.

SM0	SM1	Description	Baud Rate
0	0	8-bit shift register	CLKin/12
0	1	8-bit UART	Variable
1	0	9-bit UART	CLKin/64 or CLKin/32
1	1	9-bit UART	Variable

*** Please refer to page-14 figure 7-3-2 for "CLKin" signal.**

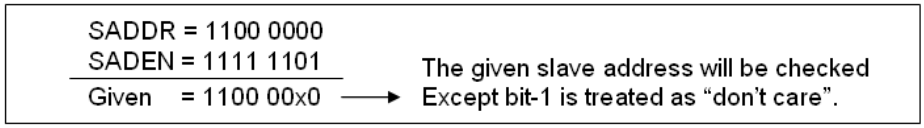
SM2	Enable the automatic address recognition feature in mode 2 and 3. If SM2=1, RI will not be set unless the received 9th data bit is 1, indicating an address, and the received byte is a given or Broadcast address. In mode1, if SM2=1 then RI will not be set unless a valid stop bit was received, and the received byte is a Given or Broadcast address.
REN	When set will enable serial reception.
TB8	The 9th data bit which will be transmitted in mode 2 and 3.
RB8	In mode 2 and 3, the received 9th data bit will go into this bit.
TI	Transmit interrupt flag.
RI	Receive interrupt flag.

SBUF register

It is used as the buffer register in transmission and reception.

SADDR register & SADEN register

SADDR register is combined with SADEN register to form Given/Broadcast Address for automatic address recognition. In fact, SADEN functions as the “mask” register for SADDR register. The following is the example for it.



The Broadcast-Address for each slave is created by taking the logical OR of SADDR and SADEN. Zero in this result is considered as “don’t care”. Upon reset, SADDR and SADEN are loaded with all 0s. This produces a Given-Address of all “don’t care” and a Broadcast Address of all “don’t care”. This disables the automatic address detection feature.

9.0 RESET & Power Saving Mode

9.1 RESET

The RESET pin is used to reset this device. It is connected into the device to a Schmitt Trigger buffer to get excellent noise immunity. Any positive pulse from RESET pin must be kept at least two-machine cycle, or the device cannot be reset.

9.2 Power saving mode

There are two kinds of power saving modes which are selectable to drive the MG87FL/E52 to enter power-saving mode.

9.2.1 Idle Mode

The user can set the bits **PCON.0** to drive this chip entering IDLE mode.
In the IDLE mode, the internal clock is gated off to the CPU, but not to the interrupt, timer and serial port functions.

There are two ways to release from the idle mode. Activation of any enabled interrupt sources will cause **PCON.0** to be cleared by hardware to terminating the idle mode. The interrupt will be serviced and following RETI, the next instruction to be executed will be performed right after the instruction that causes the device entering the idle mode. Another way to wake-up from idle is to pull **RESET** pin high to generate internal hardware reset.

9.2.2 Power-Down Mode

The user can set the bits **PCON.1** to drive this chip entering Power-Down mode.

In the Power-Down mode, the on-chip oscillator is stopped. The contents of on-chip RAM and SFRs are maintained.

The Power-Down mode can be woken-up by either hardware reset or **/INT0**, **/INT1**, **/INT2** and **/INT3** external interrupts. When it is woken-up by **RESET** pin, the program will execute from the address 0x0000, and be carefully to keep **RESET** pin active for at least 10ms in order to get a stable clock while waking up this chip from Power-Down mode. If it was woken-up from I/O, the program will jump to related interrupt vector service routine. To use I/O wake-up, interrupt-related registers have to be programmed accurately before power-down is entered. ***User should be noted to add at least one "NOP" instruction subsequent to the power-down instruction if I/O waken-up is used.***

Pin Status in IDLE Mode and POWER-DOWN Mode

Mode	Program Memory	ALE	PSEN	Port0	Port1	Port2	Port3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-Down	Internal	0	0	Data	Data	Data	Data
Power-Down	External	0	0	Float	Data	Data	Data

9.3 Power-On Flag (POF)

The register bit in PCON.4 is set only by power-on action. System RESET from Watch-Dog timer, software RESET and RESET pin can not set POF. It only can be cleared by firmware.

10.0 Interrupt Structure

Interrupt Enable (IE) register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0

EA	Global interrupt enable flag when set. When cleared & all interrupts were disabled.
-	Reserved.
ET2	When set, enable Timer-2 interrupt.
ES	When set, enable the serial port interrupt.
ET1	When set, enable Timer-1 interrupt.
EX1	When set, enable external interrupt-1.
ET0	When set, enable Timer-0 interrupt.
EX0	When set, enable external interrupt-0.

Interrupt Priority Low (IPL) Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL	-	-	PT2	PS	PT1	PX1	PT0	PX0

PT2	If set, Set priority for timer2 interrupt higher
PS	If set, Set priority for serial port interrupt higher
PT1	If set, Set priority for timer1 interrupt higher
PX1	If set, Set priority for external interrupt 1 higher
PT0	If set, Set priority for timer0 interrupt higher
PX0	If set, Set priority for external interrupt 0 higher

Interrupt Priority High (IPH) Register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPH	PX3H	PX2H	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

PX3H	If set, Set priority for external interrupt 3 highest
PX2H	If set, Set priority for external interrupt 2 highest
PT2H	If set, Set priority for timer2 interrupt highest
PSH	If set, Set priority for serial port interrupt highest
PT1H	If set, Set priority for timer1 interrupt highest
PX1H	If set, Set priority for external interrupt 1 highest

PT0H	If set, Set priority for timer0 interrupt highest
PX0H	If set, Set priority for external interrupt 0 highest

IPL (or XICON) and IPH are combined to form 4-level priority interrupt as the following table.

(IPH.x, IPL.x)	Priority Level
1,1	1 (highest)
1,0	2
0,1	3
0,0	4

External Interrupt Control (XICON) register

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XICON	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3	If set, Set priority for external interrupt 3 higher.
EX3	If set, Enables external interrupt 3.
IE3	Interrupt 3 Edge flag. Sets by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT3	Interrupt 3 type control bits. Set/Cleared by software to specified falling edge/low level triggered interrupt.
PX2	If set, Set priority for external interrupt 3 higher.
EX2	If set, enables external interrupt 2.
IE2	Interrupt 2 Edge flag. Sets by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT2	Interrupt 2 types control bits. Set/Cleared by software to specify falling edge/low level triggered interrupt.

There are eight interrupt sources available in MG87FE/L52. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the SFR named **IE**. This register also contains a global disable bit(EA), which can be cleared to disable all interrupts at once.

Each interrupt source has two corresponding bits to represent its priority. One is located in SFR named IPH and the other in IPL register. Higher-priority interrupt will be not interrupted by lower-priority interrupt request. If two interrupt requests of different priority levels are received simultaneously, the request of higher priority is serviced. If interrupt requests of the same priority

level are received simultaneously, an internal polling sequence determine which request is serviced. The following table shows the internal polling sequence in the same priority level and the interrupt vector address.

Source	Vector address	Priority within level
External interrupt 0	03H	1 (highest)
Timer 0	0BH	2
External interrupt 1	13H	3
Timer1	1BH	4
Serial Port	23H	5
Timer2	2BH	6
External interrupt 2	33H	7
External interrupt 3	3BH	8

The external interrupt /INT0, /INT1, /INT2 and /INT3 can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in register TCON, IT2 and IT3 and XICON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON, IE2 and IE3 in XICON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to *only if the interrupt was transition –activated*, then the external requesting source is what controls the request flag, rather than the on-chip hardware.

The Timer0 and Timer1 interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers in most cases. When a timer interrupt was generated, the flag that generated & it was cleared by the on-chip hardware when the service routine is vectored to.

The serial port interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. The service routine should check RI and TI to determine which one request service and it will be cleared by software.

The timer2 interrupt is generated by the logical OR of TF2 and EXF2. Just the same as serial port, neither of these flags is cleared by hardware when the service routine is vectored to.

All of the bits that generate interrupts can be set or cleared by software, with the same result as though it had been set or cleared by hardware. In other words, interrupts can be generated or pending interrupts can be canceled in software.

11.0 Watch-Dog-Timer

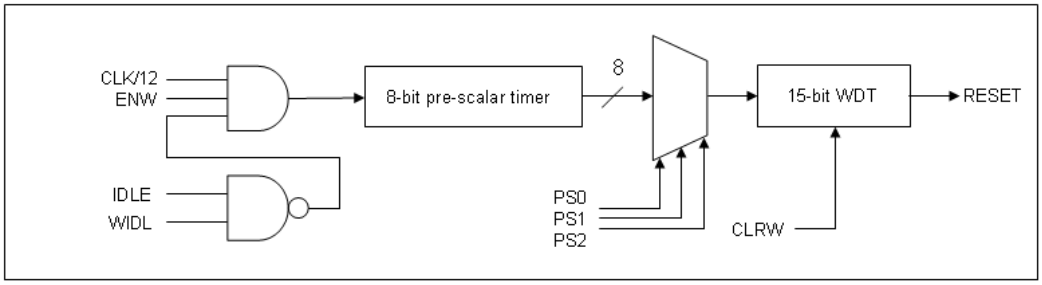
WDTCR (Watch-Dog-Timer Control Register)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WDTCR	WRF	-	ENW	CLRW	WIDL	PS2	PS1	PS0

WRF	Watch-Dog timer overflow flag. Set by hardware when Watch-Dog timer overflow.
ENW	Enable WDT while it is set. ENW can not be cleared by firmware.
CLRW	Clear WDT to re-count while it is set. Hardware will automatically clear this bit.
WIDL	Set this bit to stop WDT counting and disable WDT reset generating when uC is in idle mode.

PS2 ~ PS1: select the pre-scaler output.

PS2	PS1	PS0	Pre-scaler value
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256



12 In-System-Programming & In-Application Programmable

12.0 In-System-Programming (ISP)

In MG87FE/L52, 8K bytes flash ROM is divided into three sections. The first partition named AP-memory is the space for storing user's application program code. The next one named LD-memory is the space which ISP program is loaded. The third one named OR-memory space has option registers here.

Three-level code protection from read-out on the programmer is implemented in this chip. The first-level is LOCK bit. If LOCK bit was enabled (programming to 0), the data readout on the programmer will always be 0xFFh. SCRAMBLE bit is the second level protection. Enabling SCAMBLE bit encrypts the data readout on the programmer. The third level protection is MOVCL. Enabling MOVCL inhibits MOVC operation in the condition that the execution is from external fetch but the target code byte is in internal flash memory.

IFD (ISP Flash Data register)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IFD	Data							

IFD is the data port register for ISP/IAP operation. The data in IFD will be written into the desired address in operating ISP/IAP write and it is the data window of readout in operating ISP/IAP read.

If IMFT is indexed on IAPLB access, read/write IFD through SCMD flow will access the register content of IAPLB.

IFADRH (ISP Address for High-byte addressing)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IFADRH	Address							

IFADRH is the high-byte address port for all ISP/IAP modes.

IFADRL (ISP Address for Low-byte addressing)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IFADRL	Address							

IFADRL is the low byte address port for all ISP/IAP modes. In page erase operation, it is ignored.

IFMT (ISP Flash Mode Table)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IFMT	Reserved					Mode Selection		

B7~B3 : Reserved

Mode Selection :

B2	B1	B0	Mode
0	0	0	Standby
0	0	1	AP-memory read
0	1	0	AP-memory program
0	1	1	AP-memory page erase
1	0	0	IAPLB write
1	0	1	IAPLB read

IAPLB (IAP Flash Mode Table)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IAPLB	Data							

B7~B0 : The IAPLB determines the IAP-memory lower boundary. Since a Flash page has 512 bytes, the IAPLB must be an even number.

To read IAPLB, MCU need to define the IMFT for mode selection on IAPLB Read and set ISPCR.ISPEN. And then write 0x46h & 0xB9h sequentially into SCMD. The IAPLB content is available in IFD. If write IAPLB, MCU will put new IAPLB setting value in IFD firstly. And then select IMFT, enable ISPCR.ISPEN and then set SCMD. The IAPLB content has already finished the updated sequence.

The range of the IAP-memory is determined by IAPLB and the ISP start-address was listed below.

IAP lower boundary = IAPLB x 256, and

IAP higher boundary = ISP start address – 1.

For example, if IAPLB=0x12 and ISP start address is 0x1C00, then the IAP-memory range was located at 0x1200 ~ 0x1BFF.

Additional attention point, the IAP low boundary address must not be higher than ISP start address.

SCMD (Sequential Command Data register)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCMD	CMD							

SCMD is the command port for triggering ISP/IAP/IAPLB activity. If SCMD is filled with sequential 0x46h, 0xB9h and if ISPCR.7 = 1, ISP activity will be triggered.

ISPCR (ISP Control Register)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ISPCR	ISPEN	SWBS	SWRST	CFAIL	---			

ISPEN	= 0, Global disable all ISP/IAP program/erase/read function. = 1, Enable ISP/IAP program/erase/read function.
SWBS	= 0, Boot from main-memory after reset. = 1, Boot from ISP memory after reset.
SWRST	= 0, No operation = 1, Generate software system reset. It will be cleared by hardware automatically.
CFAIL	= 0, The last ISP/IAP command has finished successfully. = 1, The last ISP/IAP command fails. It could be caused since the access of flash memory was inhibited.
B3~B0	Reserved

12.1 In-Application-Programmable (IAP)

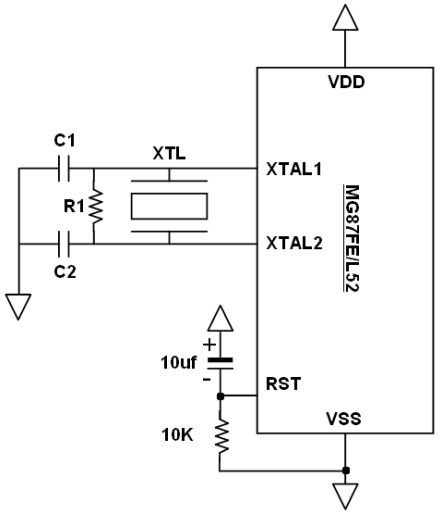
The flash memory between IAPLB and ISP start address could be defined as data flash memory and can be accessed by the ISP operation in field application. The size of IAP flash memory is variable. It is defined by IAPLB.

When the MG87FE/L52 was boots from LD-memory, AP-memory and data flash memory are opened for ISP operation.

13 System Oscillator

13.1 External crystal mode

MG87FE/L52 built-in two kinds of oscillator for MCU system clock operating. The first one is crystal oscillator & it can support 6MHz ~ 48MHz/12T or 6MHz ~ 24MHz/6T with external crystal component. Please refer to the figure 13-1.



VDD=5/3V	XTL	C1	C2	R1 (ohm)
1	6MHz	30p/15p	30p/15p	NC
2	11.059MHz	20p/10p	20p/10p	NC
3	12MHz			NC
4	22.118MHz	12p/7p	12p/7p	NC
5	24MHz			NC
6	24.576MHz			NC
7	26~30MHz	8p/8p	8p/8p	6.8K
8	31~35MHz	8p/8p	8p/8p	5.1K

13.2 Internal RC-oscillator

MG87FE/L52 had special designed & built-in internal RC-oscillator with frequency drifts that just under 4%. The operating temperature range is between -40 ~ 85°C & under its operating voltage is 4.5V ~ 5.5V or 2.7V ~ 3.6V. By the way, user could save an external crystal & just keep XTAL1 & XTAL2 pins at floating status.

The internal oscillator could support 6MHz, 11.059MHz, 12MHz, 22.118MHz, 24MHz & 24.576MHz. User can select & trim requested frequency from Megawin programming tool “8051writer U1”.

14.0 Absolute Maximum Rating

MG87FE52: (5.0V application)

Parameter	Rating	Unit
Ambient temperature under bias	-55 ~ +125	°C
Storage temperature	-65 ~ + 150	°C
Voltage on any Port I/O Pin or RST with respect to Ground	-0.5 ~ VDD + 0.5	V
Voltage on VDD with respect to Ground	-0.5 ~ +6.0	V
Maximum total current through VDD and Ground	400	mA
Maximum output current sunk by any Port pin	40	mA

*Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

MG87FL52: (3.3V application)

Parameter	Rating	Unit
Ambient temperature under bias	-55 ~ +125	°C
Storage temperature	-65 ~ + 150	°C
Voltage on any Port I/O Pin or RST with respect to Ground	-0.3 ~ VDD + 0.3	V
Voltage on VDD with respect to Ground	-0.3 ~ +4.2	V
Maximum total current through VDD and Ground	400	mA
Maximum output current sunk by any Port pin	40	mA

*Note: stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

15 DC Characteristics

15.1 MG87FE52 DC Characteristics

VDD = 5.0V, VSS = 0V, TA = 25 ℃ and 12 clocks per machine cycle, unless otherwise specified

Symbol	Parameter	Test Condition	Limits			Unit
			min	typ	max	
V_{IH1}	Input High voltage (Ports 0, 1, 2, 3, 4)		2.0			V
V_{IH2}	Input High voltage (RESET)		3.5			V
V_{IL1}	Input Low voltage (Ports 0, 1, 2, 3, 4)				0.8	V
V_{IL2}	Input Low voltage (RESET)				1.6	V
I_{IH}	Input High Leakage current (Ports 0, 1, 2, 3, 4)	V_{PIN} = VDD		0	10	uA
I_{IL}	Logic 0 input current (Ports 1, 2, 3, 4)	V_{PIN} = 0.4V		20	50	uA
I_{H2L}	Logic 1 to 0 input transition current (Ports 1, 2, 3, 4)	V_{PIN} =1.8V		250	500	uA
I_{OH1}	Output High current (Ports 1, 2, 3, 4)	V_{PIN} =2.4V	150	220		uA
I_{OH2}	Output High current (ALE, PSEN)	V_{PIN} =2.4V	12			mA
I_{OL1}	Output Low current (Ports 0, 1, 2, 3, 4)	V_{PIN} =0.4V	12			mA
I_{OL2}	Output Low current (ALE, PSEN)	V_{PIN} =0.4V	12			mA
I_{OP}	Operating current	Fosc= 12MHz		8	16	mA
		Fosc= 24MHz		10	20	
I_{IDLE}	Idle mode current	Fosc= 12MHz		4	8	mA
		Fosc= 24MHz		5	10	
I_{PD}	Power down current			1	10	uA
R_{RST}	Internal reset pull-down resistance			100		Kohm

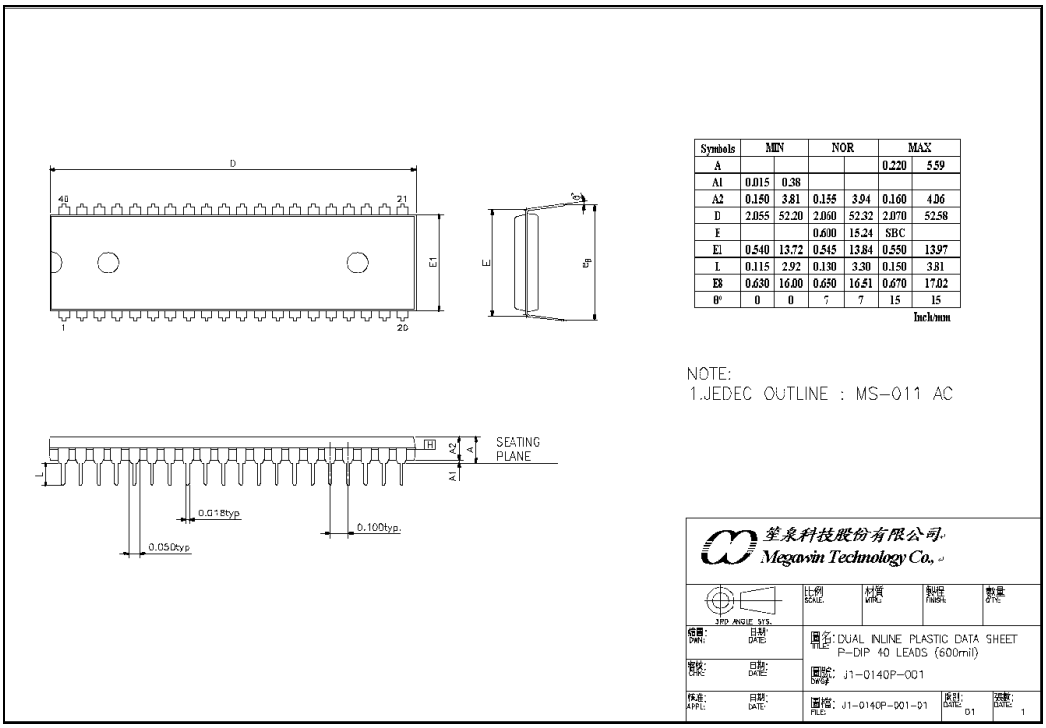
15.2 MG87FL52 DC Characteristics

VDD = 3.3V, VSS = 0V, TA = 25 ℃ and 12 clocks per machine cycle, unless otherwise specified

Symbol	Parameter	Test Condition	Limits			Unit
			min	typ	max	
V_{IH1}	Input High voltage (Ports 0, 1, 2, 3, 4)		2.0			V
V_{IH2}	Input High voltage (RESET)		2.8			V
V_{IL1}	Input Low voltage (Ports 0, 1, 2, 3, 4)				0.8	V
V_{IL2}	Input Low voltage (RESET)				1.5	V
I_{IH}	Input High Leakage current (Ports 0, 1, 2, 3, 4)	V_{PIN} = VDD		0	10	uA
I_{IL}	Logic 0 input current (Ports 1, 2, 3, 4)	V_{PIN} = 0.4V		7	30	uA
I_{H2L}	Logic 1 to 0 input transition current (Ports 1, 2, 3, 4)	V_{PIN} =1.8V		100	250	uA
I_{OH1}	Output High current (Ports 1, 2, 3, 4)	V_{PIN} =2.4V	40	70		uA
I_{OH2}	Output High current (ALE, PSEN)	V_{PIN} =2.4V	4			mA
I_{OL1}	Output Low current (Ports 0, 1, 2, 3, 4)	V_{PIN} =0.4V	8			mA
I_{OL2}	Output Low current (ALE, PSEN)	V_{PIN} =0.4V	8			mA
I_{OP}	Operating current	Fosc = 12MHz		6	12	mA
		Fosc = 24MHz		8	16	
I_{IDLE}	Idle mode current	Fosc = 12MHz		2	4	mA
		Fosc = 24MHz		2.5	5	
I_{PD}	Power down current			1	5	uA
R_{RST}	Internal reset pull-down resistance			200		Kohm

16 Package Dimension

16.1 40-Pin PDIP Package (MG87FE/L52AE)

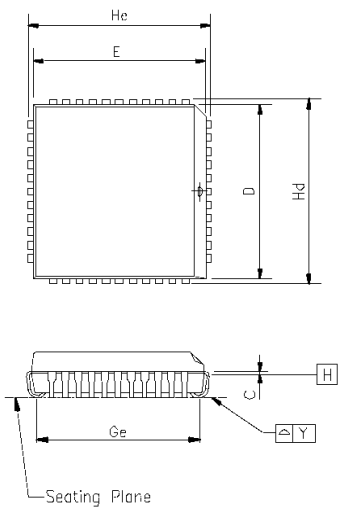


Symbols	MIN		NOR		MAX	
A					0.220	5.59
A1	0.015	0.38				
A2	0.150	3.81	0.155	3.94	0.160	4.06
D	2.055	52.20	2.060	52.32	2.070	52.58
E			0.600	15.24	SBC	
E1	0.540	13.72	0.545	13.84	0.550	13.97
L	0.115	2.92	0.130	3.30	0.150	3.81
E8	0.630	16.00	0.650	16.51	0.670	17.02
θ°	0	0	7	7	15	15

Inch/mm

NOTE:
1.JEDEC OUTLINE : MS-011 AC

16.2 44-Pin PLCC Package (MG87FE/L52AP)



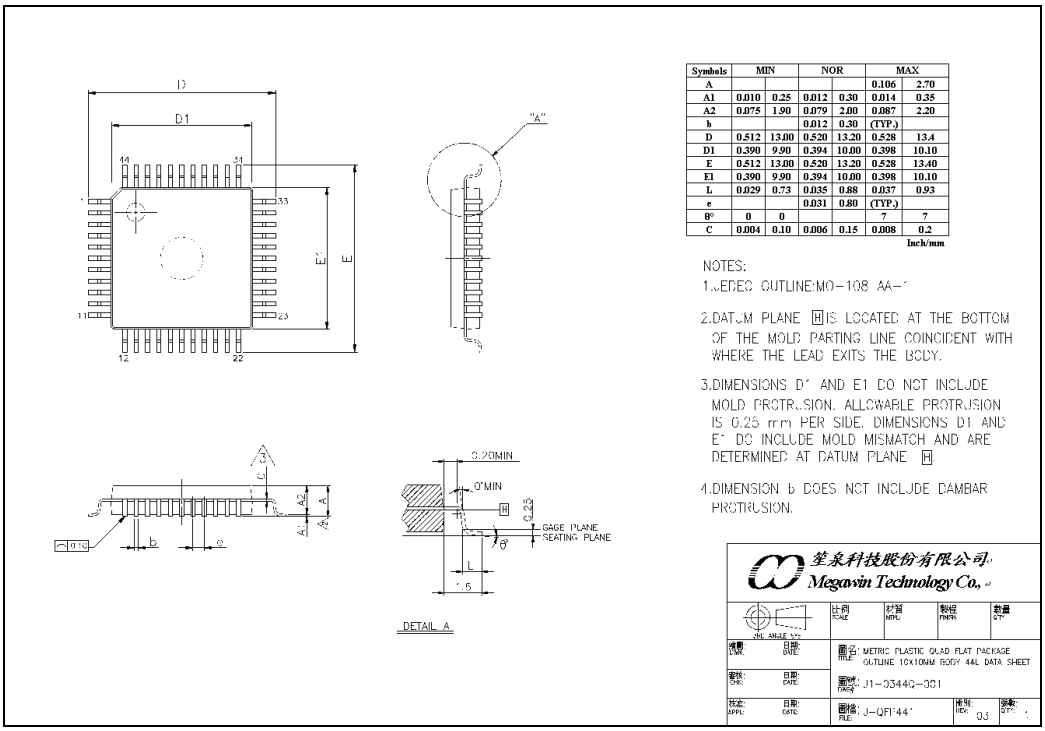
Symbols	MIN		NOR		MAX	
A					0.185	4.70
A1	0.020	0.51				
A2	0.145	3.68	0.150	3.81	0.155	3.94
b1	0.026	0.66	0.028	0.71	0.032	0.81
b	0.016	0.41	0.018	0.46	0.022	0.56
c	0.007	0.18	0.010	0.25	0.013	0.33
D	0.648	16.46	0.653	16.59	0.658	16.71
E	0.648	16.46	0.653	16.59	0.658	16.71
e			0.050	1.27	BSC	
Gd	0.590	14.99	0.610	15.49	0.630	16.00
Ge	0.590	14.99	0.610	15.49	0.630	16.00
Hd	0.680	17.27	0.690	17.53	0.700	17.78
He	0.680	17.27	0.690	17.53	0.700	17.78
L	0.090	2.29	0.100	2.54	0.110	2.79
Y					0.004	0.10

Inch/mm

* *NOTE:*

1. JEDEC OUTLINE : MO-047 AC
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY
3. DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PER SIDE. DIMENSIONS E AND D DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION .

16.3 44-Pin PQFP Package (MG87FE/L52AF)



Symbols	MIN		NOR		MAX	
A					0.106	2.70
A1	0.010	0.25	0.012	0.30	0.014	0.35
A2	0.075	1.90	0.079	2.00	0.087	2.20
b			0.012	0.30	(TYP.)	
D	0.512	13.00	0.520	13.20	0.528	13.4
D1	0.390	9.90	0.394	10.00	0.398	10.10
E	0.512	13.00	0.520	13.20	0.528	13.40
E1	0.390	9.90	0.394	10.00	0.398	10.10
L	0.029	0.73	0.035	0.88	0.037	0.93
e			0.031	0.80	(TYP.)	
θ°	0	0			7	7
C	0.004	0.10	0.006	0.15	0.008	0.2

Inch/mm

NOTES:

1. JEDEC OUTLINE:MO-108 AA-1

2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H]

4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

笙泉科技股份有限公司
Megawin Technology Co.,

METRIC PLASTIC QUAD FLAT PACKAGE OUTLINE 10x10MM BODY 44L DATA SHEET

J1-0344C-001

J-QFP44

17 Disclaimers

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

Life Support — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

Right to Make Changes — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).

18 Revision History

Revision	Description	Date	Page
Ver 1.0	Document create	2008/10/17	
Ver 1.1	Modified page-38 I_{IDLE} & I_{OP} current.	2008/11/24	38
Ver1.2	Added Internal oscillator description.	2008/12/20	36
Ver 1.3	Added external crystal Resistor & capacitor list	2008/12/25	36
Ver 1.4	Modified package form & order information	2009/04/18	2 & 3